# SECTION 3

# FUNCTIONAL AND INTERFACE DESCRIPTION

## 3.1 MEMORY MAP

If the on-board Program ROM is selected (by switch S1-4, see Table 2-4), the FDC module is assigned 4096 bytes ($8000-$8FFF). The first 3840 bytes ($8000-$8EFF) are available to the Program ROM while the last 256 bytes ($8F00-$8FFF) are dedicated to the I/O logic. Of these 256 bytes, only six are unique and are assigned to the controller device or module logic; the other 250 bytes are redundant, i.e., copies of these six bytes. Table 3-1 shows the general FDC Module Memory Map and Table 3-2 lists the FDC module detailed I/O functions.

The primitive subroutines and variables are identified in the FDC Primitive ROM (R323E), the AIM 65 DOS 1.0 ROM (R324E) and the AIM 65/40 DOS 1.0 ROM (R325E). If any of these ROMs are installed, the primitives require 90 bytes of off-board RAM; four bytes on page zero and 86 bytes on page four (see Table 4-7 for the variable address assignments). The primitives also require two RAM buffers for data input/output, each of which must be at least one sector in length (128 bytes for single-density or 256 bytes for double-density). See Section 4 for the description of the primitive routines. If the optional DOS 1.0 ROM is installed, it requires four additional bytes of RAM on page zero and 100 bytes on page five (see Tables 5-4 and 6-4 for AIM 65 and AIM 65/40 variable addresses, respectively). The default I/O buffer locations for the DOS are $600-$7FF for the AIM 65 and $3E00-$3FFF for the AIM 65/40 (these locations are user-alterable, see Tables 5-4 and 6-4). See Sections 5 and 6 for descriptions of the AIM 65 and AIM 65/40 DOS 1.0, respectively.

If the on-board Program ROM is not selected, the constraints on the base address (i.e., $8000-$8FFF) do not apply and the I/O logic may be assigned to any available page (see Section 2.2.1).

Table 3-1. FDC Module Memory Map

| Hex Addr. | Function | Hex Addr. | Function |
|---|---|---|---|
| $0000 | Page Zero RAM: $0D7 - $0DE<br>Page Four RAM: $4A0 - $4FA<br>Page Five RAM: $500 - $563<br>(Page Five for DOS use only) | $8000 | 15 Pages ROM: $8000 - $8EFF<br>1 Page I/O: $8F00 - $8FFF |
| $1000 | User Available | $9000 | User Available |
| $2000 | | $A000 | |
| $3000 | | $B000 | |
| $4000 | | $C000 | |
| $5000 | | $D000 | |
| $6000 | | $E000 | |
| $7000 | | $F000 | |

NOTES

1. Base Address Selection PROM is factory programmed to $8000.
2. RAM is not on the FDC module.
3. The DMAC module (optional) can be assigned to any available page.



Table 3-2. FDC Module I/O Memory Map

| Hex Addr. | Buffer/Register | |
|---|---|---|
| | Write (R/$\overline{W}$ = Low) | Read (R/$\overline{W}$ = High) |
| XY00 | Command Register | Status Register |
| XY01 | Track Register | Track Register |
| XY02 | Sector Register | Sector Register |
| XY03 | Data Register | Data Register |
| XY04 | Drive Control Register | Drive Status Register |
| XY15 | - - - | Force a not ready to stop the CPU until the FDC device is ready. |

NOTES

1. XY corresponds to the assigned Base Address of any two hexadecimal values. For the standard FDC, XY=8F.
2. The remaining locations in the I/O page are redundant.
3. The Drive Control Register is as follows:

| Bit | Meaning |
|---|---|
| 0 | Side Select: 0 = Side 1, 1 = Side 2 |
| 1 | Drive 1 Select: 1 = On |
| 2 | Drive 2 Select: 1 = On |
| 3 | Drive 3 Select: 1 = On |
| 4 | Drive 4 Select: 1 = On |
| 5 | 5" Motor On/8" Head Load: 1 = Active |
| 6 | STOPEN: 1 = Generate not ready, Clear IRQ |
| 7 | Density: 0 = Double, 1 = Single |

4. The Drive Status Register is as follows:

| Bit | Meaning |
|---|---|
| 0 | Selected Side: 0 = Side 2, 1 = Side 1 |
| 1 | - - - |
| 2 | - - - |
| 3 | - - - |
| 4 | - - - |
| 5 | Number of Heads: 0 = One, 1 = Two |
| 6 | Selected Size: 0 = 8", 1 = 5" |
| 7 | Selected Density: 0 = Single, 1 = Double |

## 3.2 FUNCTIONAL DESCRIPTION

The block diagram in Figure 3-1 identifies the FDC module functions and interface signals.

The Controller Clock derives a reference frequency for the FDC device from a crystal-controlled oscillator. This reference frequency is 1 MHz or 2 MHz, depending on the Standard/Mini-Floppy Selection Header position.

The FDC device, in conjunction with the Data Separator and Precompensation Circuitry, interfaces the RM 65 bus to the floppy disk medium. The circuitry supports 5-1/4" or 8" disks, with choice of single-density (FM) or double-density (MFM) soft sector formats. The FDC features powerful commands, including read/write head movements, reading and writing of data, and reading and writing of track format, with selectable record lengths. Write precompensation circuitry ensures reliable data recovery in double density formats. The Precompensation jumper (E1) selects precompensation on all tracks, only on tracks greater than 43, or no precompensation at all.

The Standard/Mini-Floppy Selection header (JB1, JB2) selects the Disk Drive connector (J1) and FDC circuitry for either 5" mini-floppy or 8" standard floppy disk formats. The 50-pin I/O receptacle connects the FDC module to a mass terminated cable connected to the installed disk drives. A 34-pin cable and mating connector can be used to connect the 5" mini-floppy drives while a 50-pin cable and mating connector is needed to connect to the 8" floppy drives.

The Drive Status Buffer allows detection of the Standard/Mini-Floppy Selection header and Dual Head Drive jumper (E3) positions, as well as selected density and side information.

The Drive Control Register provides control of the side and drive selection, motor on (5" only) or head load (8" only), the recording density, and the interrupt request disable.



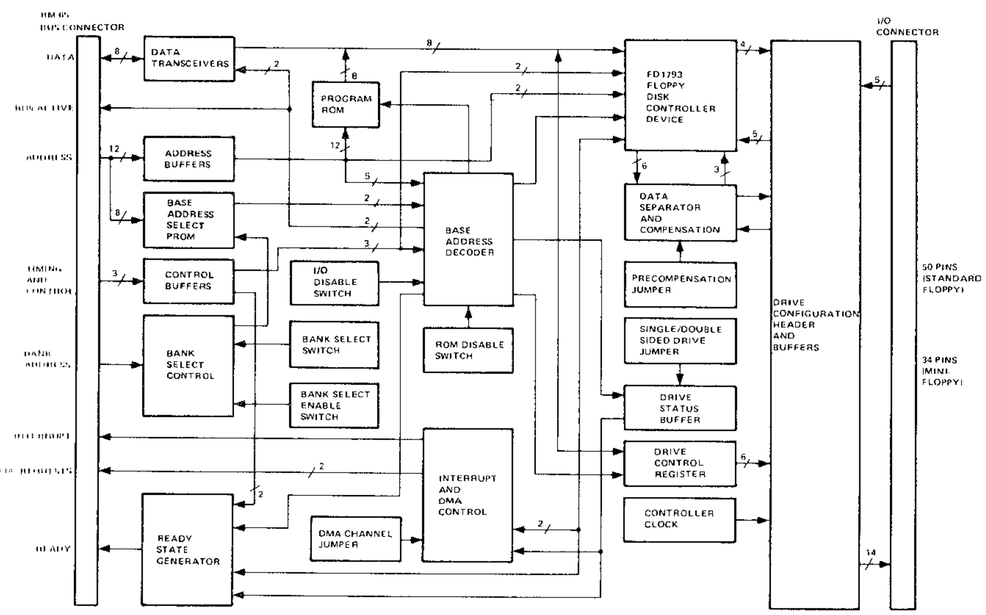


Figure 3-1. FDC Module Block Diagram

The Interrupt and DMA control circuit allows operation in either an interrupt-driven mode or under DMA control. An interrupt request latch holds all interrupt requests until serviced and cleared (STOPEN). DMA requests from the FDC module can be driven on either of two DMA request channels (BDRQ1/, BDRQ2/), as selected by the DMA Channel Selection jumper (E2), or disabled by removing the jumper.

The Ready State Generator provides wait states as required by the FDC device.

The Base Address Decoder, with the Base Address Select PROM (Z18), the Bank Select Control circuit, the ROM and I/O Disable switches (S1-2, S1-4), and the phase 2 and read/write signals control device selection on the module. The Base Address Select PROM compares the eight most significant address lines to the programmed addresses to generate device select signals to the Program ROM and the I/O devices. The ROM Disable switch assigns the module to be active either in a 256-byte page (disabled) or in a 4K-byte block (enabled). The I/O Disable switch allows the FDC I/O to be disabled.

When the ROM is disabled, only the I/O devices are active in the 256-byte page that matches all eight Base Address Select bits. For the I/O devices, the three least significant address lines, along with the phase 2 clock and read/write control signals, drive register select lines to the FDC device, and device select lines to the Drive Status Buffer and Drive Control Register.

When the ROM is enabled, the module is active in the 4K byte block that matches the four most significant Base Address Select bits. The program ROM is selected except when the address matches the four least significant Base Address Select bits, in which case the I/O device select lines are selected.



The Bank Select Control circuit detects when the module's assigned memory bank is addressed by comparing the bank address signal (BADR/) from the RM 65 bus to the Bank Select (S1-2) and Bank Select Enable (S1-1) switches. The Bank Select Enable switch allows the board to reside in common memory (both Bank Ø and Bank 1) or only in the bank set by the Bank Select switch (either Bank Ø or Bank 1).

The Control Buffers invert and transfer phase 2 clock (BØ2/), reset (BRES/), and read/write (BR/$\overline{W}$/) control signals from the RM 65 bus onto the module. The interrupt request (BIRQ/) is buffered and driven onto the RM 65 bus.

The Data Transceivers invert and buffer 8-bits of parallel data (BDØ/-BD7/) between the module and the RM 65 bus based on control signals from the Base Address Decoder and the Control Bufers. Data to the module is latched (Ø2) by the write data latch, extending the data hold time for the FDC device. Data from the module is buffered by the read data buffers. The transceivers are enabled by the Base Address Decoder when the module is addressed.

The Address Buffers invert and transfer 12 of the 16 parallel address bits (BAØ/-BA11/) from the RM 65 bus to the Base Address Decoder (AØ-A4), to the Program ROM (AØ-A11), and to the FDC device (AØ, A1).

## 3.3 INTERFACE DESCRIPTION

Tables 3-3 and 3-4 list the interface signals and pin assignments for connector P1 (RM 65 Bus) and connector J1 (Disk Drive), respectively.

Tables 3-5 and 3-6 define the interface signals for connectors P1 and J1, respectively.

Table 3-3. Connector P1 (RM 65 Bus) Pin Assignments

| Pin | Signal Mnemonic | Signal Name | Input/Output |
|---|---|---|---|
| Wa | | Not Connected (See Note) | |
| Wc | | Not Connected (See Note) | |
| Xa | +5V | +5 VDC (See Note) | |
| Xc | +5V | +5 VDC (See Note) | |
| 1a | GND | Ground | |
| 1c | +5V | +5 VDC | |
| 2a | BADR/ | Buffered Bank Address | I |
| 2c | BA15/ | Buffered Address Bit 15 | I |
| 3a | GND | Ground | |
| 3c | BA14/ | Buffered Address Bit 14 | I |
| 4a | BA13/ | Buffered Address Bit 13 | I |
| 4c | BA12/ | Buffered Address Bit 12 | I |
| 5a | BA11/ | Buffered Address Bit 11 | I |
| 5c | GND | Ground | |
| 6a | BA10/ | Buffered Address Bit 10 | I |
| 6c | BA9/ | Buffered Address Bit 9 | I |
| 7a | BA8/ | Buffered Address Bit 8 | I |
| 7c | BA7/ | Buffered Address Bit 7 | I |
| 8a | GND | Ground | |
| 8c | BA6/ | Buffered Address Bit 6 | I |
| 9a | BA5/ | Buffered Address Bit 5 | I |
| 9c | BA4/ | Buffered Address Bit 4 | I |
| 10a | BA3/ | Buffered Address Bit 3 | I |
| 10c | GND | Ground | |
| 11a | BA2/ | Buffered Address Bit 2 | I |
| 11c | BA1/ | Buffered Address Bit 1 | I |
| 12a | BA0/ | Buffered Address Bit 0 | I |
| 12c | BØ1 | Not Used | |
| 13a | GND | Ground | |
| 13c | BSYNC | Not Used | |
| 14a | BSD | Not Used | |
| 14c | BDRQ1 | Buffered DMA Request 1 | O |
| 15a | BRDY | Buffered Ready | O |



Table 3-3. Connector P1 (RM 65 Bus) Pin Assignments (Cont'd)

| Pin | Signal Mnemonic | Signal Name | Input/Output |
|---|---|---|---|
| 15c | GND | Ground | |
| 16a | | Not Used | |
| 16c | | Not Used | |
| 17a | +12V | +12V | |
| 17c | | Not Used | |
| 18a | GND | Ground | |
| 18c | | Not Used | |
| 19a | BFLT/ | Not Used | |
| 19c | BØØ | Not Used | |
| 20a | | Not Used | |
| 20c | GND | Ground | |
| 21a | BR/$\overline{W}$/ | Buffered Read/Write "Not" | I |
| 21c | BDRQ2/ | Buffered DMA Request 2 | O |
| 22a | | Not Used | |
| 22c | BR/$\overline{W}$ | Not Used | |
| 23a | GND | Ground | |
| 23c | BACT/ | Buffered Bus Active | O |
| 24a | BIRQ/ | Buffered Interrupt Request | O |
| 24c | BNMI/ | Not Used | |
| 25a | BØ2/ | Buffered Phase 2 "Not" Clock | I |
| 25c | GND | Ground | |
| 26a | BØ2 | Not Used | |
| 26c | BRES/ | Buffered Reset | I |
| 27a | BD7/ | Buffered Data Bit 7 | I/O |
| 27c | BD6/ | Buffered Data Bit 6 | I/O |
| 28a | GND | Ground | |
| 28c | BD5/ | Buffered Data Bit 5 | I/O |
| 29a | BD4/ | Buffered Data Bit 4 | I/O |
| 29c | BD3/ | Buffered Data Bit 3 | I/O |
| 30a | BD2/ | Buffered Data Bit 2 | I/O |
| 30c | GND | Ground | |
| 31a | BD1/ | Buffered Data Bit 1 | I/O |

Table 3-3. Connector P1 (RM 65 Bus) Pin Assignments (Cont'd)

| Pin | Signal Mnemonic | Signal Name | Input/Output |
|---|---|---|---|
| 31c | BDØ/ | Buffered Data Bit Ø | I/O |
| 32a | +5V | +5 VDC | |
| 32c | GND | Ground | |
| Ya | +5V | +5 VDC (See Note) | |
| Yc | +5V | +5 VDC (See Note) | |
| Za | | Not Connected (See Note) | |
| Zc | | Not Connected (See Note) | |

NOTES

1. Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are available on Edge Connector version only.
2. "/" suffix denotes signal active at negative or low voltage level.



Table 3-4. Connector J1 (Disk Drive) Pin Assignments

| FDC Module I/O Connector Pin | Standard Floppy Disk Drive Interface Cable Connector | | Mini-Floppy Disk Drive Interface Cable Connector (2) | |
|---|---|---|---|---|
| | Pin | Signal Name | Pin | Signal Name |
| 2 | 2 | Track >43 (Remex & MFE or equivalents) | | |
| 4 | 4 | N.C. | | |
| 6 | 6 | N.C. | | |
| 8 | 8 | Track >43 (C. disk or equivalents) | | |
| 10 | 10 | N.C. | | |
| 12 | 12 | N.C | | |
| 14 | 14 | 2 .J Side Select | | |
| 16 | 16 | N.C. | | |
| 18 | 18 | Head Load | 2 | N.C. |
| 20 | 20 | Index | 4 | N.C. |
| 22 | 22 | Drive Ready | 6 | Drive Select #4 |
| 24 | 24 | N.C. | 8 | Index |
| 26 | 26 | Drive Select #1 | 10 | Drive Select #1 |
| 28 | 28 | Drive Select #2 | 12 | Drive Select #2 |
| 30 | 30 | Drive Select #3 | 14 | Drive Select #3 |
| 32 | 32 | Drive Select #4 | 16 | Motor On |
| 34 | 34 | Direction In | 18 | Direction In |
| 36 | 36 | Step Pulse | 20 | Step Pulse |
| 38 | 38 | Write Data | 22 | Write Data |
| 40 | 40 | Write Gate | 24 | Write Gate |
| 42 | 42 | Track Zero | 26 | Track Zero |
| 44 | 44 | Write Protected | 28 | Write Protected |
| 46 | 46 | Read Data | 30 | Read Data |
| 48 | 48 | N.C. | 32 | 2nd Side Select |
| 50 | 50 | N.C. | 34 | N.C. |

NOTES:

1. All odd numbered pins are GND.
2. Pin 1 of the 34-pin mini-floppy disk drive interface cable connector should be keyed to pin 17 of the FDC module I/O connector.

Table 3-5. Connector P1 (RM 65 Bus) Signal Descriptions

| Mnemonic | Signal Name and Signal Description |
|---|---|
| +5V | +5 VDC supplied to the module from the RM 65 Bus. |
| +12V | +12 VDC supplied to the module from the Bus. |
| GND | Ground<br>System ground. |
| BA0/-BA15/ | Buffered Address Bits 0-15<br>Sixteen address lines transfer an inverted 16-bit parallel address from the Bus to the module. |
| BADR/ | Buffered Bank Address<br>A high BADR/ signal addresses the lower 65K (Bank 0) memory bank; a low BADR/ addresses the upper 65K (Bank 1) memory bank. |
| BD0/-BD7/ | Buffered Data Bits 0-7<br>Eight bidirectional inverted data lines transfer 8-bit data bytes between the Data Transceivers in the module and the Bus. |
| BACT/ | Buffered Bus Active<br>A low BACT/indicates that the module has been addressed and the Data Transceivers are enabled in either the receive (write operation) or transmit (read operation) direction. |
| B02/ | Buffered Phase 2 Clock "NOT"<br>The B02/ signal synchronizes data transfers on the Bus. The address and read/write lines are setup in the positive portion of B02/. The data lines are set-up in the negative portion of B02/. |



Table 3-5. Connector P1 (RM 65 Bus) Signal Descriptions (Cont'd)

| Mnemonic | Signal Name and Signal Description |
|---|---|
| BR/$\overline{W}$/ | Buffered Read/Write "Not"<br>The BR/$\overline{W}$/ signal controls the direction of data transfer on the Bus. A low BR/$\overline{W}$/ indicates a read operation. A high BR/$\overline{W}$/ indicates a write operation. |
| BRDY | Buffered Ready<br>The BRDY signal is generated by the module. When the R6502 CPU receives a low BRDY, the CPU will stop execution in the next read cycle. Execution will resume when BRDY returns high. |
| BIRQ/ | Buffered Interrupt Request<br>The BIRQ/ signal is generated by the module for the Bus to request interrupt service. BIRQ/ is forced low by any interrupt condition in the FDC device. |
| BDRQ1/,<br>BDRQ2/ | Buffered DMA Requests 1 and 2<br>Either BDRQ1/ or BDRQ2/ can be assigned to the module to request DMA service. When the FDC is ready for a data byte transfer, a DMA request is generated. |
| BRES/ | Buffered Reset<br>The BRES/ signal is received by the module from the Bus. A low BRES/ clears the Drive Status Register and the Wait State Generator, and resets the FDC device. |
| | NOTE<br>All signals interfaced to and from the module are driven at TTL voltage levels. |

Table 3-6. Connector J1 (Disk Drive) Signal Descriptions

| Signal Name and Signal Description | Signal Source |
|---|---|
| Drive Select No. 1 to No. 4<br>These signals allow up to four disk drives to to be individually selected by the FDC when active. | FDC |
| Second Side Select<br>This signal is used by the FDC to access side 1 when inactive and side 2 when active. | FDC |
| Index<br>This signal is pulsed (logic Ø) by the selected disk drive when the one disk medium is at the start of a revolution. | Drive |
| Read Data<br>This signal is the serial NRZ data from the selected disk drive medium (FM if single-density, MFM if double-density). | Drive |
| Write Data<br>This signal is the serial NRZ data from the FDC to be written to the selected disk drive medium (FM is single-density, MFM if double-density). | FDC |
| Write Gate<br>This signal, when made active by the FDC, indicates that the Write Data line is valid. When inactive, the FDC is in the read mode. | FDC |
| Track Zero<br>This signal is made active by the selected disk drive when the read/write head is on the outermost track. | Drive |



Table 3-6. Connector J1 (Disk Drive) Signal Descriptions (Cont'd)

| Signal Name and Signal Description | Signal Source |
|---|---|
| Direction In<br>This signal is made active by the FDC when the read/write head of the selected disk drive is to be moved toward an inner (higher number) track. When inactive, movement will be toward an outer (lower number) track. | FDC |
| Step Pulse<br>This signal is pulsed (logic Ø) by the FDC to move the read\write head of the selected floppy drive in the direction set by the Direction In signal. The head moves one track position on each negative transition. | FDC |
| Write Protected<br>This signal is made active by the selected disk drive to indicate that the medium is write protected. For 5" drives, this means the write protect tab is on the disk; for 8" drives, this means the write protect notch is not covered. | Drive |
| Motor On (5" Drive Only)<br>This signal, when made active by the FDC, turns on the motor of the selected disk drive. | FDC |
| Head Load (8" Drive Only)<br>This signal, when made active by the FDC, lowers the read/write head of the selected disk drive onto the medium. | FDC |

Table 3-6. Connector J1 (Disk Drive) Signal Descriptions (Cont'd)

| Signal Name and Signal Description | Signal Source |
|---|---|
| Drive Ready (8" Drive Only)<br>This signal is made active by the selected disk drive to indicate that it is ready for data transfers. | Drive |
| Track >43 (8" Drive Only)<br>This signal is made active by the selected disk drive when the read/write head is positioned on an inner track (track 44 and higher). | Drive |

NOTE

All signals interfaced to and from the module are driven at standard TTL voltage levels. An active signal (logic 0) is an electrical low while an inactive (logic 1) is an electrical high.



### 3.3.1 Mini-Floppy Disk Drive Interface Cable Assembly

The mating ribbon cable connector to the Disk Drive connector (J1) must be a 50-pin mass terminating receptacle (3M No. 3425-6000 or equivalent). For interfacing with industry standard 5" mini-floppy disk drives, this connector must be attached to a 34 wire ribbon cable, displaced such that wire 1 mates to pin 17, and wire 34 mates to pin 50.

The mini-floppy disk drives (Shugart SA-450 or equivalent) have a 34-pin edge connector for the signal interface, with a pin assignment shown in Table 3-6. Up to four 34-pin mass terminating card edge receptacles (3M No. 3463-0001 or equivalent) may be attached to the ribbon cable, one connector for each drive used. The cable length should be less than four feet, however, spacing between connectors is not critical. Figure 3-2 shows the typical connector placement.

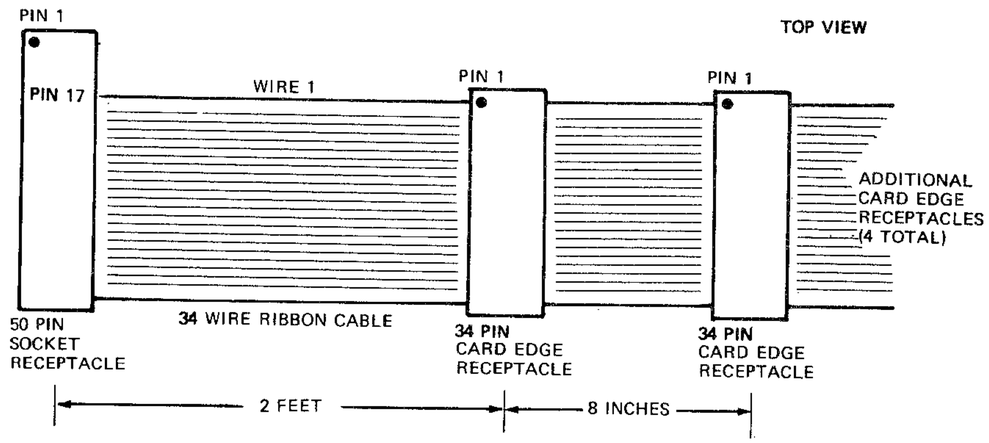


Figure 3-2. Mini-Floppy Disk Drive Interface Cable

### 3.3.2 Standard Floppy Disk Drive Interface Cable Assembly

The mating ribbon cable connector to the Disk Drive connector (J1) must be a 50-pin mass terminating receptacle (3M No. 3425-6000 or equivalent). For interfacing with industry standard 8" floppy disk drives, this connector must be attached to a 50 wire ribbon cable with wire 1 mating to pin 1.

The standard floppy disk drives (Shugart SA-850 or equivalent) have a 50-pin card edge connector for the signal interface, with a pin assignment shown in Table 3-6. One 50-pin mass terminating card edge receptacle (3M No. 3415-0001 or equivalent) must be attached to the ribbon cable for each drive used (maximum of four). The cable length should be less than four feet, however, spacing between connectors is not critical. Figure 3-3 shows the typical connector placement.

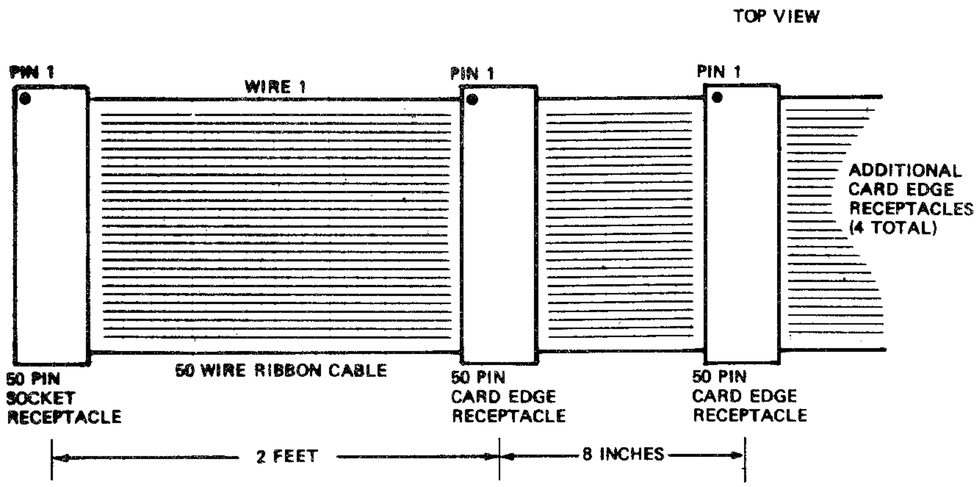


Figure 3-3. Standard Floppy Disk Drive Interface Cable



SECTION 4

# FDC MODULE PRIMITIVE ROUTINES

## 4.1 PRIMITIVE ROUTINE DESCRIPTIONS

The FDC primitive routines simplify the operation of the FDC module by:

- Handling the detail protocol to interface with the FD 1793 Floppy Disk Controller device.
- Providing a set of closed subroutines that initialize and format a disk, position drive heads, write data on a disk, and read data from a disk.

These primitives allow additional higher level functions, such as a disk operating system or specialized data recording, to be easily implemented without being concerned with the detailed operation of the controller device. The optional AIM 65 DOS 1.0 and AIM 65/40 DOS 1.0 functions described in Section 5 and 6, respectively, use these primitive routines. If you are using one of these DOS versions, skip to the appropriate section. If you are designing a DOS or other specialized disk interface/file handling function using the primitive routines, the detailed description of these routines included in this section will be helpful.

The primitive routines perform the following major functions to support operation of up to four disk drives (single- or double-sided; single- or double-density:

Format a Disk
Read or Write a Sector
Seek or Verify Seek of a Track
Reset or Re-zero the Head
Read or Write Multiple Sectors
Read or Write a Track
Turn Motors On or Off
Select or De-select any Drive