SECTION 7
AIM 65 SYSTEM DESCRIPTION

This section describes the AIM 65 hardware and software. The hardware is segmented into logical functional areas for ease of description. The AIM 65 Monitor, Editor and Assembler software are also described. User available subroutines are described along with the calling procedures and conditions.

7.1 OVERVIEW

Aim 65 is a complete microcomputer system. It contains an R6502 CPU, programmed instructions in ROM, RAM, and peripheral equipment in the form of a display, a printer and a keyboard. On- and off-board expansion capabilities enhance the usability of AIM 65. True application ease is provided by a user dedicated R6522 Versatile Interface Adapter.

The major components are shown on the AIM 65 block diagram in Figure 7-1.

7.2 FUNCTIONAL AREAS

The hardware functional areas are

Power Distribution

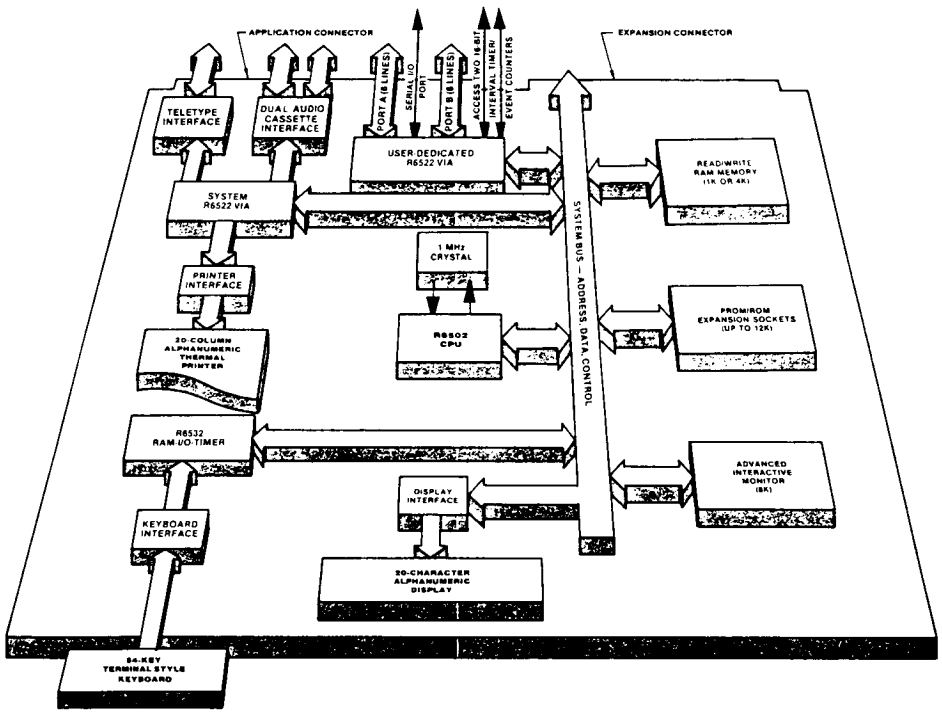

Figure 7-1. AIM 65 Block Diagram

Timing and Control
Chip Select
RAM
ROM
Printer Interface
Display Interface
Keyboard Interface
User R6522 Interface
Audio Cassette Recorder Interface
TTY and Serial Interface

7.2.1 Power Distribution

Power is routed from TB1 terminal strip connections to on-board devices and to interface connectors. Figure 7-2 shows the power distribution. +5V is required for AIM 65, audio, and TTY operation. +5V is also routed from TB1-3 to both the Expansion and Application Connectors.

+24V, required for AIM 65 printer and TTY interface circuitry operation, is routed from TB1-6 to the printer and TTY interface circuitry on the Master Module only. A jumper will extend it to Pin Z on the Application Connector.

+12V and -12V are not required for AIM 65 operation, but are routed from TB1 to the Expansion and Application Connectors for external enhancements. -12V requires a jumper for extension to the Application Connector.

7.2.2 Timing and Control

The Timing and Control area includes the R6502 CPU, the address, data and control bus lines, the R6502 clock

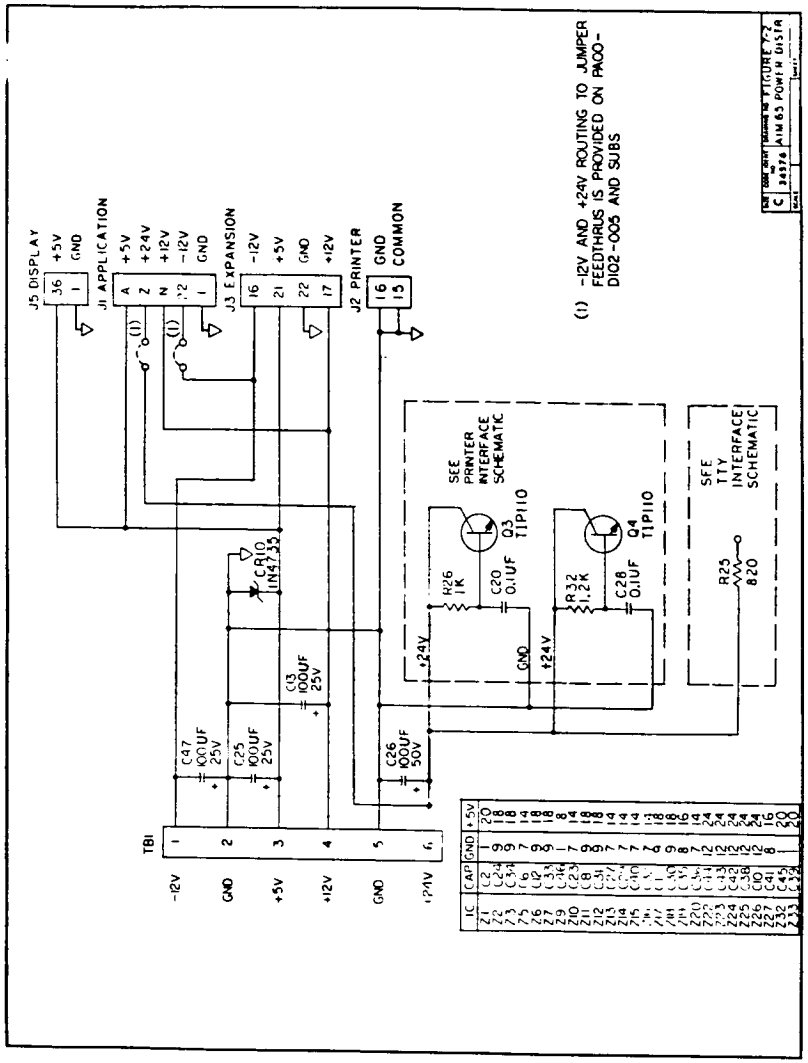

Figure 7-2. AIM 65 Power Distribution Schematic

circuitry, the Monitor R6522 VIA (Z32) interface and the AIM 65 control switches (the RESET pushbutton, the RUN/STEP switch and the KB/TTY switch). Figure 7-3 shows the Timing and Control elements.

R6502

The R6502 8-bit microprocessor, the central processing unit (CPU) of the AIM 65, provides the overall control and monitoring of all AIM 65 operations.

The R6502 communicates with other AIM 65 elements on three separate buses. A 16 bit address bus allows the CPU to directly address 65,536 memory locations. An 8-bit bidirectional data bus carries data from the R6502 CPU to/from memory and interface devices. The control bus carries various timing and control signals between the R6502 CPU and interfacing peripherals, devices and off-board elements.

Section 2 in the R6500 Hardware Manual describes the operation of the R6502 and the bus lines.

R6502 Clock

The R6502 on AIM 65 operates at 1 MHz. The frequency reference is a 4 MHz crystal controlled oscillator. Dual D-type flip-flop Z10 divides the 4 MHz signal by four to drive the R6502 phase 0 (ø0) input with a 1 MHz clock.

The R6502 generates the Phase 1 (ø1) and Phase 2 (ø2) clock outputs based on the Phase 0 input clock. The ø1 (OUT) is routed to J3-3 for external use.

The ø2 (OUT) from the R6502 is routed to J1-C and to inverter J16-9. An ø2 signal provided by J16-8 is routed to J3-Y and Z16-11. A buffered ø2 clock (SYS ø2) generated by Inverter Z16-10 provides the system level timing reference for on-board and expansion use (at J3-U).

R/$\overline{W}$

The Read/Write (R/$\overline{W}$) signal controls the direction of data transfers between the R6502 and interfacing devices. The R/$\overline{W}$ signal is routed to J1-D and Inverter Z16-3. A buffered R/$\overline{W}$ signal from Z16-6 provides the system level R/$\overline{W}$ signal (SYS R/$\overline{W}$) for on-board and expansion use (at J3-V).

CONTROL SWITCHES

RESET

Pushbutton switch S1 initiates RESET of the AIM 65 hardware and software. Timer Z4 holds the $\overline{RES}$ low for at least 15 ms from the time the pushbutton is released. $\overline{RES}$ is routed to the R6502 CPU, the Monitor R6522 (Z32), the Monitor R6532 RIOT (Z33), the user R6522 VIA (Z1), and the display R6520 PIA (U1). To initiate the device RESET function is also routed to the expansion connector for off-board RESET functions. The Monitor performs a software reset when the $\overline{RES}$ line goes high (see Section 7.3.1).

KB/TTY

The position of Switch S3 (KB/TTY) tells AIM 65 to accept commands from either the AIM 65 or the TTY keyboard. This switch is sampled through the Monitor R6522.

STEP/RUN

Switch S2 (STEP/RUN) causes AIM 65 to operate either in the RUN mode or the single STEP mode. In the STEP mode, the $\overline{NMI}$ interrupt line is driven low when SYNC and ø2 go high during instruction execution if the address lines are outside the A000-FFFF range. The $\overline{NMI}$ interrupt occurs on the high to low transition of the $\overline{NMI}$ line. The Monitor software will trace instructions and register, outside the Monitor instruction address range if the trace modes are selected and the NMI Interrupt Routine is not bypassed (see Section 7.7).

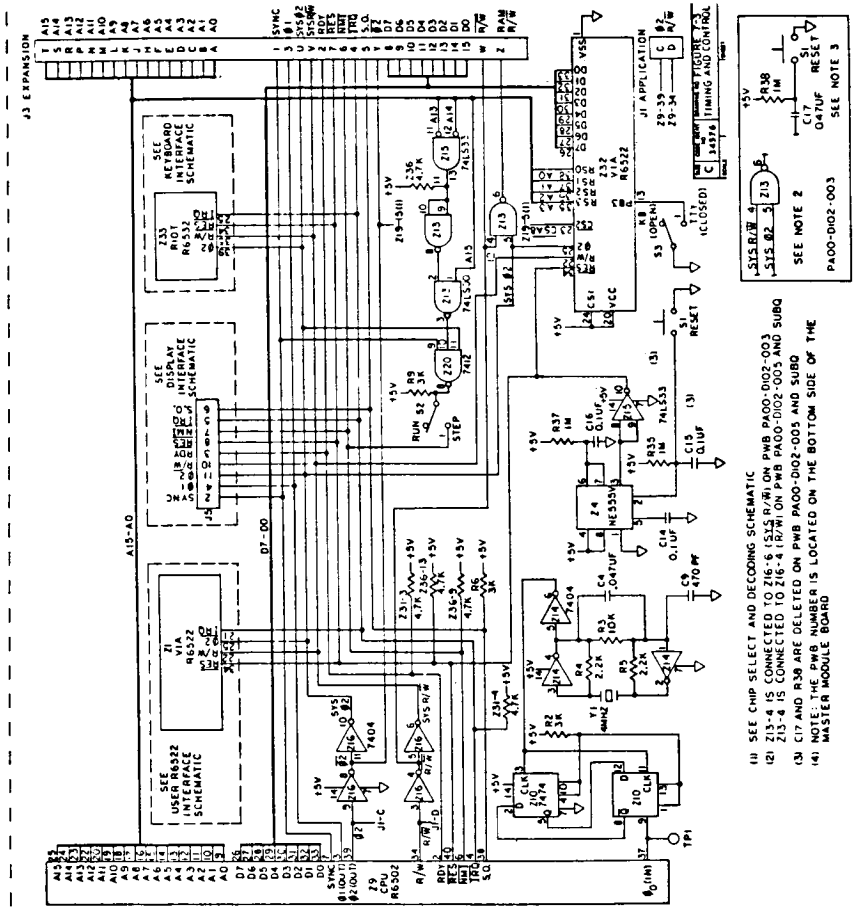

Figure 7-3. Timing and Control Schematic

7.2.3 Chip Select

The chip select function is performed by Decoders Z27 (1 of 8) and Z19 (Dual 2 to 4). See Figure 7-4.

Z27 decodes the upper four address lines (A12-A15) into one of eight possible chip select output lines. Each output line is active over a 4K address range, as shown in Table 7-1. Table 7-2 is the logic table for the Z27 device.

$\overline{CS8}$, $\overline{CS9}$ and $\overline{CSA}$ are routed to the J3 Expansion Connector for off-board use. $\overline{CSA}$ is routed to Z19 to enable the basic Master Module I/O device address select. Any use of $\overline{CSA}$ off-board for additional chip select must not conflict with the on-board use of the A000-AFFF address range (See the AIM 65 Detail Memory Map in Table 7-11.)

$\overline{CSB}$ - $\overline{CSF}$ are routed to the on-board PROM/ROM sockets Z26 - Z22, respectively. Each installed PROM/ROM may use the total 4K address range selected by the respective chip select line. Socket compatible PROM devices with a smaller address range may be directly used, however. In this case the available address range extends from the lowest available address in the range to the upper limit of the installed PROM/ROM.

Z19 performs address decoding for on-board RAM and I/O peripheral chip selection. Z19 contains two independent decoders, each decoding two input lines into one of four possible output lines. Each of the two sides of Z19 decode a selected address range of 1K. Table 7-1 shows the specific address ranges corresponding to the Z19 output chip select lines.

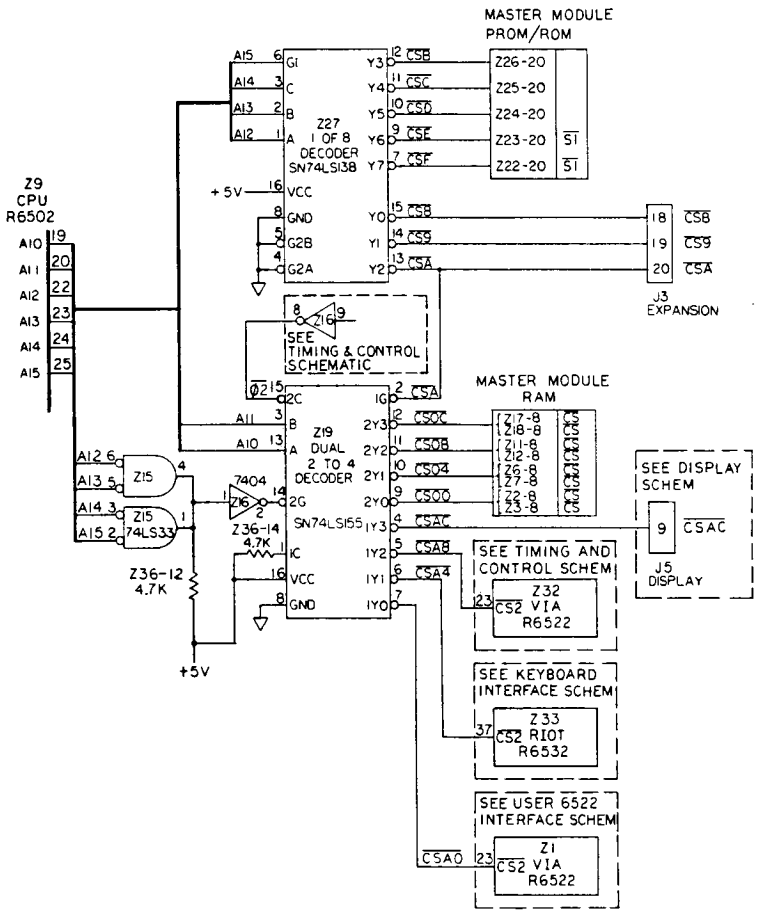

Figure 7-4. Chip Select and Decode Schematic

Side 1 of Z19 performs the individual I/O device select function (see Table 7-3). When $\overline{CSA}$ is low, address lines A10 and A11 are decoded to drive one of the $\overline{CSA0}$-$\overline{CSAC}$ output lines to the active low state. This divides the 4K I/O address range into four 1K segments. Each 1K address segment is allocated to one of the four on-board peripheral I/O devices. See Table 7-7 for the I/O memory allocation.

Side 2 of the Z19 outputs the on-board RAM chip select signals (see Table 7-4). When A12, A13, A14, and A15 are low, A10 and A11 are decoded to drive one of the four $\overline{CS00}$-$\overline{CS0C}$ output lines to the active low state. Each chip select line is routed to two on-board RAM sockets.

Table 7-1. Chip Select Logic Table

ADDRESS RANGE LOW - HIGH	INPUT ADDRESS LINES A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	OUTPUT ON-BOARD RAM SELECT CS0C	CS08	CS04	CS00	EXPAND SELECT CS8	CS9	ON-BOARD I/O SELECT CSA	CSAC	CSA8	CSA4	CSA0	ON-BOARD ROM SELECT CSF	CSE	CSD	CSC	CSB
0000-03FF	L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
0400-07FF	L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
0800-0BFF	L	L	L	L	H	L	X	X	X	X	X	X	X	X	X	X	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0C00-0FFF	L	L	L	L	H	H	X	X	X	X	X	X	X	X	X	X	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
8000-83FF	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
9000-93FF	H	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
A000-A3FF	H	L	H	L	L	L	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
A400-A7FF	H	L	H	L	L	H	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
A800-ABFF	H	L	H	L	H	L	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	H
AC00-AFFF	H	L	H	L	H	H	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
B000-B3FF	H	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
C000-C3FF	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
D000-D3FF	H	H	L	H	X	X	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
E000-E3FF	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
F000-F3FF	H	H	H	H	X	X	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H

H = High L = Low X = Irrelevant

Table 7-2. Z27 SN74LS138 Decode Logic

INPUTS						OUTPUTS							
ENABLE		SELECT											
G1 A15	G2*	C A14	B A13	A A12		Y7 $\overline{CSF}$	Y6 $\overline{CSE}$	Y5 $\overline{CSD}$	Y4 $\overline{CSC}$	Y3 $\overline{CSB}$	Y2 $\overline{CSA}$	Y1 $\overline{CS9}$	Y0 $\overline{CS8}$
X	H	X	X	X		H	H	H	H	H	H	H	H
L	X	X	X	X		H	H	H	H	H	H	H	H
H	L	L	L	L		H	H	H	H	H	H	H	L
H	L	L	L	H		H	H	H	H	H	H	L	H
H	L	L	H	L		H	H	H	H	H	L	H	H
H	L	L	H	H		H	H	H	H	L	H	H	H
H	L	H	L	L		H	H	H	L	H	H	H	H
H	L	H	L	H		H	H	L	H	H	H	H	H
H	L	H	H	L		H	L	H	H	H	H	H	H
H	L	H	H	H		L	H	H	H	H	H	H	H

H = High Level L = Low Level X = Irrelevant

*G2 = G2A + G2B = always L (GND)

Table 7-3. Z19 SN74LS155 Decode Logic - Side 1 ($\overline{CSA0}$-$\overline{CSAC}$)

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B A11	A A10	1G $\overline{CSA}$	1C*	1Y3 $\overline{CSAC}$	1Y2 $\overline{CSA8}$	1Y1 $\overline{CSA4}$	1Y0 $\overline{CSA0}$
X	X	H	X	H	H	H	H
L	L	L	H	H	H	H	L
L	H	L	H	H	H	L	H
H	L	L	H	H	L	H	H
H	H	L	H	L	H	H	H
X	X	X	L	H	H	H	H

H = High Level L = Low Level X = Irrelevant

* = Wired High

Table 7-4. Z19 SN74LS155 Decode Logic - Side 2 ($\overline{CS00}$-$\overline{CS0C}$)

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G*	2C	2Y0	2Y1	2Y2	2Y3
A11	A10		02	$\overline{CS00}$	$\overline{CS04}$	$\overline{CS08}$	$\overline{CS0C}$
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

H = High Level L = Low Level X = Irrelevant

*2G = $\overline{A12} \cdot \overline{A13} \cdot \overline{A14} \cdot \overline{A15}$

7.2.4 RAM

The R2114 Static RAM is organized 1024 words by 4-bits. One pair of R2114s are used to provide 1K 8-bit bytes. The I/O lines of one R2114 are connected to data lines D0-D3 to provide the LSD of the bytes (bits 0-3). The I/O lines of the other R2114 are connected to D4-D7 to provide the MSD of the byte (bits 4-7). Figure 7-5 shows the connection to the AIM 65 address, data and control bus lines.

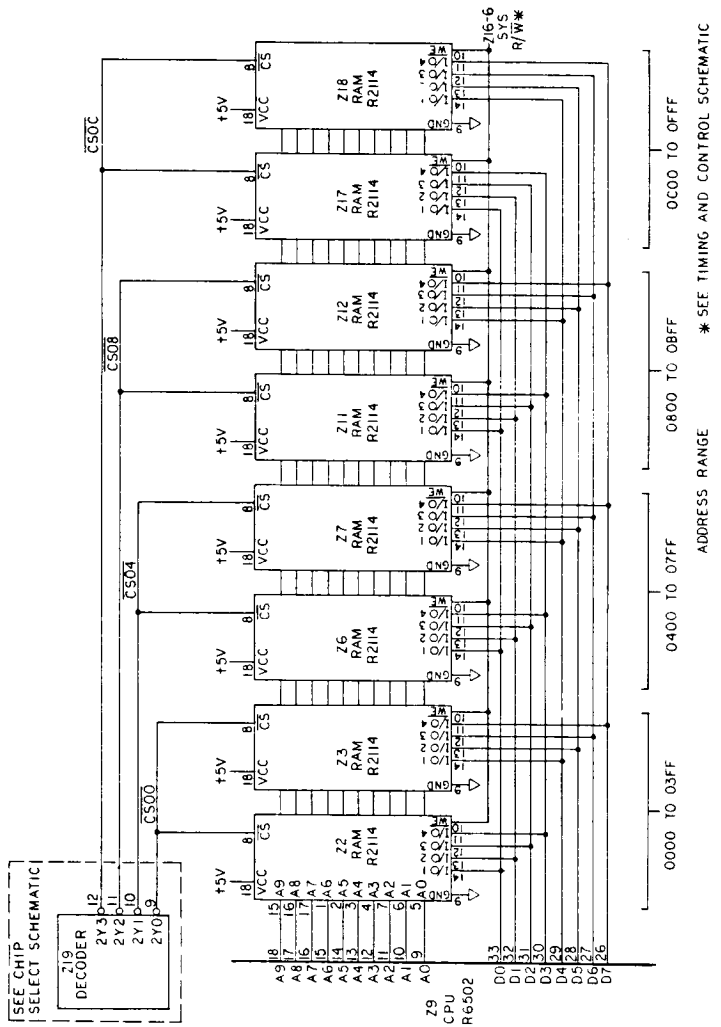

Figure 7-5. RAM Interface Schematic

Each RAM device Chip Select ($\overline{CS}$) line is connected to one of the RAM Chip Select lines ($\overline{CS00}$-$\overline{CS0C}$). When CS is low, the data in the R2114 will be placed on the device I/O lines (I/01-I/04), per address lines A0-A9.

The R2114 Write Enable ($\overline{WE}$) line is connected to SYS R/$\overline{W}$. When $\overline{WE}$ (and/or $\overline{CS}$) is high, the R2114 data input buffers are inhibited to prevent data from being written into the internal memory. Data within the RAM is changed only when both $\overline{CS}$ and $\overline{WE}$ are both low.

RAM must be installed in Z2 and Z3 sockets to provide Page 0 and Page 1 addresses for the AIM 65 to operate. RAM may be installed optionally in the other sockets for on-board RAM expansion. The R2114 RAM devices must be added in pairs Z6 and Z7, Z11 and Z12, or Z17 and Z18 to provide complete bytes of data.

7.2.5 ROM

Five PROM/ROM sockets are provided on the AIM 65 Master Module. Each socket can accept a 4K R2332 ROM or compatible PROM (see Figure 7-6)

The R2332 is a 32,768-bit static ROM, organized 4,096 words X 8 bits. The two chip select lines, S1/$\overline{S1}$/NC and S2/$\overline{S2}$/NC, are mask programmed to the desired logic level. In AIM 65 the S1/$\overline{S1}$/NC line is masked to the $\overline{S1}$ state, i.e., active low, while the S2/$\overline{S2}$/NC line is masked to the S2 level, i.e.,active high. S2 is wired to +5V to be continuously high. $\overline{S1}$ is wired to one of the AIM 65 chip select lines $\overline{CSA}$-$\overline{CSF}$.

When $\overline{S1}$ is low, the data addressed by lines A0 to A11 is placed on data lines D0-D7.

The AIM 65 Monitor is stored in R2332 devices P/N R3222 (Z22) and in P/N R3223 (Z23). The optional AIM 65 Assembler is masked into R2332 P/N R3224 for installation in Z24. The optional 8K AIM 65 BASIC Interpreter is available in R2332, P/N R3225, and P/N R3226 for installation in Z25 and Z26, respectively.

Pin compatible PROMs may be directly installed in Z24 - Z26 to operate in conjunction with the AIM 65 Monitor. The AIM 65 Monitor ROM may also be replaced, if desired, with a user provided Monitor program. The only restriction is that the interrupt vectors are located at $FFFA-$FFFF. See Section 7.8 for a discussion of the interrupt vectoring.

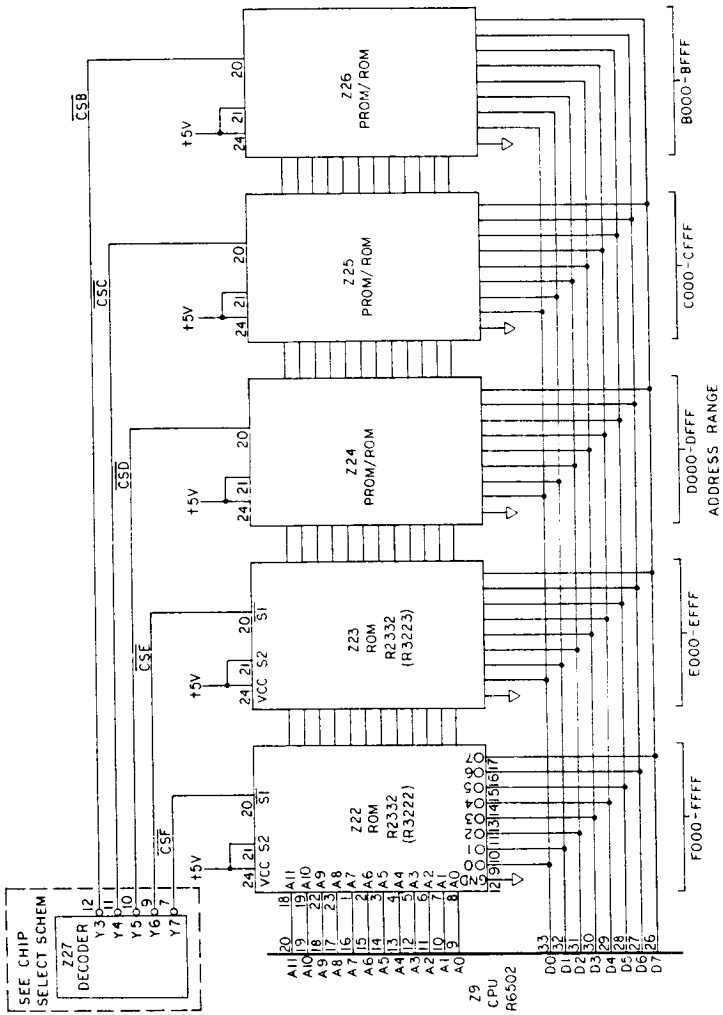

Figure 7-6. PROM/ROM Interface Schematic

7.2.6 Printer Interface

CAUTION

This section is presented for information only. Since improper timing of the print commands may damage the printer thermal head, it is not recommended that user prepared printer interface functions be attempted. The monitor output subroutines described in Table 7-13 may, however, be safely used.

The printer prints on heat sensitive roll paper by means of ten thermal elements, each of which can print two 5 x 7 matrix dot characters. The 10 thermal elements are mounted in fixed positions on a moveable thermal head. During a print cycle, the thermal head is driven back and forth horizontally allowing a row of dots to be printed during movement in each direction. The individual thermal elements are turned on for discrete intervals during the thermal head movement to form partial characters. After a row of dots has been printed, the motor driven platen advances the paper vertically by one dot row. A full line of formed characters is complete after seven dot rows are printed. The printer column layout and dot progression are illustrated in Figure 7-7. The printed characters are formed by dot patterns stored in the AIM 65 Monitor. The print cycle set-up, sequencing and timing is also controlled by the AIM 65 Monitor.

The hardware interface with the printer is provided by a portion of the AIM 65 Monitor R6522 VIA (Z32) and discrete circuitry (see Figure 7-8).

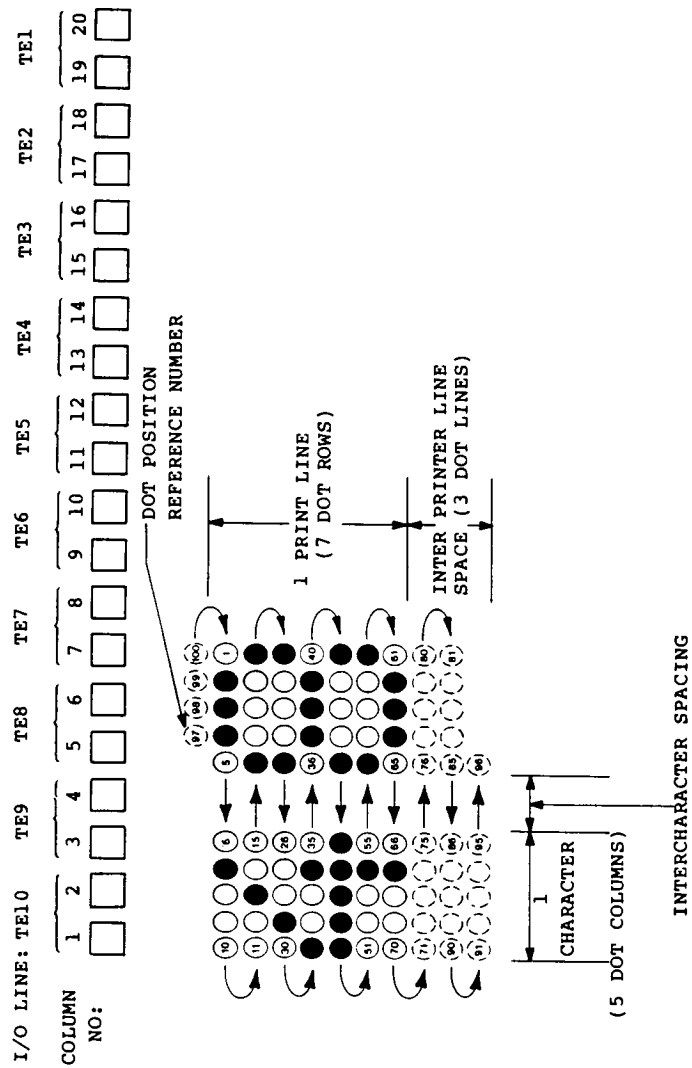

Figure 7-7. Printer Column Layout and Dot Progression

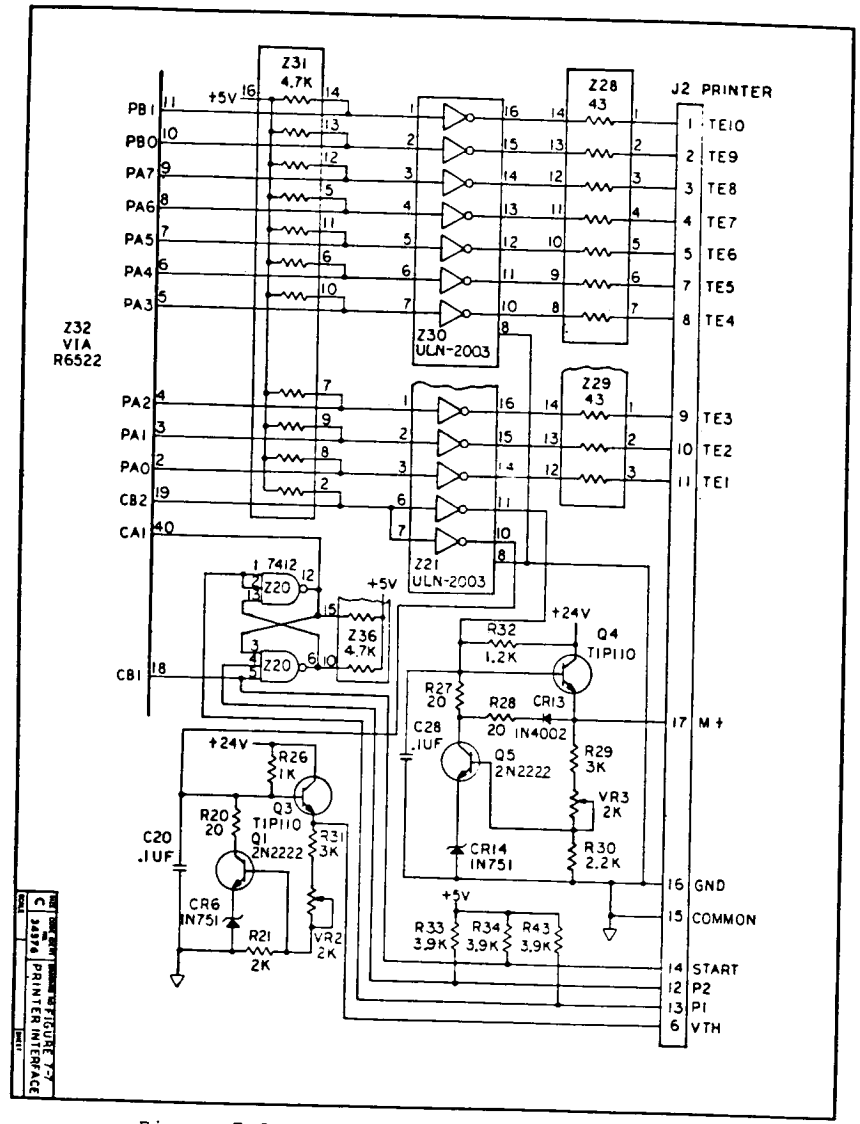

Figure 7-8. Printer Interface Schematic

CB2 operates as a discrete output to drive the motor and thermal head control circuits. A logic 0 to CB2 turns on the control circuits, logic 1 turns them off.

Motor control is provided by the Q4 power driver and Q5 feedback regulator. The output voltage on M+ varies from about 14 to 16 Vdc as adjusted by VR3, which controls the motor speed. The output voltage is zero when CB2 is logic 1. This circuit also dissipates back EMF energy generated by the motor when the motor is turned off, which provides required motor dynamic braking.

The Q3 power driver and Q1 feedback regulator and associated components provide the printer thermal head element voltage. When CB2 is logic 0, the output voltage on VTH varies from about 18 to 20 Vdc as adjusted by VR2, which controls the intensity of the printer. The output voltage is zero when CB2 is logic 1.

When the thermal head is turned on, the printer will print depending on the state of the ten thermal element lines. Thermal element lines TE1-TE10 are controlled by PA0-PA7, PB0 and PB1, respectively. When the I/O line is low (logic 0), the thermal element is turned off and will not print.

The motor operation and thermal head position is monitored by the START, P1 and P2 output lines from the printer. The printer START signal generates a negative pulse when the motor is turned on and at the start of each printed dot row. CB1 is configured to detect a negative transition of the pulse leading edge. The START signal also resets the Z20 P1/P2 debounce flip-flop to the low state. The

CA1 input is initialized to detect a positive transition.

Printer strobe signals P1 and P2 are pulses that request the thermal elements to be turned on to print dots. The P1 pulse is set low to request odd dots to be printed first. When P1 goes low, Z20-12 goes high causing a positive transition on CA1. CA1 is then reconfigured to interrupt a negative transition. The P1 is reset high before the P2 signal goes low to request even dots to be printed. Z20-12 is reset to low when P2 goes low. The CA1 input detects the positive to negative transition. This process is repeated during the print cycle.

7.2.7 Display Interface

The AIM 65 display consists of five four-digit 16 segment alphanumeric displays. Each display (DS1 - DS5) contains internal memory, decoder and driver circuitry. The displays interface with the AIM 65 address, data and control bus lines through the R6520 PIA (U1) mounted on the display module (see Figure 7-9). Each display is controlled by seven data lines (D0 - D6), two address lines (A0 and A1), two control lines ($\overline{W}$ and $\overline{CW}$) and a chip select ($\overline{CE}$).

There are five separate chip select lines ($\overline{CE1}$ - $\overline{CE5}$), one to drive each display.

Table 7-5 shows the display decode logic. To load data, $\overline{CE}$ is held low to the desired display. The desired data code (see Table 7-6) is placed on D0-D6 and the selected digit address (0-3) is placed on A0 and A1. The cursor line ($\overline{CU}$) is held in the high state. The write ($\overline{W}$) line is driven low to store and display the data. After W is returned to high, the data will continue to be displayed until replaced with new data or the cursor is displayed. Data entry may be asynchronous and random.

A display hardware cursor function may be displayed instead of an ASCII character. The cursor function causes all 16 segments of a character to turn on. The cursor is not a character, however, and upon removal the last stored displayed character is restored. The cursor is displayed when $\overline{CU}$ is low while $\overline{W}$ is low and any of the D0-D3 lines are high. The cursor will be displayed in digits 0-3 for each D0-D3 line that is high, respectively (see Table 7-7).

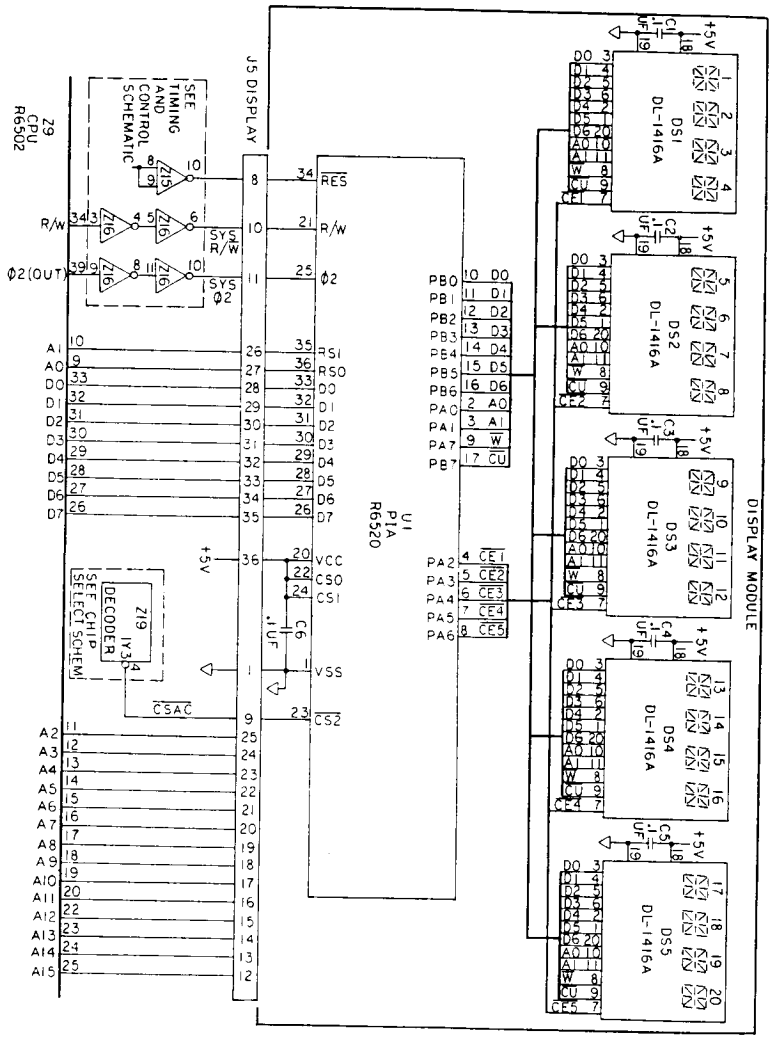

Figure 7-9. Display Interface Schematic

Table 7-5. Display Decode Logic

DISPLAY INPUTS																DISPLAY OUTPUTS																			
$\overline{W}$	$\overline{CE5}$	$\overline{CE4}$	$\overline{CE3}$	$\overline{CE2}$	$\overline{CE1}$	A1	A0	$\overline{CU}$*	D6	D5	D4	D3	D2	D1	D0	DS1				DS2				DS3				DS4				DS5			
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
																1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
L	H	H	H	H	L	L	L	H								N	N	N	T	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
L	H	H	H	H	L	L	H	H								N	N	T	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
L	H	H	H	H	L	H	L	H								N	T	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
L	H	H	H	H	L	H	H	H								T	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
L	H	H	H	L	H	L	L	H								N	N	N	N	N	N	N	T	N	N	N	N	N	N	N	N	N	N	N	N
L	H	H	H	L	H	L	H	H								N	N	N	N	N	N	T	N	N	N	N	N	N	N	N	N	N	N	N	N
L	H	H	H	L	H	H	L	H								N	N	N	N	N	T	N	N	N	N	N	N	N	N	N	N	N	N	N	N
L	H	H	H	L	H	H	H	H								N	N	N	N	T	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
L	H	H	L	H	H	L	L	H	Refer to Character Set in Table 7-6							N	N	N	N	N	N	N	N	N	N	N	T	N	N	N	N	N	N	N	N
L	H	H	L	H	H	L	H	H								N	N	N	N	N	N	N	N	N	N	T	N	N	N	N	N	N	N	N	N
L	H	H	L	H	H	H	L	H								N	N	N	N	N	N	N	N	N	T	N	N	N	N	N	N	N	N	N	N
L	H	H	L	H	H	H	H	H								N	N	N	N	N	N	N	N	T	N	N	N	N	N	N	N	N	N	N	N
L	H	L	H	H	H	L	L	H								N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	T	N	N	N	N
L	H	L	H	H	H	L	H	H								N	N	N	N	N	N	N	N	N	N	N	N	N	N	T	N	N	N	N	N
L	H	L	H	H	H	H	L	H								N	N	N	N	N	N	N	N	N	N	N	N	N	T	N	N	N	N	N	N
L	H	L	H	H	H	H	H	H								N	N	N	N	N	N	N	N	N	N	N	N	T	N	N	N	N	N	N	N
L	L	H	H	H	H	L	L	H								N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	T
L	L	H	H	H	H	L	H	H								N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	T	N
L	L	H	H	H	H	H	L	H								N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	T	N	N
L	L	H	H	H	H	H	H	H								N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	T	N	N	N

*Note: If CU is low and W is low the cursor symbol (*) will be displayed in the digit rather than the character set symbol shown in Table 7-6.

T = Refer to Table 7-6, Display Character Set

N = No change from previous display

Table 7-6. Display Figure Set

CHARACTER SET

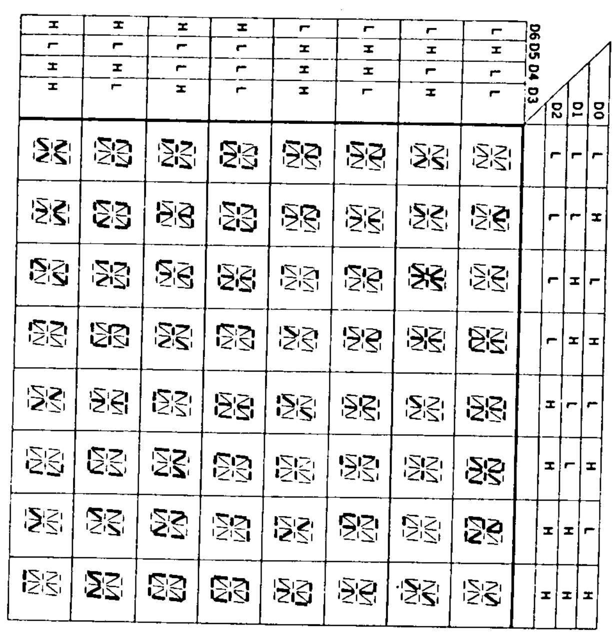

Table 7-7. Display Data/Cursor Loading

LOADING DATA

$\overline{CE}$	$\overline{CU}$	$\overline{W}$	ADDRESS A_1	A_0	DATA INPUT D6	D5	D4	D3	D2	D1	D0	DIGIT 3	DIGIT 2	DIGIT 1	DIGIT 0
H	X	X	X	X	X	X	X	X	X	X	X	NO CHANGE	NO CHANGE	NO CHANGE	NO CHANGE
L	H	L	L	L	H	L	L	L	L	L	H	NO CHANGE	NO CHANGE	NO CHANGE	A
L	H	L	L	H	H	L	L	L	L	H	L	NO CHANGE	NO CHANGE	B	A
L	H	L	H	L	H	L	L	L	L	H	H	NO CHANGE	C	B	A
L	H	L	H	H	H	L	L	L	H	L	L	D	C	B	A
L	H	L	L	L	H	L	L	L	H	L	H	D	C	B	E
L	H	L	H	L	H	L	L	H	L	H	H	D	K	B	E
L	H	L	—	—	—	—	—	—	—	—	—	SEE CHARACTER SET			

X = DON'T CARE

LOADING CURSOR

$\overline{CE}$	$\overline{CU}$	$\overline{W}$	ADDRESS A_1	A_0	DATA INPUT D6	D5	D4	D3	D2	D1	D0	DIGIT 3	DIGIT 2	DIGIT 1	DIGIT 0
H	X	X	X	X	X	X	X	X	X	X	X	D	K	B	E
L	L	L	X	X	X	X	X	L	L	L	H	D	K	B	▣
L	L	L	X	X	X	X	X	L	L	L	L	D	K	B	E
L	L	L	X	X	X	X	X	L	L	H	L	D	K	▣	E
L	L	L	X	X	X	X	X	L	H	L	L	D	▣	B	E
L	L	L	X	X	X	X	X	H	L	L	L	▣	K	B	E
L	L	L	X	X	X	X	X	H	H	H	H	▣	▣	▣	▣
L	L	L	X	X	X	X	X	L	L	L	L	D	K	B	E

X = DON'T CARE

7.2.8 Keyboard Interface

The interface to the AIM 65 keyboard is through the R6532 RIOT (see Figure 7-10). Z33 R6532 peripheral I/O lines PA0 through PA7 are assigned to keyboard input lines K11 through K18, respectively. R6532 lines PB0 through PB7 are wired to the keyboard output lines K01 through K08, respectively.

When scanning for key depression, a logic 0 is placed in the R6532 Output Register A (ORA) in one bit position at a time corresponding to one KI line. The logic 0 provides a low output to the KI line key switches. Each key depressed of the switches connected to selected KI line will present a closed circuit output from KO1-KO8 causing a logic 0 to be present in the respective bit position of R6532 Output Register B (ORB). Each unpressed key presents an open input circuit to PB0-PB7 causing a logic 1 to be present in the respective R6532 ORB bit position.

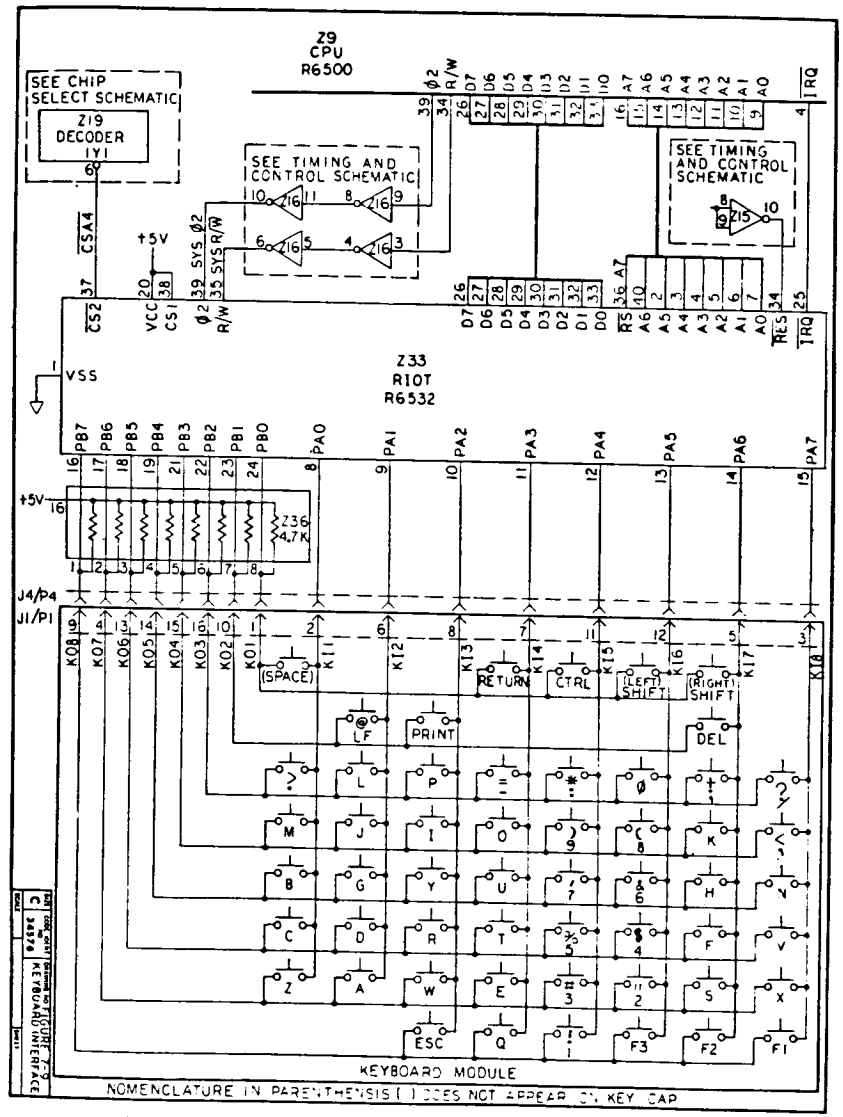

Figure 7-10. Keyboard Interface Schematic

7.2.9 User R6522 Interface

The User R6522 VIA (Z1) interface with the J1 Application Connector is shown in Figure 7-11. The total resources of the R6522 are available for user defined applications. Refer to the R6500 Hardware Manual for a full discussion of R6522 capabilities and application instructions.

The R6522 internal registers are accessible when CS1 is high and $\overline{CS2}$ is low. Since CS1 is wired high to +5V and $\overline{CS2}$ is connected to the chip-select output $\overline{CSA0}$, Z1 is enabled whenever the address is between A000 to A3FF (see Table 7-1). Also, because the Z1 RS0 to RS3 lines are connected to address lines A0 to A3, Z1 will respond to all addresses in the A000-A3FF range. The primary memory map for Z1 is A000-A00F (see Tables 7-9 and 7-10) so these addresses should be used and the addresses between A010 and A3FF avoided.

The Z1 $\overline{IRQ}$ output lines is connected to the Z9 R6502 CPU $\overline{IRQ}$ input for user definition and application. See Section 7.8 for a description of the AIM 65 Monitor IRQ interrupt linkage and handling.

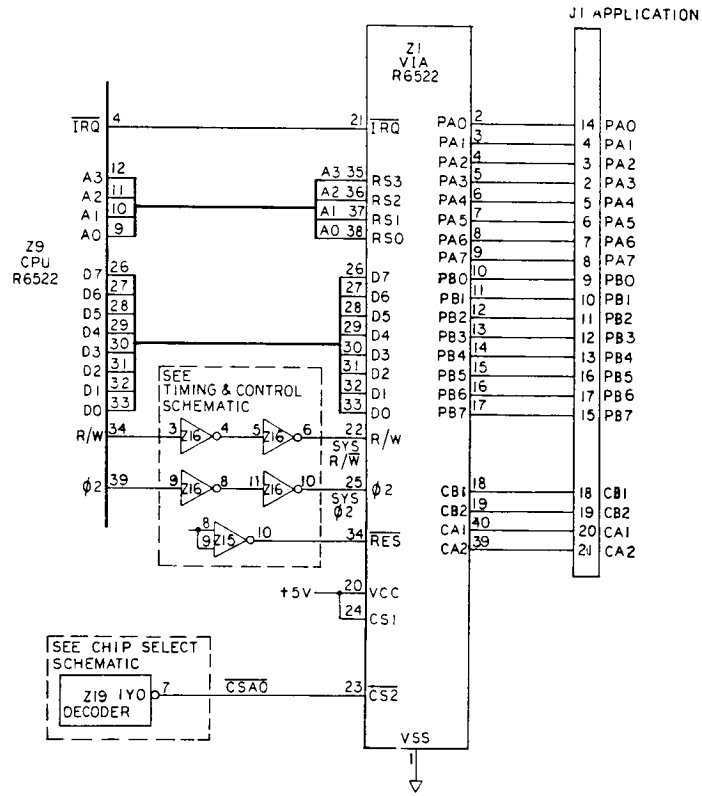

Figure 7-11. User R6522 Interface Schematic

7.2.10 Audio Cassette Recorder Interface

The AIM 65 audio cassette recorder interface provides audio data routing control and waveform shaping as well as recorder remote control circuitry. (See Figure 7-12.).

CA2 operates as a discrete output to control the audio data direction. When CA2 output is set high (logic 1), the audio input data from J1-L (AUDIO IN) is enabled through gate Z5-11 to PB-7, which is configured as an input. Z8 and associated circuitry provides AC coupling and input data compensation and shaping. Note that the audio input data output from Z5-11 is routed back through Z5-8 to J1-P (AUDIO OUT HI) and J1-M (AUDIO OUT LOW).

To output audio data from AIM 65, CA2 output is reset low by logic 0 to gate Z5-11 to inhibit any audio input data or noise from mixing with the audio output data. PB-7 is configured to operate as an output. Audio output data from PB-7 is routed to J1-P (AUDIO OUT HI) and J1-M (AUDIO OUT LO). AC coupling and waveform shaping is performed.

The audio data circuitry supports both AIM 65 and KIM-1 recording formats. The AIM 65 format is described in Appendix F, the KIM-1 format is described in Appendix G.

PB4 and PB5 are outputs that drive the audio cassette recorder remote control circuits. A logic 0 (PB4/PB5 low) turns Q6/Q7 off causing an open circuit in the recorder remote line thereby stopping motor. A logic 1 (PB4/PB5 high) turns Q6/Q7 on causing a closed circuit in the recorder remote line thereby allowing the motor to operate.

Four types of recorder motor remote control circuits are supported. Refer to Section 9.1.1 for a description of the recorder remote control wiring and recorder installation.

In the recorder remote control type PRC and PRS circuits, PB4 opens and closes the recorder No. 1 remote circuit from J1-W (motor low) to GND through Z21-12, while PB5 control recorder No. 2 power circuit from J1-V to GND through Z21-13. The AIM 65 GND must be connected to the record GND through J1-1.

In the type PVC and PVS circuits, PB4 opens and closes the recorder No. 1 remote circuit from J1-F (motor positive voltage supply) to J1-E (motor high) through Q6. PB5 controls the recorder No. 2 remote circuit from J1-J to J1-H through Q7.

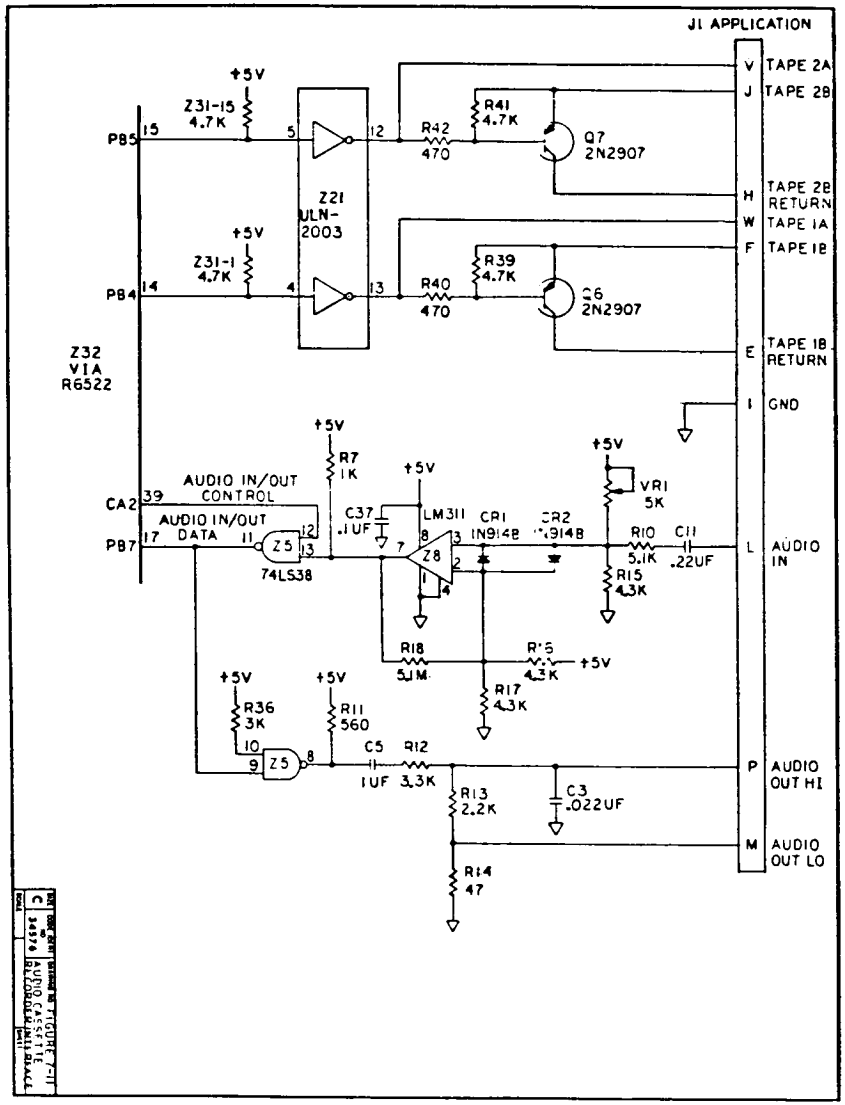

Figure 7-12. Audio Cassette Recorder Interface Schematic

7.2.11 TTY and Serial Interface

AIM 65 provides a 20 MA current loop, full duplex interface with a teleprinter or teletype (TTY). A serial input capability is also included (see Figure 7-13). Refer to Section 9.2 for the TTY installation instructions.

The current source for the TTY printer is provided at J1-S (TTY PTR RTN (+)) from the AIM 65 +5V power supply as limited by R1. The output to the TTY printer originates from PB2, which is configured as an output. The output signal is inverted by permanently enabled gate Z5-3. CR7 clamps the output to GND so only a positive pulse stream is presented to the TTY printer on J1-U (TTY PTR).

The current source for the TTY keyboard is provided at J1-R, TTY KYBD RTN (+), from the AIM 65 +24V power supply as limited by R25. The TTY keyboard input received on J1-T (TTY KYBD) is shaped by Q2 and associated components. The signal is then inverted through permanently enabled gate Z5-6 to the R6522 I/O pin PB6, which is configured as an input.

The ability to input a serial bit stream on J1-Y may be used instead of the TTY keyboard input. The bit transmission rate may be as high as 9600 baud.

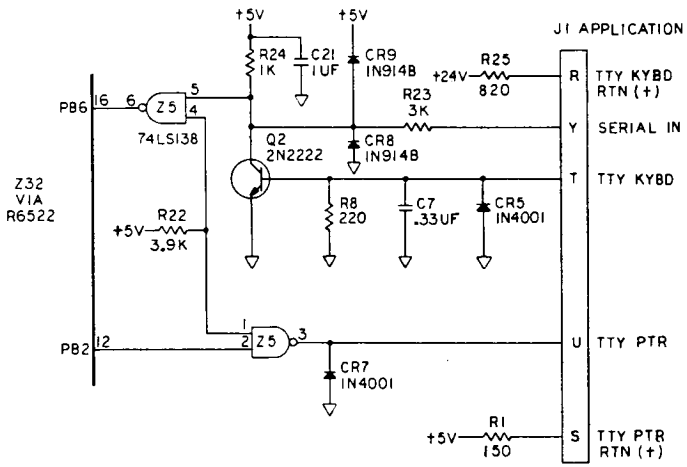

Figure 7-13. TTY and Serial Interface Schematic

7.3 AIM 65 SOFTWARE

The AIM 65 software consists of:

- The AIM 65 8K Monitor (including the Text Editor)
- The Optional AIM 65 4K Assembler
- The Optional AIM 65 8K BASIC

7.3.1 AIM 65 Monitor

The AIM 65 Monitor software provides the overall control of the AIM 65 peripheral devices (except the Z1 user R6522), the control and sequencing of AIM 65 commands and linkage to user functions. Figure 7-13 is a top level flowchart of the Monitor interrupt and command mode processing.

AIM 65 MONITOR ENTRY DUE TO RESET INTERRUPT

The Monitor is initially entered via the RST Interrupt Vector either due to AIM 65 power turn-on or pressing the RESET button. The R6502 decimal mode is cleared and the IRQ interrupt is disabled. The start pointer is initialized to $01FF as is the user saved stack pointer.

The AIM 65 peripheral devices used by the Monitor, i.e., R6522 (Z32), R6532 (Z33), and the R6520 (U1) are initialized to set up the data direction registers, load constant data and establish counter/interrupt modes (if applicable).

The variables required for AIM 65 Monitor operation are initialized. If address $A402 is not $7B or if $A403 is not $E0 (the AIM 65 NMI interrupt vector) "cold" reset

variables are initialized. During a "cold" reset, the parameters listed in Table 7-8 are initialized to the stated values. Otherwise, a "warm" reset is performed which initializes only the variables required for AIM 65 Monitor initialization.

If the KB/TTY switch is in the TTY position, the Monitor waits until RUBOUT is typed on the TTY keyboard. The Monitor then measures the TTY to AIM 65 bit transmission rate and stores the value in address $A417 (CNTH30) and $A418 (CNTL30).

The ROCKWELL AIM 65 message is displayed/printed to indicate that AIM 65 reset has been performed. The Monitor command mode is then entered.

AIM 65 MONITOR ENTRY DUE TO IRQ INTERRUPT

The Monitor IRQ Interrupt Processing may be entered due to a BRK instruction being executed. If a BRK instruction was the cause, AIM 65 displays the register contents, disassembles and displays the next instruction and enters the Monitor and Software Command Mode. See Section 7.8 for user IRQ interrupt linkage and the R6500 Hardware Manuals for additional IRQ processing considerations.

AIM 65 MONITOR ENTRY DUE TO NMI INTERRUPT

The Monitor NMI Interrupt Routine may be entered due to execution of an instruction outside the $A000-$FFFF address range while in STEP Mode (RUN/STEP switch in the STEP position). If this is the cause and either an enabled

breakpoint address is encountered (see Monitor B command) or the instruction execution termination criteria is satisfied (see Monitor G command), the register contents are displayed, the next instruction disassembled, and the Monitor Command Mode is entered. See Section 7.8 for User NMI interrupt linkage information and the R6500 Hardware and Software Manuals for additional NMI interrupt processing considerations.

AIM 65 MONITOR COMMAND MODE

The Monitor Command Mode initially displays the Monitor prompt "<" to indicate that a Monitor command may be typed. Upon receipt of a typed command, the typed character is displayed along with the command closing ">" character. If the command is not valid, "?" is displayed and the command mode re-entered. If the command is valid, the Monitor calls the command subroutine. The command subroutine executes an RTS instruction to return to the Monitor upon the completion of command processing. The Monitor then re-enters the command mode.

7.3.2 AIM 65 Memory Map

Table 7-9 shows the overall AIM 65 memory map. The input/output portion is further defined in Table 7-10. A complete detailed memory map is listed in Table 7-11.

7.4 USER DEFINED FUNCTIONS LINKAGE

Three user-defined functions may be entered by typing the F1, F2, and F3 keys. Typing one of the user function

keys causes the Monitor to jump to the AIM 65 RAM locations assigned to the first instruction in the user function. That address in turn should be loaded with a three byte JMP instruction to the rest of the user function instructions for that function located in user RAM.

CAUTION

Typing F1, F2, or F3 prior to loading a JMP instruction in the appropriate address may cause AIM 65 to hangup or to operate incorrectly. Press RESET to recover.

LABEL	ADDRESS	DESCRIPTION
KEYF1	$010C	JMP Instruction to Function 1
KEYF2	$010F	JMP Instruction to Function 2
KEYF3	$0112	JMP Instruction to Function 3

7.5 USER DEFINED INPUT/OUTPUT FUNCTION

The input (IN=) and output (OUT=) prompts allow a U to be typed to specify a user-defined I/O function. The Monitor indirectly calls the function pointed to by the user I/O handler vectors:

LABEL	ADDRESS	BYTES	DESCRIPTION
UIN	$0108	2	Vector to User Input Handler
UOUT	$010A	2	Vector to User Output Handler

USER INPUT HANDLER

The user input handler is usually called by the Monitor or a user program from the WHEREI and INALL subroutines. WHEREI is first called and asks for the input device code, i.e., IN= . In response to the typed U, WHEREI clears the carry bit in the processor status register to indicate initial entry into the user input function.

The input function should test the carry bit and conditionally branch on carry clear to input device initialization. Upon completion of input device initialization, the input function should return to the calling program. The calling program should make subsequent calls to the user input function from the INALL subroutine which first sets the carry bit. The user input function should perform the normal input processing on carry bit set.

Example:

Calling Routine

```
JSR WHEREI
JSR INALL
```

User Input Function

```
UIN .WOR INTST  (Vector to input handler subroutine)
INTST           BCC IPINIT
                :
                Perform Input Processing
                :
                RTS
```

```
        IPINIT          Perform Input Initialization
                        :
                        RTS
```

USER OUTPUT HANDLER

The user output handler is usually called by the Monitor or a user program from the WHEREO and OUTALL subroutines. WHEREO is first called and asks for the output device code, i.e., OUT= . In response to the typed U, WHEREO clears the carry bit in the processor status register to indicate initial entry into the user output function. The output function should test the carry bit and conditionally branch on carry clear to output device initialization, if required. Upon completion of output device initialization, the output function should return to the calling program. The calling program should subsequently call the user program using the OUTALL subroutine which first sets the carry bit. The user output function test should perform normal output processing on carry bit set.

Example:

Calling Routine

```
        JSR WHEREO
        JSR OUTALL
        :
        .
```

User Output Function

```
        WOUT .WOR OUTTST    (Vector to output handler subroutine)
```



```
OUTTST BCC OTINIT
        :
        Perform Output Processing
        :
        RTS
OTINIT Perform Output Initialization
        :
        RTS
```

Table 7-8. Parameters Initialized by "Cold" Reset

ADDRESS	LABEL	BYTES	VALUE	DESCRIPTION
A402	NMIV2	2	$7BEO	Vector to $E07B (NMIV3) Monitor NMI Interrupt Processing
A404	IRQV2	2	$54E1	Vector to $E154 (IRQV3) - Monitor IRQ Interrupt Processing
A406	DILINK	2	$05EF	Vector to $EF05 (OUTDIS) - Echo Input to AIM 65 Display
A408	TSPEED	1	$C7	$C7 = AIM 65 Format -
A409	GAP	1	$08	$08 = 32 SYN Characters

Table 7-8. Parameters Initialized by "Cold" Reset (Cont.)

ADDRESS	LABEL	BYTES	VALUE	DESCRIPTION
A40A	NPUL	1	$02	
A40B	TIMG	3	$CA038D	
A40E	REGF	1	$00	Turn Register Trace Off
A40F	DISFLG	1	$00	Turn Instruction Trace Off
A410	BKFLG	1	$00	Breakpoint Enable Off
A411	PRIFLG	1	$80	Turn Printer On

Table 7-9. AIM 65 System Memory Map