AMPRO
COMPUTERS, INCORPORATED

LITTLE BOARD/186

TECHNICAL MANUAL

P/N: A74011-C

****** NOTE: THIS MANUAL IS A REDUCED REPRODUCTION. APPENDIX D (COMPONENT DATA SHEETS) HAS BEEN OMITTED. ******

67 East Evelyn Ave. • Mountain View, CA 94041 • (415) 962-0230

PREFACE

This manual is for integrators of systems based on the AMPRO Little Board/186 single board computer. It contains information on hardware requirements and interconnection, and details of how to use the system. There are five chapters, organized as follows:

Chapter 1 — INTRODUCTION - General information pertaining to the Little Board/186, its major features, and a brief functional description.

Chapter 2 — INTEGRATING A SYSTEM - Descriptions of the external components necessary to construct systems based on the Little Board/186 with floppy and hard disk drives. Included are tables listing the pinouts of each of the board's connectors, as well as special considerations and specifications concerning peripheral devices.

Chapter 3 — OPERATION WITH PC-DOS - Discussion of PC and PC-DOS compatibility. Information on system customization options, including use with various types of printers, modems, and floppy and hard disk configurations. Also includes brief descriptions of the AMPRO-specific DOS utilities and drivers.

Chapter 4 — THEORY OF OPERATION - Detailed technical information on Little Board/186 hardware.

Chapter 5 — PROGRAMMERS' REFERENCE - Port addresses and other programming considerations for custom programming of Little Board/186, including information pertaining to use of the ROM-BIOS.

PLEASE NOTE

Specifications are subject to change without notice. The contents of this document are believed to be accurate. If errors are found, please notify AMPRO at the address shown on the title page of this document.

The following is a list of trademarks used within this document:

IBM: International Business Machines
MS-DOS: Microsoft Corp.
LOTUS 1-2-3: Lotus Development Corp.
LITTLE BOARD, LITTLE BOARD/186, SCSI/PLUS: AMPRO Computers, Inc.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The Little Board/186 is a compact, high performance 16-bit, PC-DOS based single board computer capable of replacing an entire computer system in many embedded microcomputer applications.

Included on the 5.75 X 7.75 inch SBC are an 8 mHz 80186 16-bit CPU, 512K bytes of RAM memory, 16K to 128K bytes of EPROM memory, two RS232C serial ports, a Centronics printer port, a floppy disk controller, and a multi-master SCSI I/O expansion bus. The SCSI bus serves multiple functions, including interface to hard disk controllers, inter-board networking, and I/O port expansion.

Typical Little Board/186 applications include network file servers, robotics, data logging, protocol conversion, data base processing, point-of-sale terminals, telecommunications, and industrial process control. In such applications, the board's 8 MHz 80186 16-bit microprocessor provides up to a four-fold performance advantage over the 4.77 MHz 8088 CPU found in standard PC's.

AMPRO's proprietary ROM-BIOS (included on the board) allows the Little Board/186 to directly "boot" and run standard IBM DOS versions 2.x and DOS 3.x, using a standard ASCII terminal connected to one of the board's serial ports as the console (keyboard and display) device. "MS-DOS generic" software normally runs without modification in this environment. However, IBM PC video compatibility (e.g. programs which write directly to "video RAM") is not supported, except by means of the Video RAM Emulator option (described below).

1.2 FEATURES

- Boots and runs IBM PC-DOS 2.x and 3.x
  - Data and file compatible with IBM PC
  - Runs "MS-DOS generic" programs
- 3X the computing power of a PC
- Mounts directly to a 5-1/4" disk drive
- Uses less than 7 watts of power
- Complete 16-bit high performance Single-Board Computer System:
  - 8 MHz 80186 CPU with DMA and counter/timers
  - 512K RAM (0 wait states) -- 16K-128K EPROM
  - Mini/Micro Floppy controller (4 drives, DSDD, 40/80 track)
  - 2 RS232C Serial Ports -- 1 Centronics Printer Port
  - PC-DOS 2.x and 3.x compatible ROM-BIOS
- SCSI (SASI) Multi-Master I/O Expansion BUS:
  - SASI Disk/Tape Controller Compatible
  - ANSC X3T9.2 (SCSI) Compatible
  - Multiple Little Board Networking
- Expansion options include:
  - Video RAM Emulator
  - Multi-Function Expansion Adapter (RAM, 8087, clock, RS232/422)
  - Prototype Adapter
  - SCSI/IOP (data acquisition & control interface)

1.3 SCSI/PLUS (tm) Multi-Master Bus

A 50-pin "ribbon cable bus" interface which meets the specifications for the popular Small Computer System Interface (SCSI) -- formerly called "SASI" -- provides a general purpose multi-master I/O expansion bus. All SCSI Initiator and Target functions are fully supported, including bus arbitration and disconnect/reselect.

AMPRO is a leading proponent of the use of SCSI for more than mass storage. To emphasize this wider use of SCSI, we have given it a name: "SCSI/PLUS". An SCSI/PLUS Architecture Overview appears in Appendix A.

Applications for the board's SCSI/PLUS bus include both direct and shared use of a wide variety of controllers and devices, as well as tightly coupled Little Board networks. Devices soon to be available for connection via the SCSI/PLUS Bus include:

- Disk, tape, and optical mass storage subsystems
- Special function mass storage (RAM disk, bubble memory, etc.)
- Printer subsystems (serial, parallel, laser, etc.)
- Communication and LAN interfaces (Ethernet, X.25, etc.)
- Real time clock
- Co-processors
- Data acquisition and control subsystems (Analog, Digital, etc.)
- Graphics controllers and subsystems
- Non-volatile RAM
- etc...

Alternatively, the 17 bidirectional I/O signals of the board's SCSI/PLUS interface may also be used as general purpose software-controlled digital I/O lines, without SCSI compatibility. In this case, the board's 8-bit SCSI bus ID input register can serve as an additional 8-bit input port.

1.4 OTHER EXPANSION OPTIONS

Several expansion options are available for use with the Little Board/186, including:

1.4.1 Video RAM Emulator

The Video RAM Emulator allows the use of software which writes directly to "video RAM" instead of making PC-DOS or ROM-BIOS function calls. Such software would otherwise require modification for use with the Little Board/186.

The Video RAM Emulator is a 5.75 X 7.75 inch daughter board which plugs into the CPU header on the Little Board/186. It can not be used in conjunction with any of the other daughter board options.

1.4.2 Multi-Function Expansion Adapter

A Multi-Function Expansion Adapter (EXPANSION/186) is available for the Little Board/186 which provides five key system options:

- 512K additional zero-wait-state DRAM.
- 8087 math coprocessor (400% the speed of an 80287)
- Two additional sync/async serial ports, with choice of RS232C, RS422, or external drivers and receivers.
- Battery-Backed Real Time Clock
- Buffered I/O bus (128 I/O locations)

The Multi-Function Expansion Adapter is a daughter board, identical in dimensions with the Little Board/186 (5.75 X 7.75), and plugs into the CPU header on the main board. It cannot be used in conjunction with any other daughter board options.

1.4.3 Prototype Adapter

Provides a user-determined general purpose I/O and memory expansion interface for the Little Board/186. Approximately 18 square inches of wire wrap space, along with pre-decoding and conditioning of 80186 signals, facilitate custom projects and product prototypes based on the Little Board/186. Especially useful in such applications as data acquisition, process control, test instrumentation, product demonstration, SCSI special function devices, etc.

The Prototype Adapter is a daughter board, identical in dimensions with the Little Board/186 (5.75 X 7.75), and plugs into the CPU header on the main board. It cannot be used in conjunction with any other daughter board options.

1.4.4 SCSI/IOP

The AMPRO SCSI/IOP is an intelligent I/O processor (IOP) which allows the addition of a wide variety of off-the-shelf STD Bus data acquisition and control interfaces to a Little Board/186. It connects via a 50-conductor flat ribbon cable plugged into the SCSI/PLUS bus connector on the Little Board/186, and does not preclude the use of any of the optional daughter boards.

The SCSI/IOP can also be used as a non-volatile RAM storage device (up to 48K bytes), as a system boot device (EPROM-Based), and as an SCSI Real Time Clock.

1.5 SPECIFICATIONS

CPU/DMA/CTC

- 8 MHz 80186

MEMORY

- 512K bytes zero wait state DRAM
- Two 28-pin sockets for 2764-27512 (16K to 128K)

SERIAL I/O

- Two RS232C compatible ports
- Based on Signetics 2681 dual UART
- Software controlled baud rates, 50-38.4K baud
- Four signals per port: data in/out, status in/out

PARALLEL I/O

- Centronics compatible printer port
- 8-bit ID input port

FLOPPY DISK INTERFACE

- Mini and micro floppy compatible
- 1 to 4 drives, single/double density, 40/80 tracks, 1-2 sided
- 125 or 250 Kbits/second data rate
- Highly reliable digital phase-locked loop
- Software enabled write precompensation

SCSI/PLUS INTERFACE

- SASI compatible
- Full ANSC X3T9.2 (SCSI) compatible (all modes)
- Based on NCR 5380 SCSI bus controller
- Usable as 17 bidirectional I/O lines (48 mA sink)
- Max. SCSI throughput: 1 Mbyte/sec (read)
  .75 Mbyte/sec (write)

POWER

- Same power connector and voltages as mini and micro floppy drives
- +5V at 1.25 A.(typ.), +9V to +15V at .05 A.(typ)
- On-board -12 VDC converter

ENVIRONMENT

- Operating temperature: 0-55 degrees Centigrade
- Relative Humidity: 5-95% (non-condensing)
- Altitude: 0 to 10,000 feet

PHYSICAL

- 7.75 x 5.75 x 0.75 inches (5-1/4 disk drive form factor)

SOFTWARE

- AMPRO ROM-BIOS (boots PC-DOS 2.x or 3.x) in two 2764s
- PC-DOS Support Software
- Optional debugger/monitor program in two 2764s

DOCUMENTATION

- Little Board/186 Technical Manual
- PC-DOS Support Software User's Manual
- Optional: 5380 Technical Manual
  SCSI/PLUS Technical Specification

CHAPTER 2

INTEGRATING A SYSTEM

2.1 INTRODUCTION

This chapter describes what is required to build a floppy- or hard disk-based computer system using the Little Board/186. Details are provided concerning external device requirements, the board's connector pinouts, and how to prepare the board for use with periperals such as terminals, printers, and modems.

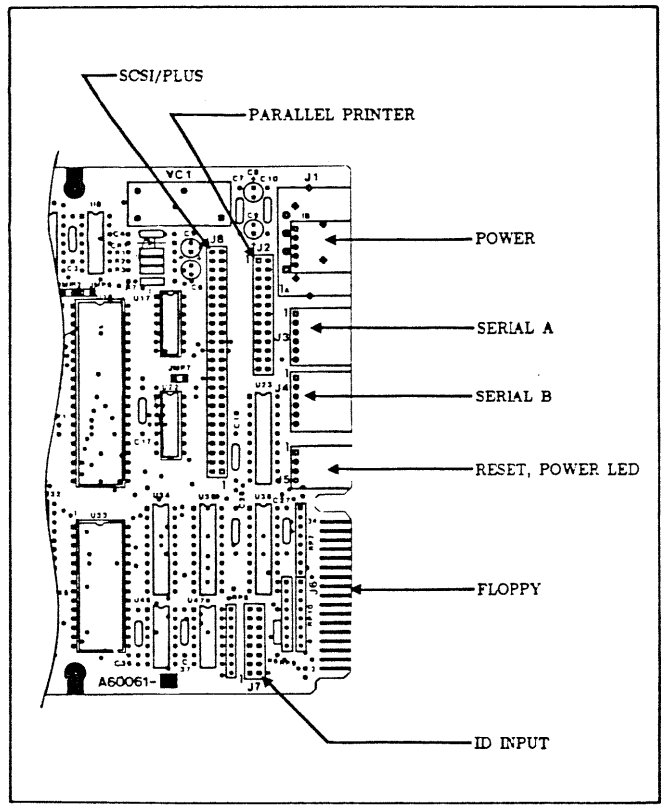

Figure 2-1. Little Board/186 Connector Locations.

2.2 BASIC REQUIREMENTS

The Little Board/186 is designed to use a standard RS232C ASCII terminal as a console device, providing both keyboard and display. You may use nearly any such terminal, providing its control codes are supported by your applications software.

The ROM-BIOS included on Little Board/186 allows you to use standard IBM PC-DOS versions 2.x or 3.x as the board's operating system. The utilities and drivers supplied on the AMPRO Little Board/186 PC-DOS Support Software diskette allow operation with 40-track, 80-track, single- or double-sided mini and micro floppy disk drives -- in various combinations -- and support a wide variety of SCSI hard disk controllers and drives. PC-DOS version 3 is required for hard disk systems; version 3.2 (or later) is required if full 80-track support is desired.

Centronics type parallel printers, and most RS232-compatible serial printers and modems may be directly connected to Little Board/186's I/O interface connectors.

2.3 SYSTEM CONNECTIONS

Figure 2-1 shows the board's external I/O connectors. The following paragraphs describe each connector interface and indicate special requirements for external devices. Mating connectors for the seven I/O interface connectors on the Little Board/186 are in Table A-4 of Appendix A.

2.3.1 DC Power Input

The power connector (J1) pinout is identical with that of power connectors on nearly all 5-1/4 inch floppy disk drives. Note that pin 1 on J1 is reversed from the other connectors on the Little Board/186. Refer to Table 2-1 for power connections, and Figure 2-2 for typical connector wiring.

CAUTION

Be sure the power plug is correctly wired before applying power to the board.

Table 2-1. Power Connections (J1)

Pin	Signal Name	Function
1	+12VDC	+6 to + 15VDC
2	Ground	Ground return
3	Ground	Ground return
4	+5VDC	+5VDC +/- 5%

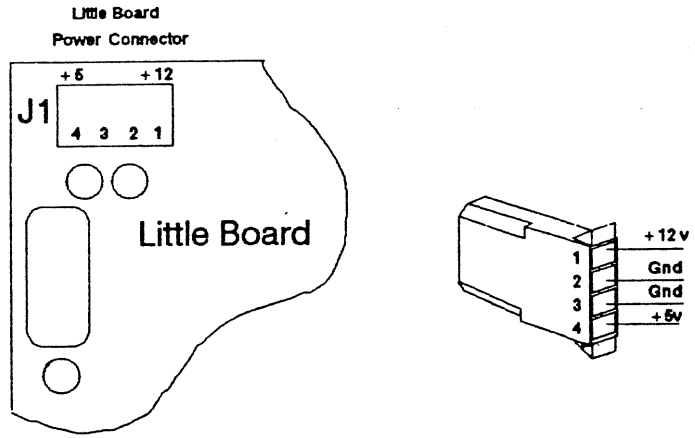

Figure 2-2. Power Connector Wiring

2.3.2 RESET, Power LED

J5 provides connection for an external s.p.s.t normally open switch to provide a manual RESET signal. In addition, a 15 mA current source provides power for an LED power-on indicator. Refer to Table 2-2 for the pinout of connector J5.

Table 2-2. RESET, Power LED Connector (J5)

Pin	Signal Name	Function
1	Ground	To LED Cathode
2	LED	To LED Anode
3	Ground	To one side of RESET switch
4	RESET	To other side of RESET switch

2.3.3 Serial Ports

Table 2-3 gives the connector pinout and signal definitions for each of the two RS232C serial ports. Serial Port A is board connector J3, and Serial Port B is board connector J4. Appendix B gives typical cable wiring for connection to terminals, serial printers, and modems.

Table 2-3. Serial Connectors (J3/J4)

Pin	Signal Name	Function	in/out	DB-25 Pin (DCE)
1	Ground	Protective Ground	--	1
2	Ground	Signal Ground	--	7
3	TxD	Data Output	out	3
4	HSO	Hand Shake Out (RTS)	out	5
5	RxD	Data Input	in	2
6	HSI	Hand Shake In (CTS)	in	20

The default ROM-BIOS "console" interface is Serial Port A. To this port you may connect nearly any type of RS232C ASCII terminal to provide monitor and keyboard functions. Asynchronous baud rates up to 38.4 Kbits per second may be utilized.

Some terminals require hardware handshaking when used at baud rates in excess of 9600. If hardware handshaking is needed, connect the terminal's CLEAR TO SEND output to the board's HANDSHAKE IN signal. Each port's HANDSHAKE OUT signal can optionally be used to stop external devices from transmitting data to the board. (The AMPRO SETCON.SYS software driver is used to enable this feature.)

Serial Port B can be used for connection of a printer, modem, or other serial device. As with port A, the main interface consideration is that the device be RS232C ASCII compatible. Printers and modems generally require handshaking in one or both directions.

2.3.4 Parallel Printer Port

The parallel printer connector, J2, has a pinout that allows the use of flat ribbon cable between the J2 header and the first 26 lines of a 36 pin male Centronics type connector at the printer end. Note that the pin numbering for the printer's interface connector differs from that of the header connector on the board. J2 is numbered as shown in Figure 2-1. Although some printers may include unique signals not shown, the signals provided by J2 are adequate for normal operation of most printers.

Refer to Table 2-4 for printer connector signal pinouts and definitions. Note that the pin numbering convention for the board's header connector differs from that of Centronics connectors. To clarify this, each signal's corresponding Centronics connector pin number has been included in Table 2-4.

Table 2-4. Parallel Printer Connector (J2)

J2 Pin	Signal Name	Function	in/out	Centronics Conn. pin
1	-DS	Sample input data	out	1
3	Data 1	LSB of printer data	out	2
5	Data 2	:	out	3
7	Data 3	:	out	4
9	Data 4	:	out	5
11	Data 5	:	out	6
13	Data 6	:	out	7
15	Data 7	:	out	8
17	Data 8	MSB of printer data	out	9
19	-ACK	Character accepted	in	10
21	BUSY	Cannot receive data	in	11
23	PAPER END	Out of paper	in	12
25	SELECT	Ready to receive data	in	13
2-22	GROUND	Signal grounds	--	19-29
24	---	(Not used)	--	30
26	-INIT	Initialize controller	out	31

The cable required is identical to that used with the Tandy (Radio Shack) TRS-80 Model 100 portable computer. The Tandy cable part number is 26-1409.

2.3.5 Floppy Disk Interface

Table 2-5 lists the floppy disk drive interface connector (J6) pinout and signals. A single 34-conductor PC edgecard connector is used at the Little Board end, while there can be from 1 to 4 connectors for connecting the disk drives.

Table 2-5. Floppy Disk Interface Connector (J6)

Pin	Signal Name	Function	in/out
2	-LOW SPEED	Speed select (option)	out
4	---	(Not used)	--
6	-DRIVE DEL 4	Drive Select 4	out
8	-INDEX	Index pulse	in
10	-DRIVE SEL	Drive Select 1	out
12	-DRIVE SEL 2	Drive Select 2	out
14	-DRIVE SEL 3	Drive Select 3	out
16	-MOTOR ON	Motor on control	out
18	-DIR SEL	Direction select	out
20	-STEP	Step	out
22	-WRITE DATA	Write data	out
24	-WRITE GATE	Write gate control	out
26	-TRACK 00	Track 00	in
28	-WRITE PRT	Write protect	in
30	-READ DATA	Read data	in
32	-SIDE ONE	Side select	out
34	-READY	Drive ready	in
1-33	(all odd pins)	Signal grounds	--

Nearly any type of soft-sectored, single or double-sided, 40 or 80 track, mini or micro floppy disk drive is usable with the Little Board/186. Naturally, the higher the quality of the drives you use, the better your system's reliability. Here are some considerations:

- The drives used must be compatible with the AMPRO floppy disk interface (see Table 2-5), and must provide the Drive Ready signal.
- High quality, DC servo direct drive motor floppy disk drives are recommended.
- More than one type of floppy disk drive, up to four, can be present in the system, and in any mix.
- If you plan to "boot" a standard copy of PC-DOS, drive A must be a 48 tpi (40 track) 5-1/4 inch double-sided mini floppy drive. Drives B, C and D can be any other system-compatible drive. PC-DOS version 3.2 (or later) allows the creation of a 96-tpi (80 track) boot diskette, but a 48 tpi drive is required to initially load the system diskette as it is supplied by IBM.
- Each disk drive must be jumpered for a specific Drive Select value, 1 through 4. Consult your drive documentation.
- Resistive terminations should be installed only on the drive connected to the last interface cable connector (farthest from the computer).
- When using drives with a Head Load option, jumper the drive for "head load with motor on" rather than "head load with drive select."

2.3.6 SCSI/Plus Interface

The SCSI/Plus interface (J8) uses a 50-pin male header connector to interface with SCSI-compatible peripherals. Table 2-6 shows the signal names and pin numbers. Refer to your disk controller documentation, or the ANSI SCSI specification for information on the signal functions.

Table 2-6. SCSI Interface Connector (J8)

Pin	Signal	Function
1 - 49	(All odd pins)	Signal grounds
2	-DB0	Data Bit 0 (LSB)
4	-DB1	" " 1
6	-DB2	" " 2
8	-DB3	" " 3
10	-DB4	" " 4
12	-DB5	" " 5
14	-DB6	" " 6
16	-DB7	" " 7 (MSB)
18	-DBP	Data Parity
20,22,24	Ground	Signal Ground
25	---	(Not used)
26	TERMPWR	Termination +5VDC
28,30	Ground	Signal Ground
32	-ATN	Attention
34	Ground	Signal Ground
36	-BSY	Busy
38	-ACK	Transfer Acknowledge
40	-RST	Reset
42	-MSG	Message
44	-SEL	Select
46	-C/D	Control/Data
48	REQ	Transfer Request
50	-I/O	Data direction

This interface can serve a variety of purposes, including connection of hard disk controllers, tape controllers, printer and communications servers, etc. In addition, the interface signals may be used as direct input/output lines, allowing the connection of TTL-level controlled devices and sensors, etc. (The output signals are open collector drivers capable of sinking 48 mA, and may be enabled and disabled under software control.) On-board removable resistor networks provide bus termination.

NOTE

The on-board resistive termination networks (U17, U22) should be present on two, and only two, SCSI bus devices. Be sure that the board's SCSI bus is terminated in at least one place (generally on the board); a non-terminated SCSI bus may "hang" the system up due to indeterminate signal levels.

2.3.7 ID Input Port / Drive Quantity Jumpers

Eight pairs of jumper pins (J7) provide an ID Input Port, which are generally used by SCSI-related software to determine the board's SCSI bus ID for bus arbitration, and by the board's ROM-BIOS to determine the number of floppy drives connected to the system (see next section). If not required for these purposes, the ID Input Port can be used as a general purpose 8-bit input port connector, with a flat ribbon cable plugged onto J7.

2.4 BOARD JUMPER CONFIGURATIONS

The board contains nine sets of jumpers, which may be used to customize the board's operation. The jumper sets consist of either two or three pins, with pin 1 a square pad, and are outlined with white boxes on the component side of the board. The options available through these jumpers are described in the following paragraphs.

NOTE

For normal operation, no jumper setup is required, other than the possible use of J7 for SCSI address jumpering and floppy drive quantity setup.

Most factory jumper settings are made by means of traces on the bottom side of the board. One exception is JMP5 which is generally shorted by means of a shorting plug on the component side of the board.

J7 - ID Input Port / Drive Quantity Jumpers

This 16-pin header is normally used to set the board's SCSI bus address, and also to indicate the number of floppy disk drives to be used. The connector pins are numbered from 1 to 16, with odd pins opposite even. The pairs are designated: J7-1/2, J7-3/4, J7-5/6, J7-7/8, J7-9/10, J7-11/12, J7-13/14, J7-15/16. Two pairs are used to indicate to the ROM-BIOS how many floppy drives are connected to the system; three pairs designate the board's SCSI bus ID; the remaining three pairs are currently unused. Refer to Table 2-7 for jumper settings.

Table 2-7. ID Input Port (J7) Jumpering

Pairs 1/2 and 3/4: Used to initialize the AMPRO ROM-BIOS floppy drive quantity value. Programmed as follows:

No. of Drives	1/2	3/4
1	in	in
2	in	out
3	out	in
4	out	out

Pairs 5/6, 7/8, 9/10: Reserved additional ID bits for SCSI/PLUS 6-bit ID, future use.

Pairs 11/12, 13/14, 15/16: Sets the board's SCSI ID, as follows:

SCSI Bus ID	11/12	13/14	15/16
0	in	in	in
1	in	in	out
2	in	out	in
3	in	out	out
4	out	in	in
5	out	in	out
6	out	out	in
7	out	out	out

JMP1,2 - EPROM Type

These jumpers are used to program the board for various types of EPROM devices. Both EPROM sockets must contain the same type of EPROM. These two jumpers are set as shown in Table 2-8.

Table 2-8. EPROM Jumper Configurations

EPROM Type	JMP1	JMP2: 1-2	JMP2: 2-3
2764	open	short	open
27128	open	short	open
27256	short	short	open
27512	short	open	short
Factory Setting	open	short	open

JMP3 - DRQ1

This jumper, when shorted, holds the 80186 DRQ1 input inactive.

FACTORY SETTING: shorted

JMP4 - 64K/256K RAM Select

This jumper, when shorted, selects 64K DRAM timing and control.

FACTORY SETTING: open

JMP5 - Clock

This jumper, when shorted, connects the system 16 mHz master clock bus to the 16 mHz hybrid oscillator (U6). It is intended for test purposes only.

FACTORY SETTING: shorted

JMP6 - SCSI-RDY

This jumper, when shorted, connects the READY output of the 5380 SCSI device to the ARDY input of the 80186. This signal is not used by the AMPRO ROM-BIOS.

FACTORY SETTING: shorted

JMP7 - SCSI Termination Power

This jumper, when shorted, connects the board's +5VDC to pin 26 of the SCSI bus connector. This is intended to provide a current source for external termination, and is only required if a cable-mounted terminator is to be used.

FACTORY SETTING: open

NOTE

No on-board protection diode is provided. Consequently, this jumper must NOT be installed on more than one bus device.

JMP8 - U45 Option

This jumper is shorted for 8 mHz-only operation of the 1772 FDC device.

NOTE

If this jumper is shorted, the clock multiplexor IC, U45 must NOT be present; if U45 is present, this jumper must be open.

FACTORY SETTING: open (U45 present)

JMP9 - NMI

This jumper, when shorted, holds the 80186 NMI input inactive.

FACTORY SETTING: shorted

JMP10 - TEST

This jumper, when shorted, holds the 80186 -TEST input low.

FACTORY SETTING: shorted

JMP11 - HOLD

This jumper, when shorted, holds the 80186 HOLD input inactive.

FACTORY SETTING: shorted

JMP12 - Diagnostic Jumper

Shorting this jumper grounds the 2681 serial controller's input port bit 6 (IP6). In addition, loopback from the 2681's output bit 6 (OP6) to IP6 is not functional (OP6 is open collector).

FACTORY SETTING: open

2.5 BOOTING THE SYSTEM

Assuming that you intend to boot the system from a standard IBM PC-DOS version 2.x or 3.x system diskette, you will only need to connect the board to one or more double-sided 48 tpi mini floppy drives, a terminal, and a source of power. A PC or other computer can be used as the terminal, using a suitable terminal emulation program (i.e., the AMPRO SuperDuo program).

The cable connections between the board's Serial Port A and an RS232C ASCII terminal are given in Appendix B. For first time startup, set the terminal as follows:

Baud Rate:	9600
Data Bits:	8
Parity:	off
Stop Bits:	1
Handshaking:	none

Set your terminal so that the Most Significant Bit (data bit #8) is transmitted as a 0 ("low" or "space"). Some terminals do not have a switch to do this, automatically sending a zero for data bit #8 when parity is off. The AMPRO ROM-BIOS does not mask the MSB when 8 bit transmission is selected.

With a terminal connected and turned on, the system is ready to boot. When power is applied, the ROM-BIOS will attempt to read the operating system from disk. If no disk is in the drive, the system will wait until a disk is in place, and the drive latch is closed. The system will then read the operating system from the disk in drive A.

If the drive's LED lights, but nothing else happens, try inserting the flip-side of the disk and pressing RESET. If this doesn't help, refer to the next section for troubleshooting information.

2.6 TROUBLESHOOTING

If the system did not work the first time, or fails sometime, you may have to troubleshoot it. The following are some suggestions:

- Recheck all wiring, soldered connections.
- Check that power is available from the power supply.
- Be certain that the drives are working, and are jumpered correctly.

  NOTE

  IBM PC drives are not jumpered in a "standard" manner; for use with Little Board/186, be sure drive A is jumpered as Drive Select 1, B as 2, etc. Also, the PC's drive cables have swapped drive select wires, rather than straight through connections as required by the Little Board/186.

- Verify that the drive you are using provides the required Drive Ready signal.
- If more than one drive select LED indicator lights during power-up, with drive handles closed (across slot), the board may be incorrectly connected to the drive cables. Switch the computer OFF and reverse the drive cable connector at the Little Board/186.
- Check the drive termination resistor pack(s) for proper location. Normally, this will be located at the drive connected at the end of the drive cable, and on only one drive.
- If you have the debugging Monitor EPROM option, you can verify some of the system functions using the debugger and other tools in the Monitor. Refer to the EPROM Monitor User's Manual.

If your system still does not boot after following these instructions, contact AMPRO customer service for assistance.

CHAPTER 3

OPERATION WITH PC-DOS

3.1 INTRODUCTION

Assuming you have successfully booted PC-DOS as described in Chapter 2, you will probably want to take advantage of the flexibility designed into the Little Board/186 ROM-BIOS and support software to create a customized PC-DOS based system.

This chapter provides an overview of the system configuration options that are available under the PC-DOS operating system, as well as a discussion of the degree of compatibility that the Little Board/186 offers relative to software written for operation on the IBM PC and compatibles.

A combination of standard IBM PC-DOS utilities, along with AMPRO-specific drivers and utilities, allows you to create a highly customized system. The required AMPRO-specific drivers and utilities are supplied on the Little Board/186 PC-DOS Support Software diskette. Please refer to the user's manual (P/N A74012) provided with that software, for full descriptions, operating instructions, and installation information.

3.2 PC SOFTWARE COMPATIBILITY

This section is intended to help you understand the extent of compatibility provided by the Little Board/186 with software written for the IBM PC and compatibles ("standard PC").

3.2.1 Hardware Considerations

The Little Board/186 is based on a 80186 integrated, high-performance 16-bit microprocessor, which provides a functional superset of the 8-bit 8088 microprocessor used in the "standard PC." Programs written for an 8088 microprocessor can run on an 80186 without modification, but with a performance improvement of up to 300 percent.

Many of the hardware devices present on the Little Board/186, and their I/O port addresses, differ from those of the "standard PC." This includes: the 2681 serial communications controller; the 1772 floppy disk controller; the hard disk interface (SCSI); and the DMA, interrupt, and timing controllers contained within the 80186 microprocessor. Furthermore, the Little Board/186 utilizes an RS232C ASCII terminal as a user console (keyboard and monitor) rather than the keyboard and display controller used in a "standard PC."

As a result, programs which make direct access to board hardware, including both I/O ports and display controller "video RAM," rather than using the operating system or ROM-BIOS functions provided for the same purpose, can not be used without I/O driver modifications.

3.2.2 Operating System

System Boot

The AMPRO ROM-BIOS normally supplied on the Little Board/186 allows the use of IBM PC-DOS versions 2.x or 3.x as the board's operating system. PC-DOS version 3.x is required for hard disk usage, while version 3.2 is required for systems with an 80-track (720K) drive A.

Files and Data

When operated under PC-DOS, the Little Board/186 provides full PC file and data compatibility. Diskettes may be copied, formatted, verified, etc. on either for the other. All of the PC-DOS 40-track mini floppy formats, and the PC-DOS Version 3.2 80-track micro floppy formats, are supported, including single- and double-sided, and eight and nine sectors per track.

Commands, Drivers, and Utilities

Most of the standard PC-DOS operating system internal commands, and many of the disk-based utilities, function normally on the Little Board/186. Because the Little Board/186 ROM-BIOS does not contain Basic, however, none of the Basic programs included on the PC-DOS diskettes are usable. In addition, the graphics related utilities can not be used. Several PC-DOS functions require the use of the installable AMPRO drivers contained on the Little Board/186 PC-DOS Support Software diskette, as discussed in the software user's manual.

3.2.3 ROM-BIOS Functions

In addition to supporting the standard PC-DOS functions, the Little Board/186 ROM-BIOS provides a software interrupt interface which is a highly compatible subset of the "standard PC" ROM-BIOS software interrupt structure.

The console and keyboard ROM-BIOS interrupts are mapped to Serial Port A, so that an RS232 ASCII terminal can be used for the required keyboard/monitor functions. The board's Serial Port B is supported as the PC-DOS COM1 port; the Centronics printer port is LPT1. The Time of Day clock and Disk I/O functions are also supported in the standard manner.

The video display interrupt (INT 10H) of the ROM-BIOS supports the Write TTY function only. This results in full compatibility with "MS-DOS generic" programs, provided the program includes a terminal installation utility. Compatibility with the "standard PC" ROM-BIOS functions for cursor addressing, clear screen, etc., requires use of the terminal driver included on the Little Board/186 PC-DOS Support Software diskette.

Hard disk support (INT 13H) is also provided, using the board's SCSI port. This includes the ability to configure a system to boot from a SCSI-based hard disk drive.

A detailed discussion of the Little Board/186 ROM-BIOS software interrupts is given in Chapter 5. Information on the installation and use of the AMPRO-specific drivers and utilities are provided in the Little Board/186 PC-DOS Support Software User's Manual.

3.2.4 Applications Software

MS-DOS Generic Programs

Programs and utilities written for operation on any MS-DOS system are called "MS-DOS Generic." These programs restrict their system access exclusively to functions provided by the operating system. MS-DOS Generic programs are "hardware independent"; they can be used on a variety of hardware implementations, including systems such as the Little Board/186 that use RS232C ASCII terminals as the system console. Such "well behaved programs" nearly always run without modification on the Little Board/186. MS-DOS Generic programs generally have a terminal installation utility which allows you to specify the terminal to be used as the system console device, usually from a menu.

Here are a few popular application programs known to be available in MS-DOS Generic versions: Multiplan (Version 1), Wordstar (Version 3), DBase II, SuperCalc2, the T/Maker Integrated Software package. In addition, most languages and software development tools have MS-DOS Generic versions, including: Microsoft C (Version 3), Basic, and MASM; Turbo Pascal, Palasm, Abel; the Intel 86-family development tools.

Programs Which Make ROM-BIOS Calls

Many popular programs written for use on the "standard PC" violate the rules of operating system usage, making direct ROM-BIOS calls, accessing system I/O ports and video RAM directly, etc. Of these, programs which only make direct ROM-BIOS calls can often be used on the Little Board/186, providing that the optional video and keyboard driver software from the Little Board/186 PC-DOS Support Software are in use.

Programs Which Make Direct Hardware Access

Programs that talk directly to hardware (floppy controller, serial ports, keyboard port, video RAM, etc.) generally do not run on the Little Board/186 without modification. Some examples include:

- Copy protected programs: often use floppy controller, serial port, or printer port hardware.
- Communications programs: generally access serial port hardware
- Programs using graphics: generally access display controller hardware
- Programs that write to Video RAM

Included in this group are many "consumer programs," including: Lotus 1-2-3, Symphony, DBase III, Flight Simulator, etc.

A "Video RAM Emulator" daughter board is available for the Little Board/186, which simulates a PC display controller. The Video RAM Emulator detects writes to "video RAM"; its associated software drivers forward the data to the RS232C console device, using appropriate terminal control sequences. Using

The Video RAM Emulator, software which is intended for operation on a standard monochrome video display controller will usually run properly, with the exception of the use of bit-mapped graphics.

Designing Software for Compatibility

To provide full compatibility between the Little Board/186 and the standard PC, the application software must simply confine itself to standard PC-DOS and the supported ROM-BIOS functions, rather than performing direct hardware accesses.

3.3 CONFIGURATION OPTIONS

Chapter 2 discussed the basic requirements for booting from a standard "out of the box" IBM PC-DOS (versions 2 or 3) system diskette. Once your system has booted successfully, you can tailor your software configuration to a custom hardware configuration. Your options include:

- Terminal baud rates other than 9600 baud (up to 38.4K)
- Parallel or Serial Printers
- Modems
- Additional -- or different types of -- floppy drives
- One or more hard disk drives
- RAM disk

A brief discussion of each of these configuration options follows. Actual configuration and installation details are provided in the Little Board/186 PC-DOS Support Software User's Manual (P/N A74012).

3.3.1 Terminal

Nearly any RS232C ASCII terminal can be used with your system. The initial terminal characteristics for first time booting must be set as described in Chapter 2 (9600 baud, 8 data bits, etc.). Once your system is initially booted, you can configure a custom system boot diskette for alternate console parameters. Baud rates up to 38.4K baud, as well as alternative data word formats, are available.

Display and keyboard drivers, available on the Little Board/186 PC-DOS Support Software diskette, provide mapping of the functions used to control a standard PC video display (cursor positioning, clear screen, etc.) and keyboard into the control codes required by your specific terminal.

3.3.2 Printers

The system can be used with both Centronics type parallel printers, and with RS232C ASCII serial printers. The Centronics port is supported as the DOS "LPT1" device. Most application software uses LPT1 as the default printer port, so printing to the parallel printer interface is automatic.

The board's Serial Bort B, supported as the DOS "COM1" device in the ROM-BIOS, can be used as a serial printer port, and can be configured for a wide variety baud rates and data word formats. Hardware handshaking (e.g. RTS/CTS) can also be configured for use with printers that require it.

3.3.3 Modems

Serial Port B can also be used as a modem interface, accessed as the DOS "COM1" device. Serial Port B data characteristics are initialized in the same manner as when the port is used as a serial printer interface, using the AMPRO utilities from the PC-DOS Support Software.

Most communications programs perform direct serial port I/O, rather than using the DOS or ROM-BIOS functions. Such programs must be customized before use. (See Chapter 5.)

The AMPRO LBCOMM.EXE program, included on the AMPRO PC-DOS Support Software diskette, is a full-featured communications program for the Little Board/186. LBCOMM offers remote system access, terminal emulation, and both XMODEM and ASCII file transfer functions.

Several other high quality communications programs are available specifically configured for the Little Board/186. These include:

- MEX-PC (NightOwl Software, Inc.)
- MICROLINK II (Wordcraft).

3.3.4 Unique Floppy Configurations

When your system initially boots from a standard PC-DOS system diskette, the floppy configuration is set for one to four 40-track (48 tpi) drives, depending on the setting of jumpers at position J7 (see Chapter 2). You can configure a system for use with 80-track mini or micro floppy drives, including the ability to boot from an 80-track device (requires PC-DOS 3.2).

One handy feature of PC-DOS is its built-in support for single-drive systems. If you jumper the Little Board/186 drive quantity jumpers (J7) to "one," the operating system will automatically assign drive letters "A" and "B" to the single floppy drive. With this configuration, you can copy files between two diskettes as though your system has two drives; PC-DOS will prompt you to change diskettes when needed.

3.3.5 Hard Disk Drives

Hard disk drives and controllers with SCSI (SASI) interfaces may be easily added to your system. Support for the first hard disk device, from which your system can be configured to boot, is contained within the Little Board/186 ROM-BIOS. Additional drives can be added as well, using the AMPRO HARD.SYS device driver. Consult the AMPRO PC-DOS Support Software user's manual for further details.

3.3.6 RAM Disk

PC-DOS Version 3 provides a useful virtual disk device driver, called VDISK.SYS, which allows you to configure one or more RAM disk drives based on memory on the Little Board/186.

CHAPTER 4

THEORY OF OPERATION

4.1 INTRODUCTION

This chapter is intended to provide a basic understanding of the functional operation of the Little Board/186 for programmers, hardware engineers, system integrators, and other technically oriented users.

The functional behavior of many of the board's devices is highly dependent on programming options. Therefore, to assist your understanding of the normal functions performed by these devices as used on the Little Board/186, some reference is made to the AMPRO ROM-BIOS default device configurations.

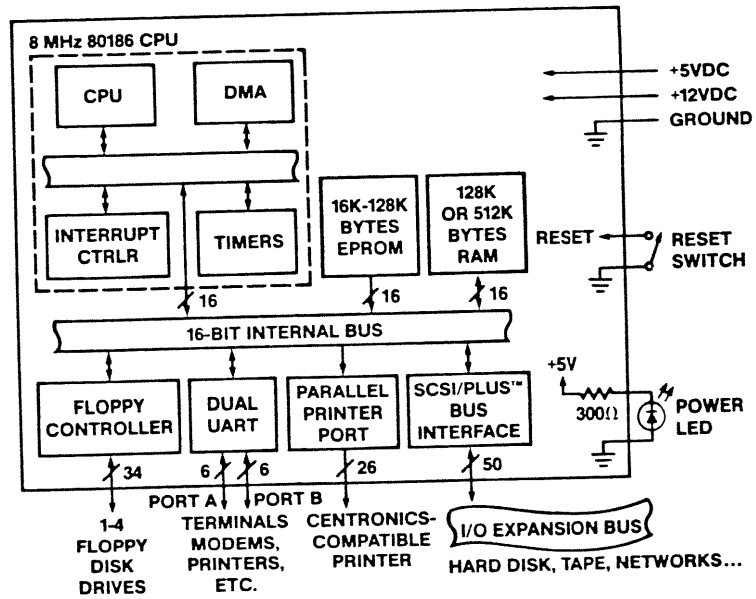

Figure 4-1. Little Board/186 Block Diagram

Data sheets are included in Appendix D for the 80186 (CPU), 2681 (UART), 1772 (FDC), and 5380 (SCSI) devices. You may also wish to obtain a copy of the following especially valuable publication, available from Intel Corporation:

AP-186: Introduction to the 80186 Microprocessor

A detailed technical manual on the 5380 is also available AMPRO for a nominal charge.

4.2 THE 80186 INTEGRATED CPU

The architecture of Little Board/186 (see Figure 4-1) is based on the 80186 integrated microprocessor unit. The 80186 device includes a 16-bit CPU, a 2-channel DMA controller, three 16-bit timers, a programmable interrupt controller, and programmable memory and I/O chip-select logic. The 80186 is more than a highly integrated version of the 8086 microprocessor; instruction execution and pipeline efficiency of the 80186 represent substantial performance improvements relative to the older 8086 device.

Since many of the 80186 characteristics are programmable -- including memory chip select addresses and timing -- the software has the responsibility to initialize these immediately on powerup. The discussion in this chapter assumes the default initialization performed by the AMPRO ROM-BIOS. Refer to Chapter 5 (Programmer's Reference) for additional programming details.

4.2.1 Chip Selects

The chip select outputs provided on the 80186 are used to control the I/O peripheral chips and EPROMs. Both the access addresses and wait state timing of these chip select outputs are programmable. Five of the six Peripheral Chip Selects (PCS0-5), in combination with a custom I/O Controller IC are used to provide device selects for all of the board's on-board I/O functions. No wait states are required.

4.2.2 Interrupts

The 80186 contains an internal four channel interrupt controller, utilized as follows:

INTR0: 2681 serial controller device interrupt.

INTR1: 5380 SCSI interface controller device interrupt.

INTR2: 1772 floppy disk controller device interrupt.

INTR3: Centronics printer port interrupt.

All are edge triggered interrupts and are sensed by the 80186 as active high. These interrupts are controlled using the 80186 internal interrupt controller.

4.2.3 Counter/Timers

The 80186 provides three 16-bit internal timers. Two of these have off-chip input and output terms, allowing their use as counters as well. The 2681 serial controller provides an additional general purpose timer channel, which is discussed in the section on that device. The three channels of the 80186 are used as follows:

Channel 0 — The AMPRO ROM-BIOS uses this counter/timer channel in conjunction with Channel 2 to provide an accurate real time clock function (18 ticks/second). Channel 2 acts as a prescaler, providing a 16 microsecond input rate to this channel.

Channel 1 — This counter/timer channel has its external counter input driven by the timer output of the 2681 serial controller. This allows the timing of long intervals, etc.

Channel 2 — This timer-only channel must be programmed to provide the required 16 microsecond DRAM refresh rate.

4.2.4 DMA

The 80186 internal DMA controller provides two powerful DMA channels. These are used as follows:

Channel 1 — This DMA channel forms an important part of the DRAM refresh logic. (See next section.) It is programmed to generate a linear 20-bit address, timed by timer channel 2, with no terminal count.

Channel 2 — This DMA channel is shared between the floppy and SCSI interfaces, as programmed in the FDC Control Register.

4.3 MEMORY

Little Board/186 supports EPROM address space of 16k to 128K bytes, for use with 2764 to 27512 standard JEDEC parts. The 80186 Upper Memory Chip Select (UMCS) is used for selection of the on-board EPROM memory. This chip select is programmed for 0 wait states and ignoring of external ready, for use with 250 nS access time EPROM's. The use of 250 nS EPROM's is required due to the 80186 data bus maximum output disable time.

A custom RAM Controller IC decodes DRAM timing directly from the 80186 control and status signals, so that 0 wait state operation with 150 nS DRAM is possible. RAM refresh addresses are provided by DMA channel 1 with control timing provided by one of the 80186 internal timer channels (ch2). The RAM Controller IC has an input pin which is used to select operation with either 64K or 256K bit DRAM devices. A low level on this pin programs the board for 64K bit DRAM operation.

The Lower Memory Chip Select (LMCS) and Middle Memory Chip Select (MMCS) lines are unused. Instead, the RAM Controller decodes its address range directly

from the address lines. Direct address decoding will also be used to decode the upper 512K of the 80186 megabyte address space on a plug-in memory expansion module. When this is done, UMCS will be used to disable access to the added memory in the high area for which the UMCS is programmed, depending on the EPROM size.

4.4 2681 SERIAL CONTROLLER

A 2681 dual Universal Asynchronous Receiver/Transmitter (UART) provides two channels of serial I/O. The 2681 also provides a number of signals for the parallel printer and floppy disk interfaces, and contains a programmable timer whose output can drive the 80186 counter/timer channel 1 input.

4.4.1 Serial I/O Ports

The 2861 provides two asynchronous serial I/O channels, featuring fully programmable serial data characteristics, including word length, parity, start/stop bits, and baud rate.

The device contains an internal baud rate generator, which operates from a 3.6864 mHz crystal source. Baud rates from 50 through 115.2K may be selected for each channel's receive and transmit data (independently). Both channels of the 2681 function in an identical manner.

RS232C signal levels are converted to and from TTL levels by a 75188/1488 line driver, and a 75189/1489 line receiver. An on board -12 volt DC-to-DC converter provides the -12VDC power for the line driver.

The 2681's OP0 (RTSA) and OP1 (RTSB) outputs generate each channel's Hand Shake Out signal, while the IP0 (CTSA) and IP1 (CTSB) inputs are used to provide each channel's Hand Shake In signal.

4.4.2 Signals Used by Other Interfaces

The 2681 Serial Controller contains an eight bit output port and a seven bit input port. Only four of these signals (OP0, OP1, IP0, and IP1) are used in conjunction with the board's serial ports. The other eleven signals are assigned as follows:

OP2 Drives the printer interface -DATA STROBE signal.
OP3 Drives the 80186 Counter/Timer channel 1 input signal.
OP4 Unused.
OP5 Drives the 1772 FDC controller -RESET input.
OP6 Looped to input pin IP6.
OP7 Drives the printer interface PRINTER INIT signal

IP2 Senses the printer interface BUSY signal.
IP3 Senses the floppy interface DRIVE READY signal.
IP4 Senses the printer interface -PRINTER SELECT signal.
IP5 Senses the printer interface -PAPER END signal.
IP6 Senses the state of output pin OP6 or JMP12.

The specific use of each of the above signals is covered in the floppy and printer interface sections, below. Note that output OP6 is looped to input

IP6, and also connected to JMP12 pin 1. Since OP6 is open drain, the state of jumper JMP12 can be sensed if OP6 is high.

NOTE

The 2681's output pins (OP0-7) are the compliment of the contents of the output port register. That is, setting a bit in the output port register results in a low (0) logic level at the corresponding output pin, and resetting a bit results in a high (1) level. The input pins (IP0-6), however, are not complimented. Therefore, the bits of the input register directly reflect the state of the corresponding input pins.

4.5 PARALLEL PRINTER PORT

An octal D-latch with a 24mA current sinking capacity is used as a Printer Data Register, driving the eight parallel printer port data lines. The eight data signals are written directly by the low order byte of the 80186 data bus by means of an output instruction. Six other input/output signals associated with this interface are also supported, as follows:

Signal Name	Connects To...	In/out	Polarity
DATA 1-8	Printer Data Register	Output	Normal
-DATA STB	2681 output OP2	Output	Normal
-PRINTER INIT	2681 output OP7	Output	Inverted
BUSY	2681 input IP2	Input	Normal
-ACK	80186 interrupt INT3	Input	Normal
PAPER END	2681 input IP5	Input	Inverted
SELECT	2681 input IP4	Input	Inverted

Each signal is shown as either inverted or non-inverted, which is relative to the actual external peripheral interface signal. When a signal is listed as "normal" polarity, this means that the interface connector pin has the **same** value as the programmed IC pin. For example, when 2681 input pin IP2 is high, the printer BUSY signal (J2, pin 21) is in a high state. (Refer to the NOTE in the section pertaining to the 2681 device, concerning output and input pin polarities.)

4.6 FLOPPY DISK INTERFACE

Most of the logic required for the floppy disk interface is provided by the WD1772 Floppy Disk Controller (FDC) device. The 1772 is a highly integrated device, and contains internal digital phased locked loop, digital write precompensation, CRC generation and checking, and motor control timing.

The 1772's interrupt request output connects to the INT2 interrupt input of the 80186. The 1772's DMA request output is one of two such signals selectively routed to the 80186 DR10 DMA request input, under control of the FDC Control Register.

The 1772's master reset pin is driven by the 2681 serial controller's OP5 output signal, such that the 1772 is held in a reset state when OP5 is low. This allows the 1772 to be reset under software control.

4.6.1 FDC Control Register

Additional control output signals, such as the four drive selects, are generated by the FDC control register. The FDC Control Register is written to directly by the low order byte of the 80186 data bus, using an output instruction. The FDC control register's output signals are utilized as follows:

The floppy disk interface READY input is inverted, and then connects to the 2681 serial controller's IP3 input signal. Not all floppy disk drives provide this signal.

The output signals of this register are all forced to 0's on powerup or reset. Output bits 0-4 and 7 drive signals on the floppy disk drive interface connector.

The 8-INCH SELECT signal allows the 1772 FDC device to send and receive data at 8-inch drive data rates, by doubling the device's master clock input frequency. However, the 1772 is currently not guaranteed to fuction properly at this doubled clock rate, and should therefore only be used in this manner with caution. A software-controlled RESET signal has been provided to assure that the 1772 does not become hung up when its master input clock is changed during operation. It is recommended that a FORCED INTERRUPT command be issued to the 1772 immediately following a change in its clock rate, and that the software-controlled RESET only be used when an error is detected, and as part of the 1772 initialization sequence following system powerup or reset.

4.7 SCSI/PLUS INTERFACE

The SCSI interface is completely controlled by the NCR 5380 protocol controller device. The 5380 provides an interface which meets the ANSI specification for SCSI, including Initiator role, Target role, Arbitration, and the Disconnect-Reselect function. It also supports the Initiator role of the AMPRO-proposed SCSI/PLUS enhancement to SCSI. The 5380 SCSI controller allows full programmable control of 17 bi-directional bus signals, and provides both buffered (low leakage) bus inputs and high current (48 mA) bus output drive capacity. The 5380 is described thoroughly in its data sheet, which appears in Appendix D.

The interrupt output of the 5380 connects to the 80186's INT1 interrupt input. The 5380's DMA request output signal is selectively connected, under control of the FDC Control Register, to the 80186 DMA request 0 input.

4.7.1 ID Input Register

An ID Input Register is used to read the state of eight sets of board jumpers. The eight bits are read in the lower half of the 80186 data bus, and represent the jumper settings as follows: when a jumper is installed, the bit will be read as a 0 (low), and when a jumper is not installed, the bit will be read as a 1 (high).

The AMPRO ROM-BIOS and AMPRO PC-DOS support drivers use these eight jumpers to determine various powerup defaults associated with the floppy and SCSI interfaces.

This port can also be used as a general purpose 8-bit input port in applications not using the AMPRO ROM-BIOS. In this case, the physical board layout of the eight pairs of jumper pins permits a 16-pin flat ribbon cable connector to be plugged directly onto them.

CHAPTER 5

PROGRAMMER'S REFERENCE

5.1 INTRODUCTION

This chapter contains information useful to programmers who intend to program Little Board/186 hardware directly. Normally PC-DOS handles the hardware for you, so that you need not be concerned with direct programming of the board's hardware -- that is the advantage of using a standard operating system. Since the AMPRO ROM-BIOS provides a high degree of compatibility with the IBM PC ROM-BIOS, there should be little need for custom programming.

The hardware theory of operation and interconnection is covered extensively in Chapter 4, whereas this chapter concentrates on details which directly relate to programming of the board's devices and I/O ports. Please read Chapter 4 before attempting to utilize the information provided in this chapter. For additional information about the board's LSI devices (80186, 2681, 1772, and 5380), refer to the data sheets in Appendix D, and to additional documentation available from the device manufacturers.

5.2 80186 UTILIZATION AND INITIALIZATION

Since the 80186 microprocessor has many programmable hardware functions which assume default values under control of the Little Board/186 ROM-BIOS, much of the information in this chapter is based on these defaults. Should you choose not to use the ROM-BIOS, these defaults (I/O port addresses, etc.) become your responsibility.

The 80186 contains a large number of internal read/write registers, called the "Peripheral Control Block," which is used for programming of the 80186's many internal functions, including the interrupt controller, DMA controller, and Counter/Timing Controller (CTC). The ROM-BIOS leaves the Peripheral Control Block at its power-up default I/O base address, FF00H, so that the registers within the Peripheral Control Block occupy I/O addresses FF20H through FFFEH. You can determine each individual register's address by adding the specific register's address offset, shown in the 80186 data sheet, to the Peripheral Control Block's base address, FF00H. For example: the UMCS Register has offset A0H, so its I/O address is FFA0H; the DMA Channel 0 Transfer Count Register has offset C8H, so its I/O address is FFC8H; etc.

5.2.1 Memory Map

The two byte-wide EPROM sockets are selected by the Upper Memory Chip Select (UMCS) output from the 80186. The 80186 UMCS is programmed on cold reset before jumping to the main task. There is enough code space at FFFF0H (the reset jump address) to program the EPROM size before jumping. The jump must be a long intersegment jump to initialize the code segment register. If a larger EPROM is to be used, the code at FFFF0H must be modified appropriately, to initialize UMCS for the required address space.

The ROM-BIOS programs UMCS for zero wait states, and ignoring of external ready. The base address of the EPROM is FC000H, to accommodate a pair of 2764

EPROM's, providing 16K of EPROM space.

The 80186 Lower Memory Chip Select (LMCS) and Middle Memory Chip Select (MMCS) lines are unused, and unprogrammed by the ROM-BIOS. This allows the lower and middle memory chip selects to be used for RAM wait state generation -- if needed -- though wait states should never be required with 150 nS, or faster, RAM. Due to the block size that these chip selects can span, they must be programmed wisely, if used.

On-board 512K or 128K RAM memory chip selection is decoded directly from the 80186 address lines, and is independent of the programming of the MMCS and LMCS lines. The 512K RAM expansion unit available from AMPRO also decodes its address space directly from the 80186 rather than using MMCS or LMCS. The 512K RAM expansion unit automatically deselects when UMCS is active, so that EPROM access overrides that of RAM.

5.2.2 I/O Map

The board's I/O device addresses are programmed by the ROM-BIOS to occupy I/O addresses from 1000H through 137FH, as shown in Table 5-1. Chip selects for the various I/O devices on the board are derived from the 80186 Peripheral Chip Selects (PCS), which are utilized as shown in Table 5-2. PCS6 is reserved for future use, such as selection of I/O devices on a plug-in daughter board. Wait state values shown in Table 5-2 are the defaults programmed by the ROM-BIOS.

Table 5-1. Summary of I/O Ports

Address	Input/Output	Function
1000H -101EH	I/O	2681 Internal Registers (See Table 5-4)
1080H -108FH	I/O	5380 Internal Registers (See Table 5-8)
1100H	I/O	1772 Command/Status Register
1102H	I/O	1772 Track Register
1104H	I/O	1772 Sector Register
1106H	I/O	1772 Data Register
1180H	I/O	5380 DMA Acknowledge
1200H	O	FDC Control Register
1280H	O	Printer Data Register
1300H	I/O	80186 PCS6 (currently unused)
FF20H -FFDAH	I/O	80186 Peripheral Control Block

Table 5-2. 80186 Peripheral Chip Select Usage.

PCSX	Read/Write	Wait States	Usage
PCS0	R/W	1	2681 chip select
PCS1	R/W	1	5380 chip select
PCS2	R/W	1	1772 chip select
PCS3	R/W	1	5380 DACK pin
PCS4	W	0	FDC Control Reg. data strobe
PCS5	W	0	Printer port data strobe
PCS6	R/W	0	Reserved for future use

5.2.3 Interrupts

The 80186 internal and external hardware interrupts are used as shown in Table 5-3. The table shows both internal interrupts from the timers and DMA channels and external interrupts from the four interrupt pins (INTRX). All of the external interrupts are edge sensitive, and are triggered on a low-to-high transition.

Table 5-3. 80186 Interrupt Usage

Priority (if used)	80186 Function	Vector "Type"	Usage
Internal Interrupts			
0	Timer	08H	Real time clock (18.2/sec)
n/a	Timer 1	12H	Not used
n/a	Timer 2	13H	Refresh timer (16 usec/tick)
n/a	DMA 0	0AH	SCSI EOP
n/a	DMA 1	0BH	Refresh DMA EOP
External Interrupts			
1	INTR 0	0CH	2681 interrupt
2	INTR 1	0DH	5380 interrupt
3	INTR 2	0EH	1772 interrupt
7	INTR 3	0FH	Printer interrupt

The ROM-BIOS uses each external hardware interrupt channel as follows:

Interrupt Channel 0 - 2681 Serial Controller Interrupt

Vector: 0CH
Priority: 1

This vector corresponds to that of the COM1 IBM PC device. The 2681 is used to implement the console port, a spare counter-timer channel, and miscellaneous I/O. Receive and transmit interrupts, break detect, counter timeout, and port bit input change interrupts are all possible. An interrupt vector table is provided by the ROM-BIOS to sort out the specific interrupt condition.

Interrupt Channel 1 - 5380 SCSI Controller Interrupt

Vector: 0DH
Priority: 2

This vector indicates an interrupt condition from the 5380 SCSI controller device. The 5380 interrupt occurs from a variety of bus events.

Interrupt Channel 2 - 1772 Floppy Disk Interface Controller

Vector: 0EH
Priority: 3

This vector is normally used to monitor the completion of a disk command when using DMA for floppy data transfers. It corresponds to that of the IBM PC.

Interrupt Channel 3 - Printer Interface Interrupt

Vector: 0FH
Priority: 7

This interrupt is triggered when the Centronics interface PRINTER ACKNOWLEDGE signal goes from inactive to active. It corresponds to the IBM PC printer interrupt vector.

5.2.4 DMA

The 80186 internal 2-channel DMA controller is normally used as follows:

DMA Channel 0 - SCSI/FDC DMA Data Read/Write

This channel is shared by the 1772 floppy disk controller and the 5380 SCSI interface controller. The contents of the FDC Control Register bit 6 determines which interface drives the 80186 DMA channel 0 transfer request input. Sharing of this DMA function between the floppy and SCSI interfaces has minimal impact since most software only performs one mass storage transfer operation at a time. Since SCSI data transfers are asynchronous, regulated by REQ/ACK handshaking, they could be done under programmed I/O if an application calls for interleaved transfer of SCSI

and FDC data.

The 1772 DMA acknowledge is a read or write of the 1772 data register, while the 5380 has a dedicated DMA acknowledge pin which is controlled by a dedicated 80186 Peripheral Chip Select. Maximum transfer speed is 2 megabytes per second.

DMA Channel 1 - Dynamic RAM Refresh Control

This channel controls dynamic RAM refresh. It is programmed for a memory-to-I/O transfer, with writes to nonexistant I/O space. A DMA cycle is requested by Timer Channel 2 every 16 microseconds. The DMA channel is programmed to continuously run through the entire megabyte of memory address space, with automatic rollover and no terminal count. It is set for word transfers (16-bit), so that the address increments by two each cycle (ADR1 is the LSB address input to the DRAM'S). This method of RAM refresh uses approximately 6 percent of the 80186 processing bandwidth. Since there is no terminal count interrupt service requirement, DRAM refresh continues uninterrupted even during 80186 halt states. This DMA channel should always be given the highest priority.

5.2.5 Counter/Timers

The 80186 internal 3-channel counter/timer controller (CTC) provides three interrupt sources. CTC Channel 0's interrupt is normally used to provide a real time clock tick, and interrupts from CTC Channels 1 and 2 are normally disabled. Channel 2 is used for regulating the time period of the DMA-controlled RAM refresh, and no software maintenance is required once that function is initialized. Channels 1 and 2 should not allowed to generate interupts, unless they can distinguish between a software call and hardware interrupt service request. (The 80186 interrupt request pending register can be read, to determine this.)

The ROM-BIOS uses the three CTC channels as follows:

CTC Channel 0 - Real Time Clock Tick

This channel is used for the real time clock tick, and may be programmed to simulate the IBM PC interrupt service routine. The required real time clock interrupt rate for compatibility with the IBM PC is 18.2 interrupts per second. In order to achieve this rate, CTC Channel 2 must be used as a prescaler.

This channel's interrupt vector, as used in the AMPRO ROM-BIOS, overlaps the IBM PC timer interrupt. (The ROM-BIOS calls INT 1CH.) The interrupt control register is programmed for non-nested mode and priority of 1; this timer's interrupt mask bit is cleared.

CTC Channel 1 - Not used

This channel is not used by the ROM-BIOS, and can be used to generate timing required by software functions. This channel is also cascaded with the 2681 counter/timer output, and can be used in conjunction with the 2681 for generating very accurate time intervals.

CTC Channel 2 - DRAM Refresh Rate

This channel is used to request DMA cycles for DRAM refresh. It is programmed for a 16 microsecond rate. The output of this channel is internally routed to Channel 0, which further divides the rate to obtain the real time clock tick.

5.3 SERIAL CONTROLLER

A 2681 Dual Asynchrounous Receiver/Transmitter (DUART) device provides two serial ports, a counter/timer, 7 signal input pins, and 8 signal output pins. There is one common interrupt to the 80186 for all functions. Multiple interrupts require a dispatch routine. This section defines the usage of the various portions of the 2681 device.

The 2681 data I/O lines (D0-D7) connect to the lower byte (D0-D7) of the system internal data bus. The 2681's internal registers occupy a block of 32 I/O addresses, beginning at the default base address of the 2681 programmed by the ROM-BIOS, 1000H. The A0-A3 address inputs to the 2681 connect to system address lines A1-A4. The 2681's internal register addresses are shown in Table 5-4.

5.3.1 Serial Port Interface

The board's two serial ports are implemented directly by the DUART's two serial channels. As indicated in the 2681 data sheet, the device's two channels can be programmed for data characteristics, baud rate, and optional RTS/CTS handshaking.

Transmit and receive baud rates for each channel are independently programmable, from 50 to 38.4K baud. Each channel's receiver has a four byte FIFO, with status flags for FIFO full and ready. Each channel can be programmed to wait until the FIFO is full before interrupting. This reduces CPU overhead when handling high baud rates. Each channel's transmitter has a holding register and a shift register, and provides both empty and ready status flags.

Table 5-4. 2681 Internal Registers

Address	Input/Output	Function
1000H	Input	Mode Register A (MR1A, MR2A)
1002H	Input	Status Register A (SRA)
1004H	Input	(Reserved)
1006H	Input	RX Holding Register A (RHRA)
1008H	Input	Input Port Change Reg. (IPCR)
100AH	Input	Interrupt Status Register (ISR)
100CH	Input	Counter/Timer Upper (CTU)
100EH	Input	Counter/Timer Lower (CTL)
1010H	Input	Mode Register B (MR1B, MR2B)
1012H	Input	Status Register B (SRB)
1014H	Input	(Reserved)
1016H	Input	RX Holding Register B (RHRA)
1018H	Input	(Reserved)
101AH	Input	Input Port
101CH	Input	Start Counter Command
101EH	Input	Stop Counter Command
1000H	Output	Mode Register A (MR1A, MR2A)
1002H	Output	Clock Select Register A (CSRA)
1004H	Output	Command Register A (MRA)
1006H	Output	TX Holding Register A (THRA)
1008H	Output	Aux. Control Register (ACR)
100AH	Output	Interrupt Mask Register (IMR)
100CH	Output	C/T Upper Register (CTUR)
100EH	Output	C/T Lower Register (CTLR)
1010H	Output	Mode Register B (MR1B, MR2B)
1012H	Output	Clock Select Register B (CSRB)
1014H	Output	Command Register B (CRB)
1016H	Output	TX Holding Register B (THRA)
1018H	Output	(Reserved)
101AH	Output	Output Port Configuration Reg (OPCR)
101CH	Output	Set Output Port Bits Command
101EH	Output	Reset Output Port Bits Command

5.3.2 Auxiliary Signals

The 7 input and 8 output general purpose I/O bits provided by the 2681 are used to provide control and status signals for a variety of Little Board/186 hardware functions. The 2681's Output Control Register is used to program the mode of these 15 I/O pins; the Output Port Register is used to the set the state of the output pins; the Input Port is used to read the state of the input pins.

The programmable output pins of the 2681 are set or reset according to values programmed in the 2681 Output Port Register. Bits of the Output Port Register can be individually set and reset. A bit is set by performing a write operation to one I/O port address, and reset by performing a write operation to a second I/O address. NOTE: The actual OP0-OP6 output pin values are the complements of the Output Port Register contents. Refer to the 2681 component

data sheet for further details.

The seven 2681 general purpose inputs are utilized as shown in Table 5-5; signal outputs provided by the 2681's general purpose outputs are shown in Table 5-6.

Table 5-5. 2681 General Purpose Input Signals

Bit 6	5	4	3	2	1	0
LOOP	PAPER	SEL	-RDY	BSY	HSIB	HSIA

Bit	Signal/Function
IP6	**LOOP** - Looped from output signal OP6; also reads the status of the diagnostic jumper, JMP12. If JMP12 is shorted, IP6 will be a 0 regardless of state of OP6.
IP5	**-PAPER** - Indicates the state of the OUT OF PAPER signal input from the printer interface (J2 pin 23). Inverted relative to the level on the connector pin. When the printer is out of paper this bit is a 0.
IP4	**-SELECTED** - Indicates the state of the SELECTED signal input from the printer interface (J2 pin 25). Inverted relative to the level on the connector pin. When the printer is on-line (SELECTED) this bit is a 0.
IP3	**DRIVE RDY** - Indicates the state of the floppy disk interface -READY signal (J6 pin 34). The signal is inverted relative to the connector pin. When this bit is a 1, the floppy media is up to speed.
IP2	**PRINTER BUSY** - Indicates the state of the BUSY signal input from the printer interface (J2 pin 21). Directly reflects the level on the connector pin. When the printer is busy, this bit is a 1.
IP1	**HSIB** - Indicates the state of Serial Port B Handshake In (HSI) signal (J4 pin 6). When Hand Shake In is active from the RS232 interface, this bit is a 1. Normally used as Channel B CTS.
IP0	**HSIA** - Indicates the state of Serial Port A Handshake In (HSI) signal (J3 pin 6). When Hand Shake In is active from the RS232 interface, this bit is a 1. Normally used as Channel A CTS.

Table 5-6. 2681 General Purpose Output Signals.

Bit 7	6	5	4	3	2	1	0
INIT	LOOP	-FDRST		TIMER	-STB	HSOB	HSOA

Bit	Signal/Function
OP7	**INITIALIZE** - Initializes the printer, when 1. The printer interface -INIT signal (J2 pin 26) is inverted relative to this pin of the 2681.
OP6	**LOOP** - Looped to input signal IP6. Has no effect when jumper JMP12 is shorted.
OP5	**-FDRST** - Hardware reset signal to the 1772 FDC. When this bit is a 0, the 1772 is held reset. (NOTE: The 1772 requires a minimum reset pulse width of 50 microseconds.)
OP4	Not used.
OP3	**TIMER** - Connected to 80186 Timer Input 1, for use as a prescaler input to 80186 CTC Channel 1.
OP2	**-STROBE** - Controls the printer interface -DATA STROBE signal (J2 pin 1). When this bit is a 0, -DATA STROBE is in its active low state.
OP1	**HSOB** - Sets the state of Serial Port B Handshake Out (HSO) output signal (J4 pin 4). When this bit is a 1, HSOB is active. Normally used as Channel B RTS.
OP0	**HSOA** - Sets the state of Serial Port A Handshake Out (HSO) output signal (J3 pin 4). When this bit is a 1, HSOA is active. Normally used as Channel A RTS.

NOTE

The 2681's output pins (OP0-7) are the complement of the contents of the Output Port Register. That is, setting a bit in the output port register results in a low (0) logic level at the corresponding output pin, and resetting a bit results in a high (1) level. The input pins (IP0-6), however, are not complemented. Therefore, the bits of the Input Port directly reflect the state of the corresponding pins.

5.3.3 Use of the Handshake In Signal

As indicated in Table 5-5, each serial channel has ony a single HANDSHAKE IN signal, connected to the respective channel's CTS pin on the 2681 serial controller. However, in most modem applications Data Carrier Detect (DCD) is the important input status signal. In this case, the HANDSHAKE IN signal can be connected to the modem's DCD signal instead of CTS; the software must

interpret the signal as DCD rather CTS.

If desired, the board's ROM-BIOS functions (INT14) can be used to transfer data and read the state of the DCD status signal. Again, "DCD" is not directly supported, but must be sensed through the "CTS" status bit supplied by the INT14 status function, since that bit reflects the state of HANDSHAKE IN status line.

5.4 Parallel Printer Interface

The Centronics printer interface consists of eight output data lines, two output control signals, and four input status signals. The data output lines are generated by the Printer Data Register. The output bits of the Printer Data Register drive the printer interface connector pins directly. The connector signals directly reflect the bit values written to the data register.

The -ACK signal from the printer interface connector (J2 pin 19) is used to provide an interrupt input to the 80186. The sense of interrupt sensing is such that an interrupt occurs when the -ACK signal makes a transition from 0 to 1, or active to inactive.

In addition, two output and three input signals associated with the printer interface are supported by the 2681 serial controller's general purpose I/O pins, as shown in Tables 5-5 and 5-6. Three of these signals are inverted relative to the printer interface connector (J2), as shown in the following summary of the five printer control and status signals:

INIT - Generated by 2681 output OP7. When this pin of the 2681 is a 1, the printer's internal logic is initialized. This output of the 2681 drives J2 pin 26 through an inverting buffer.

-DATA STROBE - Generated by 2681 output OP2. When active, signals the printer to accept (and print) data. This output of the 2681 drives J2 pin 1 through a non-inverting buffer.

-OUT OF PAPER - Sensed by 2681 input IP5. When 0, indicates that the printer is out of paper. The signal at 2681 input IP5 is inverted relative to the signal level at J2 pin 23.

-SELECTED - Sensed by 2681 input IP4. When 0, indicates that the printer is selected. The signal at 2681 input IP4 is inverted relative to the signal level at J2 pin 25.

BUSY - Sensed by 2681 input IP2. When 1, indicates that the printer is busy. The signal at 2681 input IP2 corresponds directly to the signal level at J2 pin 21.

5.5 Floppy Disk Interface

Most of the floppy disk interface support is provided by the 1772 Floppy Disk Controller (FDC) device. In addition, the FDC Control Register controls a number of signals associated with floppy disk interface functions.

Due to the complexity of programming of the floppy disk interface, we recommend that you utilize the standard functions available through PC-DOS function calls and ROM-BIOS interrupts rather than attempting to program this interface yourself.

The 1772 device is programmed as indicated in its component data sheet. For a variety of reasons beyond the scope of this document, the ROM-BIOS performs several functions in software which the 1772 data sheet claims the 1772 can do automatically. These are: motor on delay, head load delay, seek verification.

The 1772's data I/O lines (D0-D7) connect to the lower byte (D0-D7) of the system internal data bus. The 1772's internal registers occupy a block of 8 I/O addresses, beginning at the default base address of the 1772 programmed by the ROM-BIOS, 1100H. The A0 and A1 address inputs to the 1772 connect to system address lines A1 and A2, respectively. The 1772's internal register I/O port addresses are shown in Table 5-1.

The 1772 master reset pin is driven by one of the general purpose output bits of the 2681 serial controller, OP5. This allows the 1772 to be reset under software control. OP5 connects directly to the 1772's -RESET pin (pin 13), so that the 1772 is held in a reset state when 2681 output OP5 is a 0.

Pin 34 of the floppy disk drive interface (J6) connects to the 2681 serial controller's general purpose input IP3 through an inverting buffer. This signal is often used as DRIVE READY status signal, but varies among different drive manufacturers. The ROM-BIOS does not use this signal; software time delays (for head load and motor on) are used instead.

5.5.1 FDC Control Register

The FDC Control Register provides a number of important functions. The output bits of the FDC Control Register directly reflect the contents of the byte of data written to the register by the 80186 CPU. The functions of the eight output bits of this register are shown in Table 5-7.

Table 5-7. FDC Control Register Programming.

Bit 7	6	5	4	3	2	1	0
FDCLK	DMASEL	-DDEN	SIDE1	DS4	DS3	DS2	DS1

Bit	Signal/Function
Bit 7	**FDC Clock** - Selects either 8 mHz (when 0) or 16 mHz (when 1) as the clock input frequency to the 1772 FDC device. NOTE: Observe the precautions indicated in Chapter 5.
Bit 6	**DMA Select** - Switches the DMA request input to 80186 DMA channel 0 between the 1772 FDC (when 0) and the 5380 SCSI controller (when 1). Please observe the precaution indicated in Chapter 5.
Bit 5	**DDEN** - Double density enable. When 0, places the 1772 FDC in double density mode. When 1, enables single density.
Bit 4	**SIDE1** - Side one select. When 1, selects floppy disk drive side one. When 0, selects side zero.
Bits 0-3	**DS1-DS4** - Floppy disk drive selects. When the bit is 1, selects the corresponding floppy disk drive. Only one of these bits should active (1) at a time.

Here is a brief description of the FDC Control Register bit functions:

FDC Clock - Selects either 8 mHz (when low) or 16 mHz (when high) as the clock input frequency to the 1772 FDC device. Please observe the following precautions in programming this bit:

The 8-INCH SELECT signal allows the 1772 FDC device to send and receive data at 8-inch drive data rates, by doubling the device's master clock input frequency. However, the 1772 is currently not guaranteed to function properly at this doubled clock rate, and should therefore only be used in this manner with caution. A software-controlled RESET signal has been provided in case the 1772 hangs up when its master input clock is changed during operation.

It is recommended that a FORCED INTERRUPT command be issued to the 1772 immediately following a change in its clock rate, that the 1772's internal registers be re-written following clock changes, and that the software-controlled RESET only be used when an error is detected, and as part of the 1772 initialization sequence following system powerup or reset. It is further recommended that the state of this bit never be changed while any drive selects are active (i.e.: deselect all drives, change clock rate, reselect desired drive, delay appropriate head load delay).

DMA Select - Switches the DMA request input to 80186 DMA channel 0 between the 1772 FDC (when 0) and the 5380 SCSI controller (when 1). Please observe the following precaution in programming this bit:

WARNING

Never change the state of this bit while DMA channel 0 is enabled.

DDEN - Double density enable. When 0, places the 1772 FDC in double density mode. When 1, enables single density.

SIDE1 - Side one select. When 1, selects floppy disk drive side one.

DS1-DS4 - Floppy disk drive selects. When the bit is 1, selects the corresponding floppy disk drive. Only one of these bits should be active at a time.

5.6 ID INPUT PORT

This port can either be used for SCSI bus ID, for general purpose jumper settings, or as an 8-bit general purpose data input port.

The ID input port is read by an 80186 I/O input instruction. The jumpering of the eight pairs of pins at location J7 on the board determines the data byte obtained. The input buffer is non-inverting: the data read directly reflects the level on the input pin. When a jumper is inserted, the corresponding data is low (0); when out, the data bit is high (1).

Jumper assignment is as follows: J7 pins 1 and 2 corresponds to data bit 0; pins 3 and 4 are data bit 1; ...; pins 15 and 16 are data bit 7.

The ROM-BIOS default uses for these jumpers is discussed in Chapter 2, Board Jumper Configurations.

5.7 SCSI/PLUS INTERFACE

The SCSI/PLUS interface is controlled by means of an NCR 5380 SCSI Protocol Controller device. The 5380 contains 8 readable and 8 writable registers. These are accessed by 80186 I/O input and output instructions.

The 5380's data I/O lines (D0-D7) connect to the lower byte (D0-D7) of the system internal data bus. The 5380's internal registers and functions occupy a block of 16 I/O addresses, beginning at the default base address of the 5380 programmed by the ROM-BIOS, 1080H. The A0-A2 address inputs to the 5380 connect to system address lines A1-A3. The 5380's internal registers are shown in Table 5-8.

Table 5-8. 5380 Internal Registers.

Address	Input/Output	Function
1080H	Input	Current SCSI Data
1082H	Input	Initiator Command Register
1084H	Input	Mode Register
1086H	Input	Target Command Register
1088H	Input	Current SCSI Bus Status
108AH	Input	Bus & Status Register
108CH	Input	Input Data Register
108EH	Input	Reset Parity/Interrupt Command
1080H	Output	Output Data Register
1082H	Output	Initiator Command Register
1084H	Output	Mode Register
1086H	Output	Target Command Register
1088H	Output	Select Enable Register
108AH	Output	Start DMA Send Command
108CH	Output	Start DMA Target Receive Command
108EH	Output	Start DMA Initiator Receive

The SCSI/PLUS interface has a wide variety of applications, including:

- Use with SCSI (SASI) disk controllers and devices
- Use with the AMPRO SCSI/IOP for data acquisition and control
- Use as a bidirectional I/O port
- Use as a multi-master network bus

The AMPRO PC-DOS Support Software diskette provides SCSI support for "generic SCSI" hard disk controllers and drives. If you plan to use SCSI (SASI) devices not supported by the standard AMPRO drivers and utilities, you can either create a custom SCSI driver, modify the AMPRO drivers and utilities, or provide SCSI interface control within your program.

If you plan to program the 5380 yourself, you will probably require a copy of the NCR 5380 SCSI Interface Chip Design Manual, available through AMPRO for a nominal charge.

Copies of the ANSI X3T9.2 SCSI specification may be obtained by sending $20 and a self-addressed mailing label (for each copy desired) to:

The X3 Secretariat
Computer and Business Equipment Manufacturers Association
311 First Street, N.W. - Suite 500
Washington, DC 20001

The SCSI/PLUS Preliminary Technical Specification, which details AMPRO's proposed enhancement to SCSI to allow 64 (rather than 8) bus devices, is available through AMPRO for a nominal charge.

5.7.1 SCSI (SASI) Programming

When using the SCSI/PLUS interface with SCSI (SASI) disk controllers, special programming is not generally required; the AMPRO ROM-BIOS, and PC-DOS Support Software drivers and utilities accommodate many types of disk controllers and disk drives. Installation of the hard disk software is all that is generally required, providing you are using controller and drive types supported. (Refer to the AMPRO PC-DOS Support Software User's Manual.)

When using the 5380 in SCSI (SASI) applications, care must be taken to meet the specified timing constraints. For detailed timing information, consult your peripheral controller's technical manual, or the SCSI specification referenced above.

5.7.2 Simple Bidirectional I/O

If you plan to program the 5380 yourself, you will need a copy of the NCR 5380 design manual mentioned above. The 5380 has 17 bidirectional I/O lines, which may be used as inputs or outputs under software control.

The 5380 has two operating modes: Initiator and Target modes. In Initiator mode, several conditions are required before data output to the I/O bus can be active. If the device is used in the Target mode, however, these special conditions are not applicable. This results in more straight forward programming of simple I/O applications, and is recommended for simple bidirectional I/O.

The 5380 is placed in Target mode by writing 40h to the Mode Register. Once in Target mode, all 17 I/O signals except ACK and ATN may be used as both inputs and outputs. In Target mode, ACK and ATN are inputs only. The data lines (DB0-7,P) are outputs when bit 0 ("Assert Data Bus") of the Initiator Command Register is a 1, and inputs when bit 0 of that register is a 0.

Eight additional inputs are available via the ID Input Port, discussed above. Also, the parallel printer port can also provide an additional set of eight outputs and five handshake signals, if it not required as a printer interface.

5.8 ROM-BIOS INTERRUPTS

This section provides information on the software interrupts provided by the Little Board/186 ROM-BIOS. Compatibility with the IBM PC and PC-AT ROM-BIOS software interrupt calling conventions has been maintained wherever possible.

INT 10H - Video Display

The video display BIOS call is used to send characters to the system console device connected to the 2681 serial controller's channel A. The Little Board/186 supports only the "write tty" function. All other INT 10H function calls do nothing. This allows maximum RS232 ASCII terminal flexibility.

Support of the remaining functions is left to a terminal device driver, which allows various terminals to be controlled using BIOS calls. The

required device driver installs itself over the INT 10 vector and fields the BIOS calls. (See AMPRO PC-DOS Support Software User's Manual.)

If the 2681 automatic hardware handshaking has been enabled, and the 2681 cannot accept an output character, then the driver will hang up until the character has been sent.

Usage protocal:

AH = 0EH, write character in 'AL' to screen
AL = character

All registers preserved

Other INT 10H functions return to caller with no action taken.

INT 11H - Equipment Check

This BIOS call returns the value in the equipment flag stored in RAM at same location as that used by the IBM ROM-BIOS. This is a ROM constant, and always indicates: 1 RS232 device, 0 printers, 64K planar ram, bootable, 80 x 25 monochrome display, and the number of floppies determined by the jumpering of J7 pin pairs 1/2 and 3/4 (see Table 2-9).

Usage protocol:

Inputs: none

Output: AX contains the equipment flag, as described above.

INT 12H - Determine Memory Size

This BIOS call returns the total RAM size that is determined by the ROM-BIOS on powerup or reset. The result is stored in the same location used by the IBM ROM-BIOS.

Usage protocol:

Inputs: none

Output: AX = number of contiguous 1K blocks of memory

INT 13H - Hard Disk I/O

If a 5380 SCSI controller is present on the board, the hard disk support is installed at interrupt 13H location by the ROM BIOS, first relocating the floppy interrupt to INT 40H, and then replacing the address at INT 13H.

Usage protocol:

function	register
disk reset	ah, = 0
return disk status	ah, = 1
read sector(s)	ah, = 2
write sector(s)	ah, = 3
verify sector	ah, = 4
format track	ah, = 5, note 3
flag bad track	ah, = 6, note 2
format drive at track	ah, = 7, note 2
return drive parameters	ah, = 8
set drive parameters	ah, = 9, note 1
read with/ecc	ah, = A, note 1
write with/ecc	ah, = B, note 1
seek	ah, = C
reset disk controller	ah, = D, note 1
read controller buffer	ah, = E, note 2
write controller buffer	ah, = F, note 2
test drive ready	ah, = 10
recalibrate	ah, = 11
controller ram diagnostics	ah, = 12, note 2
disk drive diagnostics	ah, = 13, note 2
disk controller diagnostics	ah, = 14, note 1
read dasd	ah, = 15

Parameters passed in the following registers:

dl, = drive number, 0 to 7
dh, = head, 0 or 7
ch, = track number, 0 to max track
cl, = sector number, 0 to 17, bits 6,7 = msb of track
al, = number of sectors to be transfered
es:bx = pointer, segment in es:, offset in bx:

Returns:

good status	ah, = 0, sucessful read al, = number of sectors read cf, = 0, sucessful read
bad status	ah, = status cf, = 1, unsucessful read

Notes: (1) Returns good status
(2) Returns bad status
(3) Does not format track, HFORMAT is used to format.

INT 14H - RS232 I/O

This BIOS call controls serial channel B of the 2681 and expects to have a non-zero port address in the RAM data area at 40:0, just as in the IBM ROM-BIOS.

The serial port address at 40:0 is not used. The port number received in DX must be 0; if DX has a number greater than zero the call returns a time out. The initialization function sets the same baud rates, parity and number of bits as does the IBM ROM-BIOS.

The send and receive functions are identical to those of the IBM ROM-BIOS. Line status (returned in AH) is identical to that returned by the corresponding IBM ROM-BIOS functions, as the same status information is available from the 2681. The status call, however, differs in AL. Only status bits DSR and CTS are implemented, with DSR always a 1 and CTS reflecting the signal input to the 2681 from the hand shake in signal on serial port B. The ring indicator, receive line signal detect, and the Delta signals are not supported and are always returned as 0. This is because the 2681 does not offer support for these signals. The CTS signal can be used for a Data Carrier Detect (DCD) sensing by modem software, provided that the cable between the board and the modem has appropriate wiring.

Usage protocol:

```
DX = port number (must be 0)
AH = 0  initialize serial port B, return status in ah
AL = init value, as follows:
     bits 7,6,5 - baud rate:  110, 150, 300, 600, 1200, 2400,
                              4800, or 9600
     bits 4,3 - parity:       none, odd, even
     bit  2 - stop bits:      1 or 2
     bits 1,0 - bits/char:    7 or 8
AH = 1  sends the character in AL, returns status in AH
AH = 2  returns receive character in AL, returns status in AH
AH = 3  returns status in AX
```

INT 15H - Cassette I/O

This is a null function and returns a timeout.

INT 16H - Keyboard I/O

Interrupt 16 returns data input from the 2681 serial controller's channel A.

This ROM-BIOS call is identical to that of the IBM ROM-BIOS, with the following two exceptions:

(1) Characters are buffered in the same ring buffer space but no scan codes are stored. Consequently, there is twice the key buffering capacity for keystrokes.

(2) A scan code of zero is returned in AH, always. Keyboard shift status is always returned as caps active (40H), and it is stored at the same RAM location as in the IBM ROM-BIOS.

Usage protocol:

AH = 0 Returns the next character input from the console. Result in AL, scan code (always 0) in AH.

AH = 1 Sets Z flag to indicate if character available, as follows:

```
ZF = 1    Key not available
ZF = 0    Key "down"
```

When ZF = 0, the next character in the buffer to be read is in AX, and entry remains in the buffer.

AH = 2 Returns keyboard shift status in AL, as caps active (40H).

INT 17H - Printer I/O

The printer I/O BIOS vector supports the DOS LPT1 device (DX = 0) only, mapping it to the the board's Centronics printer port. The protocol is has a few minor differences from that of the IBM ROM-BIOS. The print character timeout is a fixed constant and not in RAM as the IBM XT and later use. The printer status returned supports all bits except the hardware I/O error bit, which has no cable input connection. If DX is non-zero on input, a timeout error results.

Usage protocol:

```
AH = 0   Sends character in AL to printer port, returns status in AH
AH = 1   Initializes printer, returns status in AH
AH = 2   Returns printer status in AH

Where:   DX = port value. Must be zero or a timeout results.

Outputs: Same status returned as in IBM ROM-BIOS, except I/O error
         bit. All registers except AH are preserved.
```

INT 18H - Resident BASIC

The ROM basic interrupt points to the cold boot, as there is no ROM BASIC.

INT 19H - Boot Strap Loader

INT 19H, the boot strap loader interrupt, tries 3 times to read the boot sector from floppy drive 0 (A). After the 3 floppy tries INT 19H will attempt to read the boot sector from the hard disk system. During this sequence if any read is sucessful, the sector read will be tested for validity. If valid, a jump to the boot sector code is made.

NOTE: If no NCR 5380 is installed the hard disk interrupt is not installed during system initialization.

INT 1AH - Get/Set Time of Day

Interrupt 1AH is used to get or set the BIOS real time clock. The following parameters are passed.

function	register
get tod	ah, = 0
returns	current time of day cx, = high count dx, = low count al, = rollover count value
set tod	ah, = 01 cx, = high count dx, = low count

INT 1BH - Keyboard Break

The Keyboard break interrupt vector is neither called nor supported in the ROM-BIOS. This is left to the terminal drivers.

INT 1CH - Timer Tick Interrupt

This interrupt is not used by the ROM BIOS and points to an IRET. It is called during each tick of the timer. (Tick INT 8H, 18 per/sec)

Application programs that need servicing at regular intervals patch this interrupt for their own status entry routines.

INT 1DH - Video Initialization

Not used.

INT 1EH - Diskette Parameters

The diskette I/O does not use the disk parameter table pointer. Also, the RAM storage location for motor turnoff delay (MOTOR_WAIT) is not used, as the 1772 handles this automatically.

INT 1FH - Video Graphics Characters

Not used.

INT 40H - Floppy I/O

The floppy interrupt is installed at INT 40H if the NCR 5380 SCSI interface is installed. If the 5380 is not installed the floppy I/O is interrupt 13H.

Usage protocol:

function	register
disk reset	ah, = 0
disk status	ah, = 1, return last disk status
read	ah, = 2
write	ah, = 3
verify	ah, = 4, no data transfered
format track	ah, = 5

For functions 2 thru 4 the following registers are used:

dl, = drive number, 0 to 3
dh, = head, 0 or 1
ch, = track number, 0 to 79
cl, = sector number, 0 to 8, or 0 to 9
al, = number of sectors to be transfered
es:bx = pointer, segment in es:, offset in bx:

For function 5, format track, ES:BX points to a table of sector headers (1 header per sector) with the following format:

1. track number
2. head number (side)
3. sector number
4. bytes per sector
   00 = 128 bytes
   01 = 256 bytes
   02 = 512
   03 = 1028

Returns:

good status	al, = number of sectors read ah, = 0, sucessful read cf, = 0, sucessful read
bad status	ah, = status cf, = 1, unsucessful read

INT 41H - Hard Disk Parameters

Interrupt 41H points to the hard disk parameter table.

APPENDIX A

TYPICAL INTERFACE CABLES

This Appendix contains wiring information for connection of the two Little Board/186 serial ports to typical terminals, modems, and serial printers. In the tables, signal directions are relative to the Little Board/186.

TERMINAL CABLE

Table A-1 lists the pin connections generally used to connect to a terminal. To reduce EMI radiation, the cable should be shielded, with the shield connected to the connector shell. The terminal connector can be either male or female, depending upon the specific terminal.

Table A-1. Typical Terminal Cable Wiring

Board Connector (J3)	Signal Name	Function	Terminal Connector (DB-25)
1	Ground	Protective Ground	1
5	RxD	Data Input	2
3	TxD	Data Output	3
4	HSO	Handshake Signal Out	5
2	Ground	Signal Ground	7
6	HSI	Handshake Signal In	20

SERIAL PRINTER CABLE

Table A-2 lists the pin connections generally used to connect Serial Port B to a serial printer. To reduce EMI radiation, the cable must be shielded, and the shield must be connected to the connector shell. The printer connector can be either male or female, depending upon the specific printer.

Table A-2. Typical Serial Printer Cable Wiring

Board Connector (J4)	Signal Name	Function	Printer Connector (DB-25)
1	Ground	Protective Ground	1
5	RxD	Data Input	2
3	TxD	Data Output	3
4	HSO	Hand Shake Out	5
2	Ground	Signal Ground	7
6	HSI	Hand Shake In	(11)*

NOTE

"Handshake Signal In" must connect to the printer's "Busy" output, i.e., the signal which tells the computer to start/stop sending data to the printer. The specific printer connector pin required for "Handshake Signal In" may vary between printers, so be sure to consult your printer's instruction manual.

MODEM CABLE

Table A-3 lists the pin connections generally used to connect to a modem. To reduce EMI radiation, the cable must be shielded, and the shield connected to the connector shell. The connector for the computer end must be a male DB-25, while the modem connector can be either male or female (usually male), depending upon the specific modem.

Table A-3. Typical Modem Cable Wiring

Board Connector (J4)	Signal Name	Function	Modem Connector (DB-25)
1	Ground	Protective Ground	1
5	RxD	Data Input	3
3	TxD	Data Output	2
4	HSO	Hand Shake Out	20
2	Ground	Signal Ground	7
6	HSI	Hand Shake In	5

CONNECTORS

Table A-4 lists mating connectors used with the Little Board/186.

Table A-4. Mating Connector Part Numbers

Board Connector	Function	Part Number
J1	Power Connector	Housing: AMP 1-480424-0 Contacts: AMP 60619-1 (4 req.)
J2	Parallel Printer, Board end	3M: 3399-6000 T&B: 609-2601M Molex: 15-29-8262
	Parallel Printer, Printer end	AMP: 57F-30360 3M: 3366-1001 T&B: 609-36M
J3,4	Serial Ports A,B	Housing: Molex 22-01-2067 Contacts: Molex 08-50-0114 (6 req.)
J5	RESET, Power LED	Housing: Molex 22-01-2047 Contacts: Molex 08-50-0114 (4 req.)
J6	Floppy Disk Interface (Card edge connectors)	3M: 3463-0001 T&B: 609-3415M Molex: 15-29-0341
J8	SCSI/PLUS Interface	T&B: 609-5000M Molex: 15-29-8502 Berg: 66902-150

Actual Size