

DSTD-102 CPU AND SERIAL I/O

OPERATION MANUAL

Rev 6

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NOTICE

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CHANGE NOTICE

Revision 6 of the DSTD-102 contains several significant enhancements over revision 4 and earlier boards. These enhancements have been added following customer requests to take advantage of recent technology developments.

1. The DSTD-102 now supports 8 kbyte RAMs (Intel 2186) and 16 kbyte EPROMs. Note that the addition of this feature required the re-layout of the memory device jumper blocks JB9, JB10 and JB12. Refer to section 3.2 for a complete description.
2. The memory decode PAL now supports six different memory configurations, including 2K, 4K, 8K and 16K configurations in the one PAL
3. Using a jumper block the DSTD-102 will now support both "synchronous" edge triggered push button reset (available on rev 4 boards) and level sensitive resets (new). The level sensitive push button reset capability is required when using brown-out detection logic such as that on the DSTD 703.
4. This rev allows full access to the on-board I/O devices from other cards in the system. This is particularly useful when the DSTD-103 slave processor is being used.

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SECTION 1

1.0 GENERAL INFORMATION

1.1 Introduction

The dy-4 SYSTEMS' DSTD-102 CPU, Figure 1 - 1, is a Z80 based microcomputer board. It features a CPU chip, two serial communications channels, 4 counter/timers and three 28 pin memory sockets for byte-wide memory devices.

1.2 DSTD Series General Description

The DSTD series was designed to satisfy the need for low cost OEM microcomputer modules. The DSTD-Z80 BUS uses a motherboard interconnect system concept. The modules for the STD-Z80 BUS are a compact 4.5 x 6.5 inches which provides for system partitioning by function, e.g. CPU, Memory, I/O, etc. This smaller module size makes system packaging easier, while increasing MOS-LSI densities provide high functionality per module.

1.3 DSTD-102 Features

- . Utilizes the powerful Z80 microprocessor
- . Provides three 28 pin sockets which may be strapped to accept any combination of the following industry standard memory devices.

EPROM		STATIC RAM		ROM
2758	(1kx8)	4118	(1kx8)	
2759	(1kx8)			
2716	(2kx8)	4802	(2kx8)	MK34000 (2kx8)
2732	(4kx8)			
2764	(8kx8)	2186	(8kx8)	
27128	(16kx8)			

- . Four cascadable counter/timer channels
- . 2 serial RS-232C channels - Channel A has two additional RS-232C drivers and receivers for external clocking allowing full synchronous operation.
- . Transmit and Receive LEDs on Channel A
- . Fully buffered signals for system expandability

- . Selectable reset address to either 0000H or E000H
- . All on-board memory can be disabled and enabled under software control
- . Selectable WAIT state generator for memory devices on all M1 cycles, MEMRQ cycles or all INTAK cycles
- . Compatible with MDX-SST for single step operation during debugging
- . 4MHz version available
- . STD-Z80 bus compatible

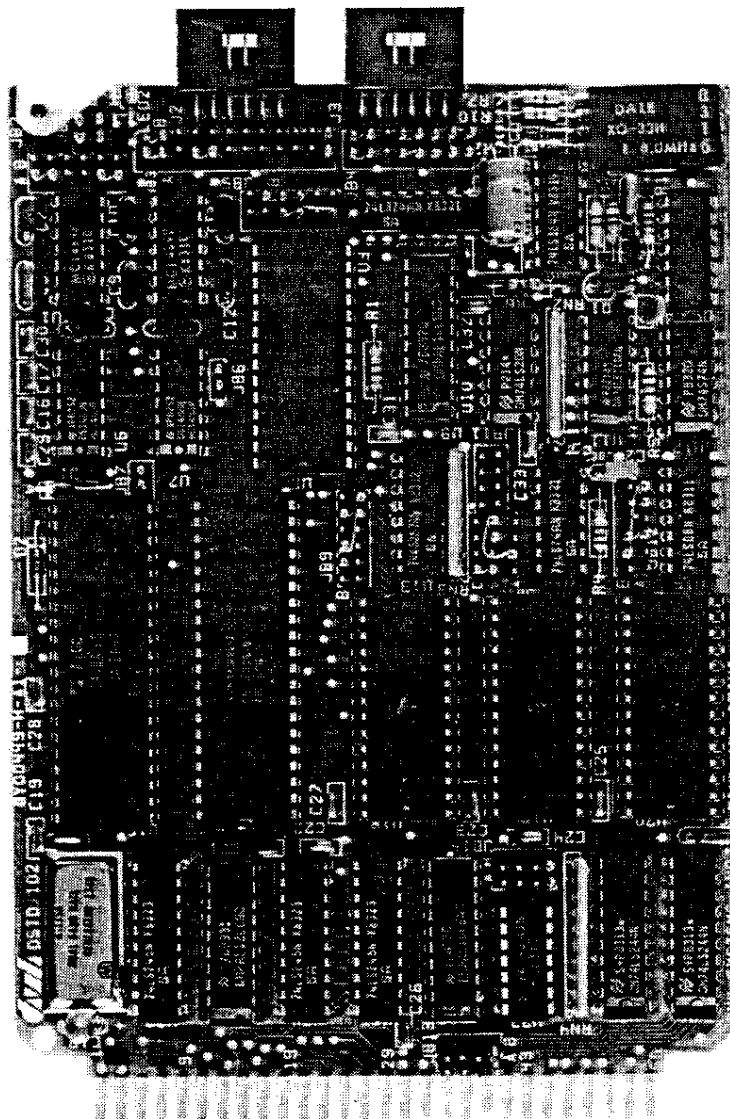


FIGURE 1 - 1 DSTD-102 MODULE

SECTION 2

2.0 FUNCTIONAL HARDWARE DESCRIPTION**2.1 Introduction**

The DSTD-102 utilizes a Z80 microprocessor as the system controller. It features three 28 pin memory sockets which enables the user to populate the module with any combination of designated ROM and EPROM. Custom address decoding allows the user to configure the memory on any 8K boundary of the 64K memory map. A PAL decoder is supplied to allow the user to choose one of six popular memory configurations, or if desired the user may implement other mixtures of memory devices simply by programming the PAL accordingly.

A 4 channel counter/timer circuit is included for software controlled counting and timing functions. On-board strapping options make it possible to cascade the four CTC channels for long count sequences. The CTC may also be used as a baud rate generator for the serial channels if non-standard baud rates are required.

The DSTD-102 has two serial channels implemented using the Z80-SIO LSI chip. The SIO allows for both asynchronous and synchronous (SDLC, HDLC, BISYNC, etc.) modes. Channel A can be used as both asynchronous and synchronous modes and channel B provides asynchronous operation. (Synchronous operation is available on the DSTD-102A version of the board - not the standard DSTD-102.) Channel A has additional RS-232C drivers and receivers for external clocks. In asynchronous mode both channels will operate up to 19.2k baud using the baud rate generator. The CTC may be used for higher rates. Channel A will run to 307 kilobaud in synchronous mode.

A strapping option allows the user to select the reset address to be either 0000H or E000H. The E000H option is required for use of standard software and hardware products including dy-4 SYSTEMS Debug Monitor (DDM) and Disk Control Monitor (DCM) firmware products. Also these products require onboard RAM strapped to reside at location F000H to FFFFH.

The DSTD-102 is available in 2.5 MHz and 4 Mhz versions.

2.2 Block Diagram Description

Figure 2 - 1 is a block diagram illustrating the flow of system address, data and control signals on the DSTD-102. The following paragraphs describe the function of each of the major blocks.

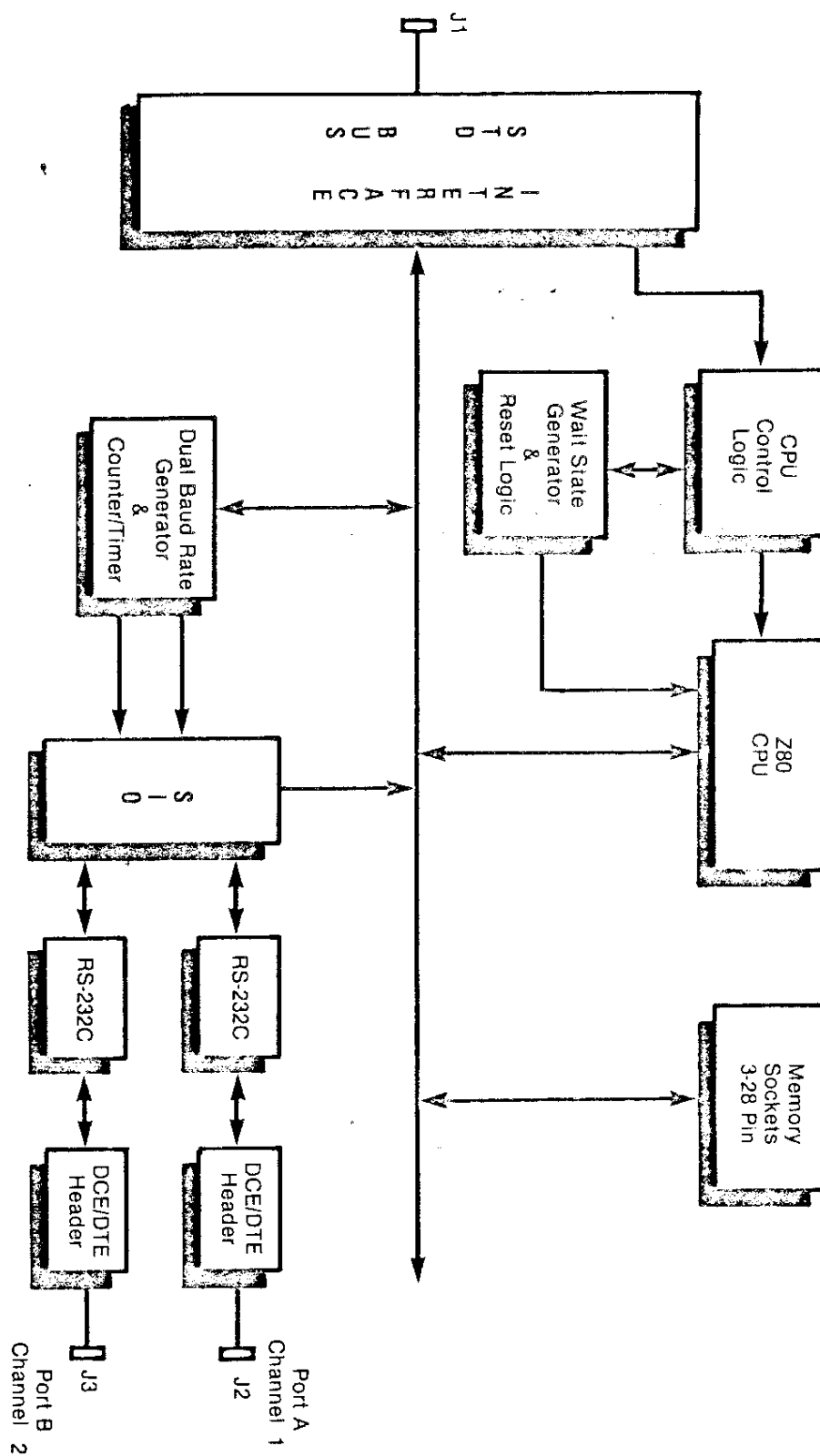


FIGURE 2 - 1 FUNCTIONAL BLOCK DIAGRAM

2.2.1 CPU

The Z80 is the system controller. It fetches, decodes and executes instructions from memory and generates the necessary address and control signals to co-ordinate data flow between the CPU and memory or between the CPU and system I/O devices.

2.2.2 Clock Generator

The DSTD-102 has a crystal controlled oscillator to generate the basic clock signals for the CPU and peripheral chips. A divide-by-two circuit ensures a 50% duty cycle and an active pullup circuit ensures proper clock levels. An inverted clock is supplied to the bus for use by other modules.

2.2.3 CTC (Counter/Circuit)

The Counter/Timer Circuit (MK3882/Z80-CTC) provides four independent, programmable channels for either software or hardware controlled counting and timing functions. Each channel can be configured by the CPU for various modes of operation and the built-in daisy chain priority interrupt logic provides for automatic, independent interrupt vectoring. The I/O port addresses for the CTC are hard-wired as follows:

I/O PORT ADDRESS	CTC CHANNEL
7C	0
7D	1
7E	2
7F	3

A strapping option has also been included to permit any or all of the four CTC channels to be cascaded for long count sequences.

Section 3 provides the necessary information for utilizing this option. For a complete description of the CTC operation, refer to either the Mostek MK3882 or Zilog Z80-CTC Technical Manual or Appendix A-15 of this manual.

2.2.4 Memory

The DSTD-102 has been designed to accommodate any combination of the byte-wide RAM, ROM and EPROM devices. Three 28-pin sockets have been provided, each of which may be strapped for any of the allowable memory types. These user-selectable options are fully described in Section 3.

2.2.5 Decode Logic

This section consists primarily of a PAL which decodes the high order six bits of memory address and generates the applicable chip select if on-board memory is to be selected. The PAL provides six separate memory configurations. The memory configurations are selected using an option jumper block as explained in Section 3.

The DSTD-102 has a latch to disable all on-board memory under software control. On power-up and reset, the latch is preset enabling the on board memory.

On-board memory is disabled by writing a '1' to I/O port 07BH. The on-board memory can be re-enabled by writing a '0' to port 07BH.

2.2.6 Reset Control Logic

This is a strapping option that causes a hardware-forced memory starting address upon system reset. A reset address of either 0000H or E000H may be selected.

This logic is required for use of standard MOSTEK hardware and software products including DDT-80, FLP-80DOS/MDX, MDX-SST, and MDX-DEBUG and dy-4 Debug Monitor (DDM) and CP/M software.

Also the push button reset function may be edge triggered or level sensitive depending on jumper block JB15. The edge triggered reset is synchronised with M1 to ensure that the contents of any dynamic RAM in the system are preserved during the reset process. The level sensitive option is required when it is necessary to hold the processor in a reset state indefinitely such as in a 'brown-out' situation.

2.2.7 Wait State Generator

This function, if enabled, causes memory read and write cycles to be lengthened by one clock period in order to allow sufficient access time when slower memory devices are used. Wait states can be enabled selectively, namely, - all memory cycles or opcode fetch cycles only or all memory cycles accessing on-board memory devices or all opcode fetch cycles and all memory cycles accessing onboard memory. An additional wait state may also be inserted during INTAK cycles.

2.2.8 Serial Ports

The DSTD-102 has two RS-232C serial ports implemented using the Z80-SIO/MK3884. Each port has a software programmable baud rate generator. The baud rate is set by writing to port 7AH. The least significant 4 bits set the baud rate for Channel A and the most significant 4 bits are for Channel B. Both Channels will operate from 50 baud to 19.2K baud. In addition the CTC may be used to generate the receive and transmit data clocks of Channel A allowing for non-standard baud rates. The CTC can only be used for asynchronous modes because it does not generate a 50% duty cycle clock. Channel A also has additional RS-232C drivers and receivers to enable it to handle external clocks for full synchronous operation (SDLC, HDLC, BYSYNC, MONOSYNC etc.).

SECTION 3

3.0 USER-SELECTABLE OPTIONS**3.1 Introduction**

The DSTD-102 incorporates many strapping options to provide the user with a high degree of flexibility in system configurations. This section describes the use of the available jumper options.

3.2 Debug/Single Step Configurations

The DSTD-102 supports the MDX-SST module. This module generates a NMI (non-maskable interrupt) and asserts the DEBUG signal. This debug signal when enabled forces a logic '1' onto the most significant three bits of the address bus. Thus the interrupt service routine is located at E066H. If the debug is disabled the interrupt service routine is at the normal address (0066H). To enable the debug line, install a jumper between JB8-2 and JB8-3 and between JB13-4A to JB13-4B. Ensure that the memory option strap position the monitor software at E000H. dy-4 SYSTEMS' DDM firmware supports the single step facilities.

3.3 Memory Options

The PAL memory decoder shipped with DSTD-102 from the factory supports the options discussed in the following sections.

3.3.1 Restart Address

The DSTD-102 is capable of starting execution at either 0000H or E000H after reset. Reset address E000H is implemented in hardware. Since the program counter (internal to the Z80 microprocessor) always resets to 0000H, external hardware is required to force the most significant three bits of the data bus to all ones to get 0E000H. A multiplexer and a latch to control the multiplexer are used to perform this function. The first instruction at E000H should be 'JMP E003' to set the processors internal program counter to the correct memory location. The hardware latch forcing the address bit must then be cleared. This is done automatically by the first I/O cycle that the processor performs. If no I/O port access is normally made then a dummy I/O read of an unused port address must be done otherwise memory accessed will be constrained to addresses E000H through FFFFH. To ensure proper operation after reset, the following code sequence should be placed in memory at the E000H.

E000	C3 03 E0	JP E003H	; jump instruction ; to update program counter
E003	DB nn	IN A,(nn)	; read unused I/O ; port nn to clear ; reset address latch
E005			; first instruction ; of user program

When using standard dy-4 SYSTEMS' or Mostek software (including DDM, DCM, DDT-80, FLP-80, DOS/MDX or MDX-DEBUG), the reset address must be E000H. The program counter and address latch modification instructions previously described are already contained with the DDM ROM. Ensure that pins 2 and 3 of JB8 are connected when the MDX-SST module is used.

3.3.2 Memory Configuration

The DSTD-102 incorporates three 28 pin sockets which can be independently configured to accept a variety of pin compatible memory devices. Table 3 - 1 lists each socket, its corresponding jumper block, and its address space for the standard configurations. The memory decoding is done using a PAL device. Table 3 - 2 shows for reference the signals brought to the jumper block for each of the different memory types. Table 3- 3 illustrates the necessary jumper connections for configuring a socket to accept each memory device.

Consult the factory for PAL programming details for non-standard requirements.

Option numbers are binary coded using JB14. JB14, 1A-1B has a weighting of '1'; JB14, 2A-2B has a weighting of '2' and JB14, 3A-3B has a weighting of '4'. For example, if option 5 (101) is desired JB14, 1A-1B, 3A-3B are left open and JB14, 2A-2B are inserted.

TABLE 3 - 1

MEMORY SOCKET/JUMPER BLOCK ASSIGNMENT

MEM TYPE	OPTION	MEM RANGE	U20(JB11)	U19(JB10)	U18(JB9)
2K	7(111)	E000-FFFF	E000-E7FF	E800-EFFF	F000-FFFF
2K	6(110)	0000-1FFF	0000-07FF	0800-0FFF	1000-1FFF
4K	5(101)	E000-FFFF	E000-EFFF	F000-FBFF	FC00-FFFF
4K	4(100)	0000-3FFF	0000-0FFF	1000-1FFF	2000-3FFF
8K	2(010)	0000-7FFF	0000-1FFF	2000-3FFF	4000-7FFF
16K	0(000)	0000-BFFF	0000-3FFF	4000-7FFF	8000-BFFF

NOTE: For 2K, 4K and 8K devices the memory range for U18 is twice as large as for U19 and U20. Hence when using the same memory device sizes for all three sockets, memory expansion off board will not be contiguous.

Option 5 is the memory configuration used for the boot proms and monitor in dy-4's STD Bus based microcomputer development systems.

TABLE 3 - 2

MEMORY DEVICE JUMPER STRAPS

TYPE	PART NO.	PINS				
		27	26	23	21	1
1Kx8 EPROM	2758	-	Vcc	Vpp	GND	-
1Kx8 EPROM	2759	-	Vcc	Vpp	Vcc	-
2Kx8 EPROM	2716	-	Vcc	Vpp	A10	-
4Kx8 EPROM	2732	-	Vcc	A11	A10	-
8Kx8 EPROM	2764	PGM	n/c	A11	A10	Vpp
16Kx8 EPROM	27128	PGM	A13	A11	A10	Vpp
1Kx8 RAM	4801	-	Vcc	/WE	GND	-
2Kx8 RAM	4802	-	Vcc	/WE	A10	-
8Kx8 RAM	2186	/WE	n/c	A11	A10	RDY
2Kx8 EEROM	X2816A	-	Vcc	/WE	A10	-

TABLE 3 - 3

MEMORY DEVICE JUMPER STRAPS

TYPE	PART NO.	JUMPER BLOCKS JB9 and JB12	JUMPER BLOCK JB10
1Kx8 EPROM	2758	B2-A6 ; A5-A6 B3-B4	A2-B4 ; B3-B4 C1-C2
1Kx8 EPROM	2759	B2-A6 ; A5-A6 B3-B2	A2-B4 ; B3-B4 C1-B3
2Kx8 EPROM	2716	B2-A6 ; A5-A6 B3-A3	A2-B4 ; B3-B4 B1-C1
4Kx8 EPROM	2732	B2-A6 ; A4-A5 B3-A3	A2-B4 ; B3-B2 B1-C1
8Kx8 EPROM	2764	B1-B5 ; A4-A5 B3-A3 ; A1-A6	A3-C3 ; B2-B3 B1-C1 ; A4-B4
16Kx8 EPROM	27128	B1-B5 ; A4-A5 B3-A3 ; A1-A6 B2-B6	A3-C3 ; B2-B3 B1-C1 ; A4-B4 C4-A2
1Kx8 RAM	4801	B2-A6 ; A5-B5 B3-A6	A2-B4 ; B3-C3 C1-C2
2Kx8 RAM	4802	B2-A6 ; A5-B5 B3-A3	A2-B4 ; B3-C3 B1-C1
8Kx8 RAM	2186	B1-B5 ; A4-A5 B3-A3 ; A1-A2	A3-C3 ; B2-B3 B1-C1 ; A1-A4
2Kx8 EEROM	X2816A	B2-A6 ; A5-B5 B3-A3	A2-B4 ; B3-C3 B1-C1

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ERRATA

Manual Change

Table 3-3

Change

2764 JB9,J12: Change B1-B5 to B1-A1
JB10 : Change A3-C3 to A3-A4

27128 JB9,J12: Change B1-B5 to B1-A1
JB10 : Change A3-C3 to A3-A4

3.3.3 On-board Memory Disable Latch

All on-board memory can be enabled and disabled under software control. To use this feature jumper JB14 4A-4B is installed. This jumper allows the memory disable latch to be used. The latch is located at address 7BH. Writing a '0' to this latch enables on-board memory. Writing a '1' to the latch disables on-board memory. A power-up or RESET clears the latch thus enabling on-board memory.

3.4 WAIT State Generator

Three jumpers are provided to allow the use of slow memory devices. The first jumper generates a WAIT state on all memory cycles. The second jumper generates a WAIT state for M1 memory cycles only. Table 3 - 4 lists the access times of memory devices internal and external to the card for the two different memory cycle types for both the 2.5 MHz and 4.0 MHz DSTD 102 cards. The third jumper generates a WAIT state on internal memory accesses only. This means that slower EPROMS can be used on the DSTD-102 along with a high speed RAM card. A fourth jumper allows the generation of a WAIT state on interrupt acknowledge cycles. Table 3 - 5 gives the connections for the WAIT state options.

TABLE 3 - 4A

M1-MEMORY CYCLE WAIT STATES TIMING 2.5MHz

FUNCTION	JB11 Connections	INTERNAL		EXTERNAL	
		M1	Other	M1	Other
No WAIT states	---	580	780	550	750
WAIT states on M1 cycles	1A to 1B	620	780	950	750
WAIT states on all memory cycles	3A to 3B	620	1180	950	1150

(in nanoseconds)

TABLE 3 - 4B

M1-MEMORY CYCLE WAIT STATES TIMING 4.0MHZ

FUNCTION	JB11 Connections	INTERNAL		EXTERNAL	
		M1	Other	M1	Other
No WAIT states	---	330	455	300	425
WAIT states on M1 cycle	1A to 1B	590	455	560	425
WAIT states on all memory cycles	3A to 3B	590	705	560	675

(in nanoseconds)

TABLE 3 - 5 WAIT STATE OPTIONS

OPTION	JB11
No WAIT states	No Jumpers
All M1 cycles	1A to 1B
All Memory cycles	3A to 3B
Internal Memory cycles only	4A to 4B
Internal Memory cycles and external M1 cycles	4A to 4B 1A to 1B
Interrupt acknowledge cycle	2A to 2B

3.5 Counter/Timer Options

The four Counter/Timer channels may be cascaded for extended counting and timer functions. Appendix A-6 shows the jumper pin numbers for the CTC. Refer to the MK3882 Technical Manual or the Zilog Data Book for a complete description of the CTC operation.

Provision is made on the Counter/Timer option block to enable the NMI input of the processor to be connected to one of the outputs of the CTC. NMI is pin 5A of JB5.

In addition the CTC can be used as a baud rate generator for the serial channels to create non-standard baud rates.

Two commonly unused pins on the STD bus (MEMEX and IOEXP) may be connected through JB13 and buffers to the CTC. One pin is used as an input (IOEXP) and the other is used as an output (MEMEX).

3.6 Serial Channel Options

3.6.1 Baud Rate Generator

The DSTD-102 has a dual software-programmable baud rate generator. It is accessed through I/O port 7AH. This port is a write-only port. Bits 0 to 3 control channel A and bits 4 to 7 control channel B. Table 3 - 7 shows the programming information for the baud rate generator.

Table 3 - 6

Baud Rate Generator Programming					
BAUD RATE	D3/D7	D2/D6	D1/D5	D0/D4	(HEX)
19,200	1	1	1	1	F
9,600	1	1	1	0	E
7,200	1	1	0	1	D
4,800	1	1	0	0	C
3,600	1	0	1	1	B
2,400	1	0	1	0	A
2,000	1	0	0	1	9
1,800	1	0	0	0	8
1,200	0	1	1	1	7
600	0	1	1	0	6
300	0	1	0	1	5
150	0	1	0	0	4
134.5	0	0	1	1	3
110	0	0	1	0	2
75	0	0	0	1	1
50	0	0	0	0	0

Thus to set port A to 9600 baud and port B to 1200 baud output a 7EH to I/O address 7AH.

3.6.2 DTE/DCE Configurations

3.6.2.1 DCE Configuration

When connecting to a CRT, printer or similar equipment the serial port is wired as Data Communications Equipment. The signal names indicate control and data flow with respect to the CRT. Table 3 - 7 itemizes the jumper configurations for this mode of operation.

TABLE 3 - 7

RS-232C DCE Jumper Configuration

EIA(DCE) Signal Name	SIO Function	Installed Jumpers JB3,JB4	J2/J3 Pin Numbers
TX (2)	RX	2B to 1B	2
RX (3)	TX	1A to 2A	3
RTS (4)	CTS	4A to 5A	4
CTS (5)	RTS	5B to 4B	5
DTR (20)	DCD	7A to 6B	9
DCD (8)	DTR	6A to 7B	8
DSR (6)	+12V	8A to 8B	6 (JB3 only)

3.6.2.2 DTE Configuration

When connecting to a MODEM or similar equipment the serial port is wired as Data Terminal Equipment. The signal names indicate control and data flow with respect to the DSTD-102. Table 3 - 8 itemizes the jumper configuration for the mode of operation.

TABLE 3 - 8

RS-232C DTE Jumper Configuration

EIA(DTE) Signal Name	SIO Function	Installed Jumpers JB3,JB4	J2/J3 Pin Numbers
TX (2)	TX	1A to 1B	2
RX (3)	RX	2B to 2A	3
RTS (4)	RTS	3A to 3B	4
CTS (5)	CTS	4A to 4B	5
DTR (20)	DTR	6A to 6B	9
DCD (8)	DCD	7A to 7B	8
DSR (6)		-----	6

3.6.3 Synchronous Operation

The DSTD-102A allows synchronous operation on Channel A. That is, additional RS-232C drivers and receivers are provided for interfacing external clocks. Two configurations are possible.

- i) The DCE provides both transmit and receive timing information. When the DSTD-102A is the DCE, two RS-232C drivers are required. When the DSTD-102A is the DTE two RS-232C receivers are required.
- ii) The DCE provides the transmit timing information and the DTE provides the receive timing information. The DSTD-102A provides the receive timing information. The DSTD-102 uses both the RS-232C driver and the RS-232C receiver.

Table 3 - 9 shows the jumpering required for each configuration. Note that the same drivers used for the external clocks are also used to drive the on-board TX and RX LED's. When these drivers are to be used for external clocking the LED's should be disconnected.

TABLE 3 - 9

DCE provides both clocks. DSTD-102A is the DCE

	JB2	JB3	J2	EIA
TX Clock	2A - 2B 1A - 2A	9A - 9B	10	15
RX Clock	3A - 4A 4A - 4B	11A - 11B	11	17

DCE provides both clocks. DSTD-102A is the DTE

	JB2	JB3	J2	EIA
TX Clock	1A - 1B	8A - 8B	10	15
RX Clock	3A - 3B	10A - 10B	11	17

DTE provides the transmit clock. DCE provides the receive clock. DSTD-102A is DCE.

	JB2	JB3	J2	EIA
TX Clock	1A - 2A 2A - 2B	9A - 9B	10	24
RX Clock	3A - 3B	10A - 10B	11	17

DTE provides the transmit clock, DCE provides the receive clock. DSTD-102A is DTE.

	JB2	JB3	J2	EIA
RX Clock	1A - 1B	8A - 8B	10	24
TX Clock	2A - 3A 4A - 4B	11A - 11B	11	17

Note that the clock names given above refer to data flow with respect to the DTE. EIA refers to the DB25 pin numbers assigned to these signals by the EIA RS-232C specifications.

Table 3-10 shows the cable connections to a standard RS-232C DB25S connector. Typically the cable is the same for both DCE and DTE systems with the configuration being determined by the on-based jumpers.

TABLE 3-10
SERIAL CABLE CONNECTIONS

J2/J3	RS232C/DB25S	EIA CIRCUIT
1	1	AA
2	2	BA
3	3	BB
4	4	CA
5	5	CB
6	6	CC
7	7	AB
8	8	CF
9	20	CD
10	15	DB
11	17	DD
12	19	--

NOTE: Pin 12 (DB25S pin 19) is included to accomodate some printers that use pin 19 for flow control.

SECTION 4

4.0 SPECIFICATIONS

4.1 Functional Specifications

4.1.1 Word Size

Instructions: 8, 16, 24, or 32 bits

Data: 8 bits

4.1.2 Cycle Time

Clock period (T state): 400 ns for DSTD-102-2.5
250 ns for DSTD-102-4.0

Instruction Cycle: Min. 4 T states
Max. 23 T states

4.1.3 Memory Capacity

Three 28 pin sockets are provided which may be populated with any mixture of the following devices:

2758 (1K x 8 EPROM)
2759 (1K x 8 EPROM)
2716 (2K x 8 EPROM)
2732 (4K x 8 EPROM)
2764 (8K x 8 EPROM)
27128 (16K x 8 EPROM)
MK 34000 (2K x 8 EPROM)
4118 (1K x 8 Static RAM)
4801 (1K x 8 Static RAM)
4802 (2K x 8 Static RAM)
2186 (8K X 8 Pseudo Static RAM)
X2816 (2K x 8 EEROM)

4.1.4 Memory Access Time

The time required to access on-board memory by external DMA controllers is 100 ns plus the access time of the memory device. This is defined as the time interval between the time that the memory address is valid on the STD-BUS and the time that the output data is valid on the STD-BUS.

4.1.5 I/O Addressing

The on-board I/O addressing is hard wired to the following port addresses:

PORT				ADDRESS
BAUD RATE GENERATOR				7A
ON-BOARD DISABLE LATCH				7B
CTC	CH	0		7C
CTC	CH	1		7D
CTC	CH	2		7E
CTC	CH	3		7F
SIO	CH	A	DATA	BC
SIO	CH	A	CONTROL	BD
SIO	CH	B	DATA	BE
SIO	CH	B	CONTROL	BF

4.1.6 I/O Capacity

The Z80 CPU utilizes the lower 8 bits of its address bus for I/O addressing to yield a total of 256 possible port addresses.

4.1.7 Interrupts

The CPU may be programmed to process interrupts in any of three different modes (mode 0, 1, or 2 as described in any Z80 Technical Manual). Mode 2 operation (vectored interrupts) is by far the most powerful and is compatible with dy-4 DSTD and MOSTEK MDX Series cards.

Multi-level interrupt processing is also possible with the Z80 CPU. The level of stacking is limited only by available memory space.

The DSTD-102 will also accept non-maskable interrupts which force a restart at location 0066H.

4.1.8 System Clock

DSTD-102-2.5	2.5MHz $\pm 0.05\%$
DSTD-102-4.0	4.0MHz $\pm 0.05\%$

4.2 Electrical Specification

4.2.1 STD Bus Interface

Bus Inputs: One 74LS load max.

Bus Outputs: $I_{OL} = 24 \text{ mA min. @ } V_{OL} = 0.5 \text{ Volts}$
 $I_{OH} = 15 \text{ mA min. @ } V_{OH} = 2.4 \text{ Volts}$

4.2.2 Serial Ports

Inputs: One 74LS load max.

Outputs: +/- 12V Current Limited to 10mA

4.2.3 Operating Temperature

0 Degrees C to 50 Degrees C
95% humidity non-condensing

4.2.4 Power Supply Requirements

+5V +/- 5% @ 1.2A

+12V +/- 5% @ 0.1A

-12V +/- 5% @ 0.1A

(excluding memory power requirements)

4.3 Mechanical Specifications**4.3.1 Card Dimensions**

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm)
long

0.48 in. (1.22 cm.) maximum height

0.062 in. (0.16 cm.) printed circuit board
thickness

4.3.2 STD Bus Edge Connector

56 pin Dual Readout; 0.125 in. centers

Mating Connector

Viking 3VH28/1CE5 (printed circuit)

Viking 3VH28/1CND5 (wire wrap)

Viking 3VH28/1CN5 (solder lug)

SPECIFICATIONS

DSTD-102

4.3.3 Serial Port Connector

12 Pin Dual Readout; 0.100 inch grid

Mating Connector

Amp 87631-8 (housing)

Amp 86016-2 (contact)
or equivalent

SECTION 5

5.0 FACTORY NOTICES

5.1 Factory Repair Service

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. **THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL.** Enclose a letter containing the following information with the returned circuit board:

Name, address and phone number of purchaser
Date and place of purchase
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

Service Department
dy-4 SYSTEMS INC.,
888 Lady Ellen Place, or
Ottawa, Ontario
K1Z 5M1, Canada

Service Department
dy-4 SYSTEMS INC.,
3582 Dubarry Rd.
Indianapolis, IN 46226

Securely package and mail the circuit board, prepaid and insured, to the same address.

5.2 Limited Warranty

dy-4 warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

NOTICE

The antistatic bag is provided for shipment of the dy-4 PC boards to prevent damage to the components due to electrostatic discharge. Failure to use this bag in shipment will **VOID** the warranty.

FACTORY NOTICES

DSTD-102

APPENDIX A
OPTION PROGRAMMING SUMMARY

APPENDIX A

OPTION PROGRAMMING SUMMARY

- 1 OPTIONAL JUMPER BLOCKS

The following is a list of the option Jumper Blocks on the STD-102 card.

JB1	LED connection
JB2	Serial Channel A Clock TTL Side
JB3	Serial Channel A DTE/DCE Configuration Block
JB4	Serial Channel B DTE/DCE Configuration Block
JB5	Counter Timer Jumper Block
JB6	LED Transmit
JB7	LED Receive
JB8	Restart Address Jumper Block
JB9	Memory Socket Configuration Block for U18
JB10	Memory Socket Configuration Block for U19
JB11	WAIT State Generator options
JB12	Memory Socket Configuration Block of U20
JB13	CTC/Bus Interface Jumper Block
JB14	On-board Memory Options
JB15	Reset Mode

A - 2 LED Connections (JB1)

These jumpers are installed to drive the LED's. Note the jumpers should not be installed if Serial Channel A is used in synchronous mode and is supplying the clocks to external equipment.

	A	B	
Driver 1	1	o----o	LED 1
Driver 2	2	o----o	LED 2
----			Indicates Factory Default

A - 3 Serial Channel A Clock Jumpers TTL Side (JB2)

This jumper block allows the selection of the Transmit and receive clocks for Channel A.

	A	B	
Transmit Clock (input)	1	o o	RS232 Clock Receiver 1
Internal Baud Rate Generator	2	o o	RS232 Clock Transmitter 1
Receiver Clock (input)	3	o o	RS232 Clock Receiver 2
Internal Baud Rate Generator	4	o o	RS232 Clock Transmitter 2
Receiver Clock (input)	5	o o	CTC output
Transmit Clock (input)	6	o o	CTC output

A - 4

Channel A DTE/DCE Configuration Block (JB3)

These jumpers allow the board to be configured as Data Terminal Equipment or Data Communications Equipment when used with a standard dy-4 SYSTEMS Cable. The signals given are those of the SIO device which is labelled as Data Terminal Equipment.

		A	B	
Transmit Data	1	o	o	Connector J2 Pin 2
Connector J2 Pin 3	2	o	o	Received Data
Request to Sent (RTS)	3	o	o	Connector J2 Pin 4
Clear to Send (CTS)	4	o	o	Connector J2 Pin 5
Connector J2 Pin 4	5	o	o	Request to Send (RTS)
Data Terminal Ready (DTR)	6	o	o	Connector J2 Pin 9
Data Carrier Detect (DCD)	7	o	o	Connector J2 Pin 8
RS-232C Receiver 1	8	o	o	Connector J2 Pin 10
RS-232C Transmit 1	9	o	o	Connector J2 Pin 10
RS-232C Receiver 2	10	o	o	Connector J2 Pin 11
RS-232C Transmit 2	11	o	o	Connector J2 Pin 11
+12 through 3k ohms	12	o--o		Connector J2 Pin 6

A - 5 Channel B DTE/DCE Configuration Block (JB4)

This jumper block allows the channel to be configured as Data Terminal Equipment or Data Communications Equipment.

	A	B	
Transmit Data	1	o o	Connector J2 Pin 2
Connector J2 Pin 3	2	o o	Received Data
Request to Send (RTS)	3	o o	Connector J2 Pin 4
Clear to Send (CTS)	4	o o	Connector J2 Pin 5
Connector J2 Pin 4	5	o o	Request to Send (RTS)
Data Terminal Ready (DTR)	6	o o	Connector J2 Pin 9
Data Carrier Detect (DCD)	7	o o	Connector J2 Pin 8
+12 through 3k ohms	8	o--o	Connector J2 Pin 6

A - 6 Counter Timer Jumper Block (JB5)

This jumper block allows the counter/timer channels to be cascaded for longer sequences. It also provides access to the auxiliary input and output buffers which are connected through JB12 to MEMEX and IOEXP bus signals. The SIO clock is used when the CRT is used as a baud rate generator.

	A	B	
Auxiliary Input	1	o o	SIO Clock
CTC Channel 0 input	2	o o	CTC Channel 0 zero detect
CTC Channel 1 Zero detect	3	o o	CTC Channel 1 input
CTC Channel 2 input	4	o o	CTC Channel 2 zero detect
Internal Non-Maskable Interrupt	5	o o	Auxiliary Output
CTC Channel 3 input	6	o o	N/C

A - 7 JB6/7 LED Blocks

These jumpers are installed to drive the LEDs. They should be removed when Channel A is operated in Synchronous mode.

	A	B	
TX Driver	o--o		LED Driver U7 (JB6)
RX Driver	o--o		LED Driver U6 (JB7)

A - 8 Restart Address Jumper Block JB8

Installing the jumper between pins 2 and 3 forces the restart address to E000H. Installing the jumper between pins 1 and 2 forces a restart address to 0000H.

JB8		
1	o	Force 0000H
2	o	Restart address control
3	o	Force E000H

A - 9 Memory Socket Configuration Blocks JB9, JB12

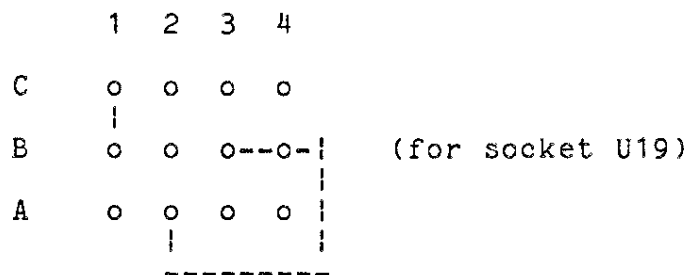
	JB9							JB12					
	1	2	3	4	5	6		1	2	3	4	5	6
B	o	o	o	o	o	o		B	o	o	o	o	o
A	o	o	o	o	o	o--		A	o	o	o	o	o--o--

for socket U18
(1K RAM)

for socket U20
(2K EPROM)

A1	Socket Pin 1	(pstatic RAM ready/Vpp)
B1	Socket Pin 27	(Pseudo static RAM /WE)
A2	Processor wait logic	
B2	Socket Pin 26	(Vcc/A13)

A3	Processor Address Bit A10
B3	Socket Pin 21 (A10/L)
A4	Processor Address Pin A11
B4	Ground
A5	Socket Pin 23 (A11/WE/Vpp)
B5	Processor Write Strobe
A6	+5V
B6	Processor Address Bit 13

A - 10**Memory Socket Configuration Block JB10**

A1	Processor wait logic
A2	Socket Pin 26 (Vcc/A13)
A3	Socket Pin 27 (Pseudo static RAM /WE)
A4	Socket Pin 1 (pstatic RAM ready/Vpp)
B1	Processor Address Bit A10
B2	Processor Address Pin A11
B3	Socket Pin 23 (A11/WE/Vpp)
B4	+5V
C1	Socket Pin 21 (A10/L)
C2	Ground
C3	Processor Write Strobe
C4	Processor Address Bit 13

A - 11 Wait State Generator Configuration Block JB11

	1	2	3	4
B	o	o	o	o
A	o	o	o	o

A1,B1	Wait on M1 cycles
A2,B2	Wait on Interrupt Acknowledge cycles
A3,B3	Wait on MREQ cycles
A4,B4	Wait on On-board Memory Cycles

A - 12 CTC/BUS Interface (JB13)

These jumpers are installed to allow counter/timer I/O to be accessed using two lines of the backplane that are not normally used by the Z80 STD bus cards. These signals use the BUS lines normally referred to as MEMEX and IOEXP. This jumper block also contains the Debug function enable jumper.

	A	B	
MEMEX (J1-36)	o	o	CTC Output
Ground	o	o	Ground
CTC Input	o	o	IOEXP (J1-35)
DEBUG (J1-38)	o--o		debug f/f

A - 13 On Board Memory Options (JB14)

Memory option weight '1', '2', and '4' selects the memory configuration for the DSTD-102. This jumper block is used in a binary coded fashion. See section 3.3.2 for details.

To use the on-board memory disable feature jumper 4A - 4B has to be installed. Port 7B can then be used to control the memory.

			A	B	
Memory Option 1	Weight '1'	1	o	o	Ground
Memory Option 2	Weight '2'	2	o	o	Ground
Memory Option 3	Weight '4'	3	o	o	Ground
DSMEN Latch Input		4	o--o		DSMEN Option Output

A - 14 Reset Mode (JB15)

Jumper JB15 is used to select the push button reset mode. The push button logic is edge sensitive if the jumper is omitted and is level sensitive if it is installed.

JB15

Push Button Input	o	o	Reset Logic
-------------------	---	---	-------------

A- 15 Programming The CTC**1) Channel Selection**

DSTD products using the Z80 CTC decode the CTC to occupy 4 contiguous port addresses. Writing to the appropriate port address will automatically select the correct register in the CTC.

2) Interrupt Vectors

If any one of the CTC channels is going to be used with its interrupt enabled, an Interrupt Vector must be written to the CTC. The user need only supply the 5 high bits of one vector as the CTC assumes the vector points to 4 contiguous byte pairs corresponding to the 4 channels. Note that D0 must equal 0 to indicate that the word being written to the CTC is an interrupt vector; this also requires vectored addresses to start at an even memory location.

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	X	X	0
<USER SUPPLIED VECTOR>					<SUPPLIED BY CTC>		

3) Channel Control Register

The control register bit functions are as illustrated below.

D7	D6	D5	D4	D3	D2	D1	D0
INT					LOAD		
ENA	MODE	RANGE	SLOPE	TRIG	TC	RESET	1

D0 = 0 indicates the byte is an INTERRUPT VECTOR.

D0 = 1 indicates the byte is a CONTROL WORD.

D1 = 0 the channel continues current operation.

D1 = 1 the channel is immediately RESET to control word values.

D2 = 0 indicates NO TIME CONSTANT to follow.

D2 = 1 the next I/O byte will be a TIME CONSTANT. (1 to 256)

D3 = 0 timer will FREE-RUN starting on next processor cycle.

D3 = 1 indicates timer will start on EXTERNAL TRIGGER.

D4 = 0 indicates external trigger on NEGATIVE-GOING edge.

D4 = 1 indicates external trigger on POSITIVE-GOING edge.

D5 = 0 indicates prescaler factor of 16. (timer mode only)

D5 = 1 indicates prescaler factor of 256. (timer mode only)

D6 = 0 indicates TIMER mode. (prescaler is enabled)

D6 = 1 indicates COUNTER mode. (prescaler disabled)

D7 = 0 INTERRUPT DISABLED for that channel.

D7 = 1 INTERRUPT on zero count ENABLED for the channel.

APPENDIX B

STD-Z80 BUS PIN OUT

APPENDIX B

STD-Z80 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	Ground - System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	
15	A7	Address Bus (Tri-state, output, active high).
16	A15	
17	A6	
18	A14	

STD-Z80 BUS PIN OUT

19	A5	A0-A15 make up a 16-bit address bus. The address bus provides the address for memory (up to 65k bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Memory Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Memory Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-State output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 Systems DSTD.

STD-Z80 BUS PIN OUT

36	/MEMEX	Memory expansion, not used on dy-4 Systems DSTD cards.
37	/REFRESH	/REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic zero and the upper 8 bits of the address bus contains the I register.
38	/DEBUG	/DEBUG (Input) used in conjunction with DDT-80 operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the /DEBUG line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
39	/M1	Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the opcode fetch cycle of an instruction. Note that during the execution of a 2-byte opcodes, /M1 will be generated as each opcode is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
40	STATUS 0	DMA priority chain input.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

STD-Z80 BUS PIN OUT

- 42 /BUSRQ Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.
- 43 /INTAK Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.
- 44 /INTRQ Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.
- 45 /WAITRQ WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

STD-280 BUS PIN OUT

46	/NMIRQ	Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will over-ride a /NMIRQ.
47	/SYSRESET	System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H and set Interrupt Mode 0.
48	/PBRESET	Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset.
49	/CLOCK	Processor Clock (Output, active low). Single phase system clock.
50	CNTRL	Auxiliary Timing
51	PCO	Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

STD-Z80 BUS PIN OUT

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.

APPENDIX C
DSTD-102 PARTS LIST

APPENDIX C

DSTD 102 PARTS LIST

DY4PART	QTY	DESCRIPTION	DESIGNATION
PT012008	1	74LS08 TTL-LS	U15
PT012014	1	74LS14 TTL-LS	U5
PT012020	1	74LS20 TTL-LS	U10
PT012074	2	74LS74 TTL-LS	U3,U14
PT012112	1	74LS112 TTL-LS	U11
PT012164	1	74LS164 TTL-LS	U4
PT012243	1	74LS243 TTL-LS	U27
PT012244	2	74LS244 TTL-LS	U28,U29
PT012245	3	74LS245 TTL-LS	U22,U24,U25
PT012257	1	74LS257 TTL-LS	U13
PT013074	1	74S74 TTL-S	U12
PT015009	1	MK3880n (280-CPU) 2.5 MHZ CPU	U17
PT015013	1	MK3882n (280-CTC) 2.5 MHZ CTC	U8
PT015017	1	MK3884n (280-SIO/0) 2.5 MHZ SIO/0	U16
PT016001	2	75188 OR MC1488 INTERFACE	U6,U7
PT016002	2	75189 OR MC1489 INTERFACE	U1,U2
PT036001	1	PAL12L6	U23
PT036002	2	PAL16L8	U9,U26
PT041101	1	1/4 WATT, 100 OHM, 5% RESISTOR	R12
PT041122	1	1/4 WATT, 1.2K OHM, 5% RESISTOR	R4
PT041220	1	1/4 WATT, 22 OHM, 5% RESISTOR	R6
PT041221	1	1/4 WATT, 220 OHM, 5% RESISTOR	R5
PT041302	2	1/4 WATT, 3K OHM, 5% RESISTOR	R1,R7
PT041472	2	1/4 WATT, 4.7K OHM, 5% RESISTOR	R2,R3
PT041473	1	1/4 WATT, 47K OHM, 5% RESISTOR	R10
PT041681	1	1/4 WATT, 680 OHM, 5% RESISTOR	R13
PT043012	2	8 PIN, 7 RESISTOR, 4.7K OHM, SIP RESISTOR NETWORK	RN2,RN3
PT043017	1	10 PIN, 9 RESISTOR, 4.7K OHM, SIP RESISTOR NETWORK	RN4
PT051004	1	034-55101 OR 035-56101, 100uf, RADIAL ELECTROLYTIC CAPACITOR	C35
PT052003	1	CK05BX330K, 33pf, 200V CERAMIC CAPACITOR	C2
PT052004	8	CK05BX331K, 330pf, 200V CERAMIC CAPACITOR	C6-13
PT052009	1	8131-100-25U-474M, .47uf, 50V, CERAMIC CAPACITOR	C3
PT052010	18	.1uf, 50V(.1 LD. SP.) 8121-050-25U-104M, CERAMIC CAPACITOR	C16,17,19,21-34,36
PT052013	1	.1uf, 50V (.2 LD. SP.) 8121-050-25U-104M) (102 BOARD ONLY)	C14
PT053000	1	TAG10M25, 10uf, 25V TANTALUM CAPACITOR	C18
PT061003	1	2N3906 TRANSISTOR	Q1
PT071000	1	1N4148 SIGNAL DIODE	D3
PT073001	2	1N4001 RECTIFIER	D1,D2
PT091000	1	HLMP6300 SMALL RED LED	LED2
PT091002	1	HLMP6500 SMALL GREEN LED	LED1
PT101000	1	K1135A CRYSTAL OSCILLATOR GENERATOR	U21
PT101005	1	K1116A 5.000 MHZ CRYSTAL OSCILLATOR	U30
PT111073	1	S208-1 CARD EJECTOR WITH PINS	
PT122003	3	CHD6960WIS 60 PIN DOUBLE ROW HEADER	JB1-JB5,JB9-JB15
PT122004	1	CHS6936WIS 36 PIN SINGLE ROW HEADER	JB6,JB7-JB10c,JB15
PT123003	2	87516-2 12 PIN RIGHT ANGLE CONNECTOR (AMP ONLY)	J2,J3
PT126020	3	640464-3 20 PIN I.C. SOCKET	U9,U23,U26
PT126028	4	640362-3 28 PIN I.C. SOCKET	U18-U20,U8
PT126040	2	640379-3 40 PIN I.C. SOCKET	U16,U17
PT344901	1	DSTD 102 DY00449-H-A1-6	
PT711003	1	102 MANUAL	

APPENDIX C

DSTD 102 PARTS LIST

QTY	PART	DESCRIPTION	DESIGNATION
1	PT012008	74LS08 TTL-LS	U15
1	PT012014	74LS14 TTL-LS	U5
1	PT012020	74LS20 TTL-LS	U10
2	PT012074	74LS74 TTL-LS	U3,U14
1	PT012112	74LS112 TTL-LS	U11
1	PT012164	74LS164 TTL-LS	U4
1	PT012243	74LS243 TTL-LS	U27
2	PT012244	74LS244 TTL-LS	U28,U29
3	PT012245	74LS245 TTL-LS	U22,U24,U25
1	PT012257	74LS257 TTL-LS	U13
1	PT013074	74S74 TTL-S	U12
1	PT015010	MK3880n-4 (280A-CPU) 4.00 MHZ CPU	U17
1	PT015014	MK3882n-4 (280A-CTC) 4.00 MHZ CTC	U8
1	PT015020	MK3884n-84 (280A-DART) 4.00 MHZ DART	U16
2	PT016001	75188 OR MC1488 INTERFACE	U6,U7
2	PT016002	75189 OR MC1489 INTERFACE	U1,U2
1	PT036001	PAL12L6	U23
2	PT036002	PAL16L8	U9,U26
1	PT041101	1/4 WATT, 100 OHM, 5% RESISTOR	R12
1	PT041122	1/4 WATT, 1.2K OHM, 5% RESISTOR	R4
1	PT041220	1/4 WATT, 22 OHM, 5% RESISTOR	R6
1	PT041221	1/4 WATT, 220 OHM, 5% RESISTOR	R5
2	PT041302	1/4 WATT, 3K OHM, 5% RESISTOR	R1,R7
2	PT041472	1/4 WATT, 4.7K OHM, 5% RESISTOR	R2,R3
1	PT041473	1/4 WATT, 47K OHM, 5% RESISTOR	R10
1	PT041681	1/4 WATT, 680 OHM, 5% RESISTOR	R13
2	PT043012	8 PIN, 7 RESISTOR, 4.7K OHM, SIP RESISTOR NETWORK	RN2,RN3
1	PT043017	10 PIN, 9 RESISTOR, 4.7K OHM, SIP RESISTOR NETWORK	RN4
1	PT051004	034-55101 OR 035-56101, 100uf, RADIAL ELECTROLYTIC CAPACITOR	C35
1	PT052003	CK05BX330K, 330pf, 200V CERAMIC CAPACITOR	C2
8	PT052004	CK05BX331K, 330pf, 200V CERAMIC CAPACITOR	C6-13
1	PT052009	8131-100-25U-474M, .47uf, 50V, CERAMIC CAPACITOR	C3
18	PT052010	.1uf, 50V(.1 LD, SP.) 8121-050-25U-104M, CERAMIC CAPACITOR	C16,17,19,21-34,36
1	PT052013	.1uf, 50V (.2 LD, SP.) 8121-050-25U-104M) (102 BOARD ONLY)	C14
1	PT053000	TAG10M25, 10uf, 25V TANTALUM CAPACITOR	C18
1	PT061003	2N3906 TRANSISTOR	Q1
1	PT071000	1N4148 SIGNAL DIODE	D3
2	PT073001	1N4001 RECTIFIER	D1,D2
1	PT091000	HLMP6300 SMALL RED LED	LED2
1	PT091001	HLMP6400 SMALL YELLOW LED	LED1
1	PT101000	K1135A BAUD RATE GENERATOR	U21
1	PT101007	K1116A 8.000 MHZ CRYSTAL OSCILLATOR	U30
1	PT111073	S208-1 CARD EJECTOR WITH PINS	
2	PT122003	CHD6960WIS 60 PIN DOUBLE ROW HEADER	JB1-JB5,JB9-JB15
1	PT122004	CHS6934WIS 36 PIN SINGLE ROW HEADER	JB6,JB7-JB10c,JB15
2	PT123003	87516-2 12 PIN RIGHT ANGLE CONNECTOR (AMP ONLY)	J2,J3
3	PT126020	640464-3 20 PIN I.C. SOCKET	U9,U23,U26
4	PT126028	640362-3 28 PIN I.C. SOCKET	U18-U20,U8
2	PT126040	640379-3 40 PIN I.C. SOCKET	U16,U17
1	PT344901	DSTD 102 DY00449-H-A1-7	
1	PT711003	102 MANUAL	

PARTS LIST

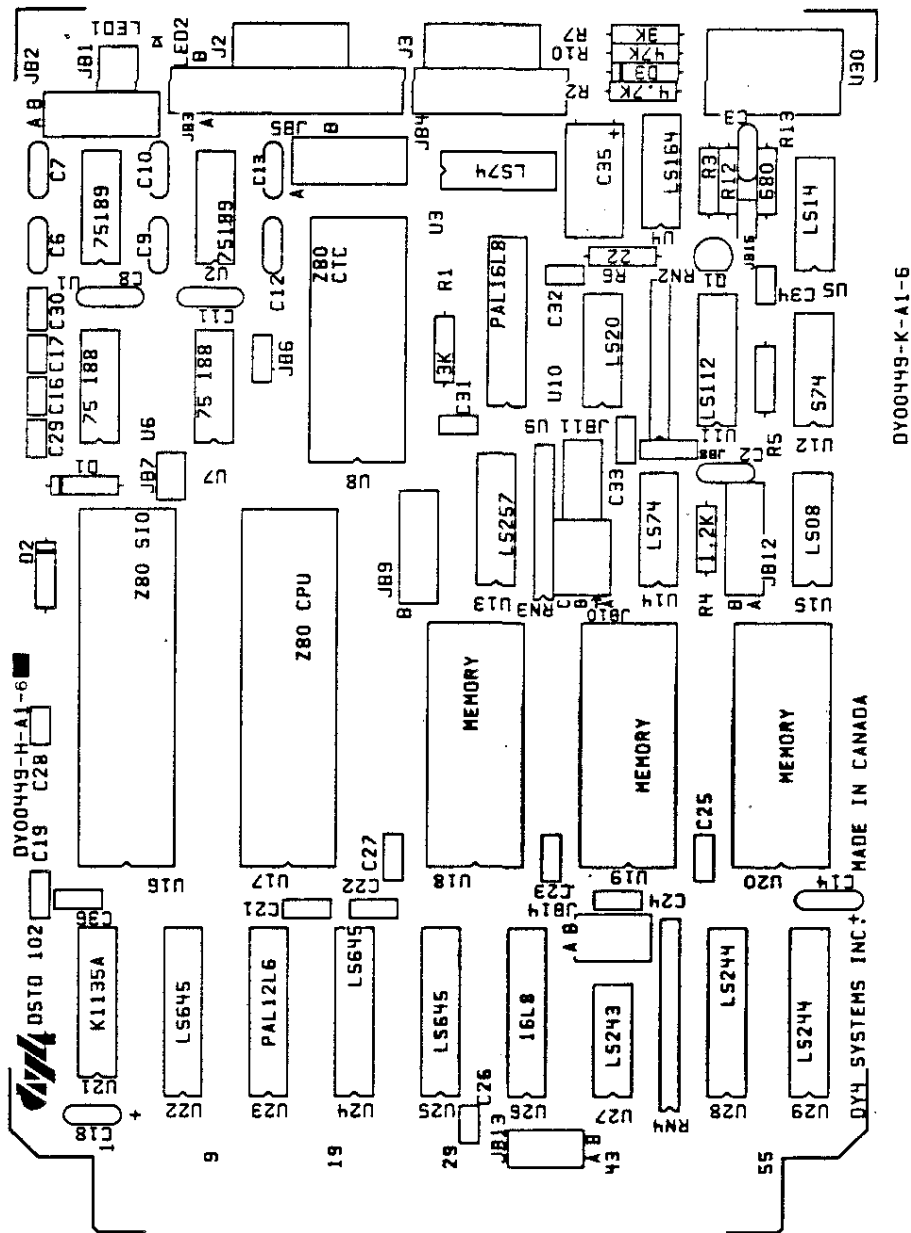


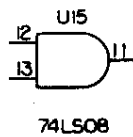
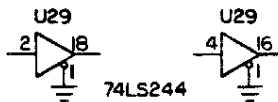
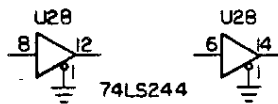
FIGURE C-1 DSTD-102-4 SILK SCREEN

APPENDIX D
SCHEMATIC

ISSUE	DESCRIPTION	DATE	DRN	CHK
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IC POWER PINS					
TYPE	+12	-12	+5	-5	GND
74LS08			14		7
74LS14			14		7
74LS20			14		7
74LS74			14		7
74S74			14		7
74LS112			16		8
74LS164			14		7
74LS243			14		7
74LS244			20		10
74LS257			16		8
74LS645			20		10
2716/2764			28		14
75188	14	1			7
75189			14		7
K1135A	9		2		11
PAL12L6			20		10
Z80 CTC			24		5
Z80 SIO			9		31
Z80 CPU			11		29
XTAL LOCOII			14		7

UNUSED GATES



DSTD 102			
SCALE	DRN D. NICHOLLS	CHK	DATE 4/11/82
APP'D	TOL	MAT'L	FINISH
TITLE DSTD 102 (POWER & GND. TABLE)			
DWG NO. DY00449-I-A1-6	ISS 6	SH 1	OF 3

