

DSTD-188 CPU AND SERIAL I/O

OPERATIONS MANUAL

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SECTION 1

1.0 GENERAL INFORMATION

1.1 Introduction

The dy-4 SYSTEMS' DSTD-188 CPU, Figure 1 - 1, is a 8088 based microcomputer board. It is designed to be compatible with both the Z80 and 8088 STD bus specifications. It features the 8088 CPU, the 8087 maths co-processor chip, two serial communications channels and two 28 pin memory sockets for byte-wide memory devices.

1.2 DSTD Series General Description

The DSTD series was designed to satisfy the need for low cost OEM microcomputer modules. The DSTD-Z80 and DSTD-8088 BUSSES uses a motherboard interconnect system concept. The modules for the STD bus are a compact 4.5 x 6.5 inches which provides for system partitioning by function, e.g. CPU, Memory, I/O, etc. This smaller module size makes system packaging easier, while increasing MOS-LSI densities provide high functionality per module.

1.3 DSTD-188 Features

- * Uses the 8088 microprocessor.
- * The 8087 maths co-processor may be installed as an option.
- * Provides two 28 pin sockets which may be strapped to accept any combination of the following industry standard memory devices.

EPROM	STATIC RAM
2716 (2kx8)	4802 (2kx8)
2732 (4kx8)	2186 (8kx8)
2764 (8kx8)	
27128 (16kx8)	

- * 2 serial RS-232C channels
- * Fully buffered signals for system expandability.

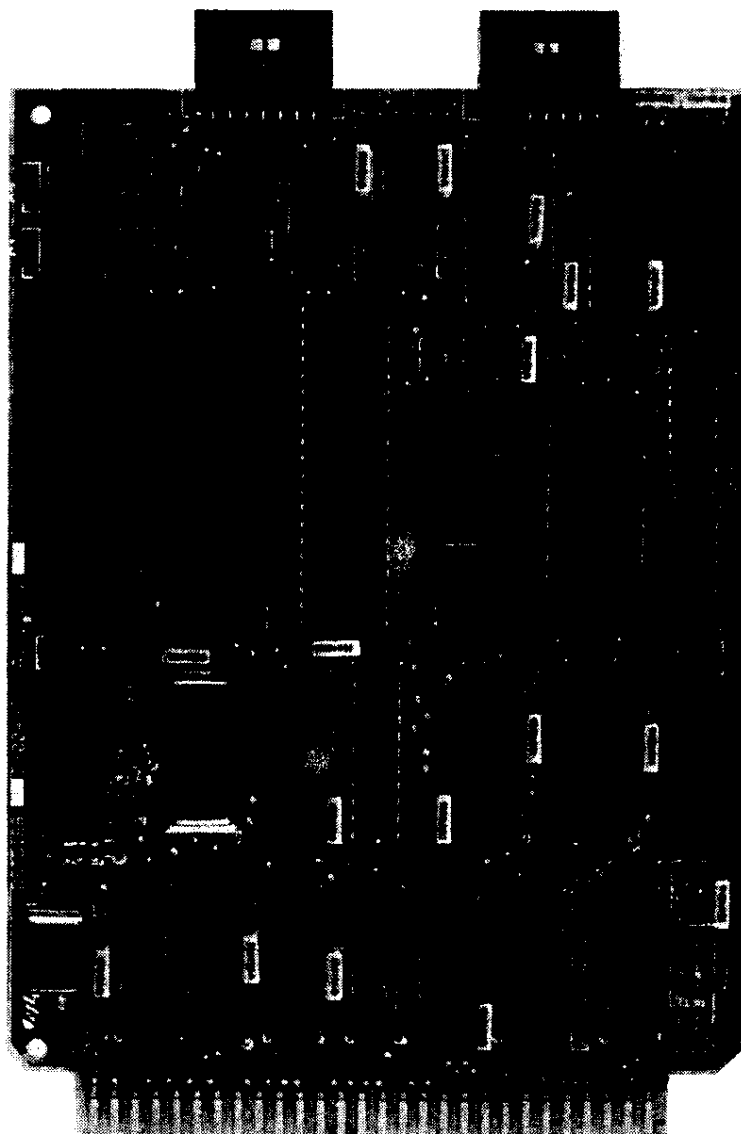


FIGURE 1 - 1 DSTD-188 MODULE

SECTION 2

2.0 FUNCTIONAL HARDWARE DESCRIPTION

2.1 Introduction

The DSTD-188 utilizes a 8088 microprocessor as the system controller. It features two 28 pin memory sockets which can be populated with any combination of designated RAM or EPROM and may be used as boot memory in disk based systems. The DSTD-188 also has a socket for the 8087 maths co-processor chip.

The DSTD-188 has two serial channels implemented using the 8274 LSI chip. This chip allows for asynchronous serial communication. Both channels will operate up to 19.2k baud.

The reset address is fixed at location FFFF0H. On power-up or system reset the on-board memory is enabled automatically. This feature is required for standard software and hardware products including dy-4 SYSTEMS Debug Monitor (DDM) and Disk Control Monitor (DCM) firmware products.

The DSTD-188 is available in 5.00 MHz and 8.0 MHz versions.

2.2 Block Diagram Description

Figure 2 - 1 is a block diagram illustrating the flow of system address, data and control signals on the DSTD-188. The following paragraphs describe the function of each of the major blocks.

2.2.1 CPU

The system controller is the 8088 CPU. It fetches, decodes and executes instructions from memory and generates the necessary address and control signals to co-ordinate data flow between the CPU and memory or between the CPU and system I/O devices.

2.2.2 Clock Generator

The DSTD-188 has a crystal controlled oscillator based on the 8284 to generate the basic clock signals for the CPU and peripheral chips. An inverted clock is supplied to the bus for use by other modules.

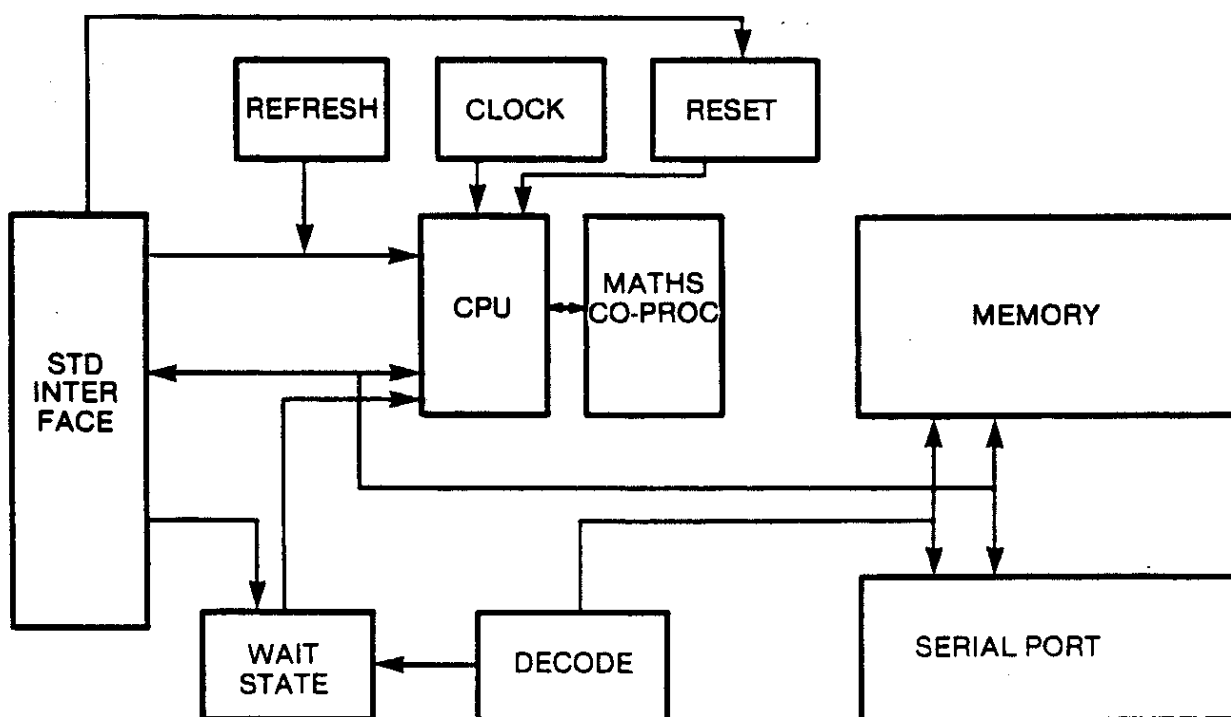


FIGURE 2 - 1 DSTD-188 FUNCTIONAL BLOCK DIAGRAM

2.2.3 Memory

The DSTD-188 has been designed to accommodate combinations of the byte-wide RAM, ROM and EPROM devices. Two 28-pin sockets have been provided, both of which may be strapped for any of the allowable memory types. These user-selectable options are fully described in Section 3.

2.2.4 Decode Logic

This section consists primarily of a PAL which decodes the high order eight bits of memory address and generates the applicable chip select if on-board memory is to be selected. The PAL provides for two separate memory configurations. The first places the first socket at location F8000H and the second socket at FC000H. The second configuration places the first socket at location 00000H and the second stays at location FC000H. The second configuration allows the 8088 interrupt vectors to be placed in on-board RAM. A strapping option must be hardwired to the desired configuration as explained in Section 3.

The DSTD-188 has a latch to disable all on-board memory under software control. On power-up and reset, the latch is preset enabling the on-board memory.

On-board memory is disabled by writing an '0' to I/O port 00BAH. The on-board memory can be re-enabled by writing a '1' to port 00BAH.

2.2.5 Reset Control Logic

Power-up reset is handled by the 8284 clock generator chip.

The push button reset (PBRESET) has two modes of operation, asynchronous and synchronous reset. The synchronous reset mode synchronizes the reset pulse with ALE and ensures that dynamic memory in the system will not be affected. The reset pulse is generated on the rising edge of PBRESET. In the asynchronous mode the processor reset line follows the level of the PBRESET line. This mode is used, for example when power brown-out detection logic is used and when the processor must remain inactive during periods of low power supply voltages.

2.2.6 Wait State Generator

This function, if enabled, causes memory read and write cycles to be lengthened by one clock period in order to allow sufficient access time when slower memory devices are used. Wait States can be enabled selectively, namely, - all memory cycles or all memory cycles accessing on-board memory devices. These options are

selected using JB7.

2.2.7 Serial Ports

The DSTD-188 has two RS-232C serial ports implemented using the Intel 8274. Each port has a software programmable baud rate generator. The baud rate is set by writing to port 00B9H. The least significant 4 bits set the baud rate for Channel A and the most significant 4 bits are for Channel B. Both Channels will operate from 50 baud to 19.2K baud. For 8274 programming and operation description refer to the INTEL Microprocessor and Peripheral Handbook.

2.2.8 Refresh Logic

The DSTD-188 has counters and logic to simulate the Z80 refresh cycles when the board is used in STD-Z80 mode. This logic generates a refresh cycle every 15 microseconds by putting the processor in HOLD mode and taking over the internal address bus. The refresh logic may be disabled when the DSTD-188 is operated in 8088 mode. (This assumes that any dynamic RAM in the system has its own memory refresh logic.)

2.2.9 Math Co-processor

The DSTD-188 is designed to accommodate the 8087 maths co-processor chip. The chip may be installed on the DSTD-188 as an option. For more information on the operation of the 8087 consult the Intel Microprocessor and Peripheral Handbook.

SECTION 3

3.0 USER-SELECTABLE OPTIONS

3.1 Introduction

The DSTD-188 incorporates many strapping options to provide the user with a high degree of flexibility in system configurations. This section describes the use of the available jumper options.

3.2 Z80 or 8088 Modes

The DSTD-188 is designed to operate in both Z80-STD and 8088-STD bus systems. A hardwire jumper (JB6) is used to select the mode of operation. Installing the jumper selects Z80 mode.

	o	Mode line
JB6	o	Ground

JB3 is also used when selecting the processor mode. Either install JB3 pins 2 to 3 when using the Z80 mode or install JB3 pins 2 to 1 when using 8088 mode. This jumper generates /S1 in 8088 mode and M1 in Z80 mode.

	1	2	3
JB3	o	o	o

pin 1	8088 /S1 signal
pin 2	driver input for P1 - 39
pin 3	Simulated M1 signal for Z80 peripherals

3.3 Memory Configuration

The DSTD-188 incorporates two 28 pin sockets which can be independently configured to accept a variety of pin compatible memory devices. Tables 3 - 1 shows the sockets, the corresponding jumper blocks, and the address space for the standard configurations. Table 3 - 2 illustrates the necessary jumper connections for configuring a socket to accept a particular memory device.

Non-standard memory configurations are available from the factory. Please consult the factory for more details.

Note that the two sockets, no matter what size of memory device is used they still occupy 16 Kbytes in the address space. This means that if a 2K device is used, it will be "repeated" 8 times within the 16 Kbyte address space. If a 4K memory device is used it will be "repeated" 4 times in the 16 kbyte address space. etc.

Thus the user can have contiguous memory (centered around location FC000H) using any combination of devices and still be able to handle the 8088 restart vector at FFFF0H.

TABLE 3 - 1

Memory Socket Addressing

DEVICE	SOCKET U12		SOCKET U11
	OPT 0 (JB11 installed)	OPT 1 (JB11 open)	OPT 0 & 1
2K	00000H - 007FFH	FB800H - FBFFFH	FC000H - FC7FFH
4K	00000H - 00FFFH	FB000H - FBFFFH	FC000H - FCFFFH
8K	00000H - 01FFFH	FA000H - FBFFFH	FC000H - FDFFFH
16K	00000H - 03FFFH	F8000H - FC000H	FC000H - FFFFFH

TABLE 3 - 2

Memory Device Jumper Straps

TYPE	PART NO.	PINS			JUMPERS
		26	23	1	
2Kx8 EPROM	2716	Vcc	Vpp	-	A3-B3 ; A1-B1
4Kx8 EPROM	2732	Vcc	A11	-	A3-B3 ; A2-B2
8Kx8 EPROM	2764	-	A11	Vpp	A2-B2 ; A3-A4
16Kx8 EPROM	27128	A13	A11	Vpp	B3-B4 ; A2-B2 A3-A4
32Kx8 EPROM	27256	A13	A11	A14	B3-B4 ; A2-B2 A4-A5
2Kx8 RAM	4802	Vcc	/WE	-	A3-B3 ; A1-A2
8Kx8 RAM	2186	-	A11	RDY	A2-B2 ; A4-B5
2Kx8 EEROM	X2816A	Vcc	/WE	-	A3-B3 ; A1-A2

JUMPER BLOCK LAYOUT FOR JB8,9

	A	B	
/WE	1	o o	n/c
socket pin 23	2	o o	Address bit 11
+5 volts	3	o o	Socket pin 26
socket pin 1 (RDY)	4	o o	Address bit 13
Address bit 14	5	o o	Processor ready (RRDY)

3.4 WAIT State Generator

A jumper block is provided to allow the use of slow memory devices. There are three modes. A jumper can be installed between JB7-2 and JB7-3 to generate WAIT STATES on all memory cycles or a jumper can be installed between JB7-2 and JB7-1 to generate WAIT STATES on on-board memory cycles only. This allows for example, high speed main memory with slower boot PROMs. With no jumpers installed no WAIT STATES are generated. Table 3 - 3 lists the access times of memory devices internal and external to the card for both the 5.0 MHz and 8.0 MHz DSTD-188 cards.

TABLE 3 - 3

Memory Cycle Timing With and Without WAIT States

FUNCTION	Connections (JB7)	INTERNAL		EXTERNAL	
		5.0	8.0	5.0	8.0
No WAIT States	---	400	250	370	220
WAIT States on-board memory	1 to 2	600	375	570	345
WAIT States on all memory cycles	2 to 3	600	375	570	345

(in nanoseconds)

3.5 Serial Channel Options

3.5.1 Baud Rate Generator

The DSTD-188 has a dual software-programmable baud rate generator. It is accessed through I/O port 00B8H (or 00B9H) This port is a write-only port. Bits 0 to 3 control channel A and bits 4 to 7 control channel B. Table 3 - 4 shows the programming information for the baud rate generator.

TABLE 3 - 4

Baud Rate Generator Programming

BAUD RATE	D3/D7	D2/D6	D1/D5	D0/D4	(HEX)
19,200	1	1	1	1	F
9,600	1	1	1	0	E
7,200	1	1	0	1	D
4,800	1	1	0	0	C
3,600	1	0	1	1	B
2,400	1	0	1	0	A
2,000	1	0	0	1	9
1,800	1	0	0	0	8
1,200	0	1	1	1	7
600	0	1	1	0	6
300	0	1	0	1	5
150	0	1	0	0	4
134.5	0	0	1	1	3
110	0	0	1	0	2
75	0	0	0	1	1
50	0	0	0	0	0

Thus to set port A to 9600 baud and port B to 1200 baud output a 7EH to I/O address 00B8H.

3.5.2 DTE/DCE Configurations

In addition to the transmit and receive data lines, the DSTD-188 supports some modem control lines. However due to board area constraints not all the modem control lines have been implemented. Channel A supports CTS and RTS. The RS-232C driver and receiver that are normally used for the RTS and CTS of Channel B are actually connected to jumpers blocks (JB2 and JB5) and arranged so that they can be used for the DCD and DTR signals of Channel A or the RTS and CTS signals of Channel B.

3.5.2.1 DCE Configuration

When connecting to a CRT, printer or similar equipment the serial port is wired as Data Communications Equipment. The signal names indicate control and data flow with respect to the CRT. Table 3 - 5 itemizes the jumper configurations for this mode of operation.

TABLE 3 - 5

RS-232C DCE Jumper Configuration Channel A

EIA Signal Name	Installed Jumpers JB1	Connector J2 Pin Numbers
TX	2B to 3B	2
RX	2A to 3A	3
RTS	4A to 5A	4
CTS	4B to 5B	5
DSR	1A to 1B	6
DCD	JB2-1B to 3B and JB5-2A to 1B	8
DTR	JB2-1A to 3A and JB5-3B to 1A	9

TABLE 3 - 6

RS-232C DCE Jumper Configuration Channel B

EIA Signal Name	Installed Jumpers JB5	Connector J3 Pin Numbers
TX	4B to 5B	2
RX	4A to 5A	3
DSR	6A to 6B	6
RTS	JB5-2B to 3B and JB2-3A to 4A	4
CTS	JB5-3A to 2A and JB2-3B to 4B	5

3.6.2.2 DTE Configuration

When connecting to a MODEM or similar equipment the serial port is wired as Data Terminal Equipment. The signal names indicate control and data flow with respect to the DSTD-188. Table 3 - 8 itemizes the jumper configuration for the mode of operation.

TABLE 3 - 7

RS-232C DTE Jumper Configuration Channel A

EIA Signal Name	Installed Jumpers JB1	Connector J2 Pin Numbers
TX	2A to 2B	2
RX	3A to 3B	3
RTS	4A to 4B	4
CTS	5A to 5B	5
DCD	JB2-1A to 3A and JB5-1B to 3B	8
DTR	JB2-1B to 3B and JB5-2A to 1A	9

TABLE 3 - 8

RS-232C DTE Jumper Configuration Channel B

EIA Signal Name	Installed Jumpers JBxx	Connector J3 Pin Numbers
TX	4A to 4B	2
RX	5A to 5B	3
RTS	JB2-3B to 4B and JB5-2A to 2B	4
CTS	JB2-3A to 4A and JB5-3A to 3B	5

Table 3-9 shows the cable connections to a standard RS-232C DB25S connector. Typically the cable is the same for both DCE and DTE systems with the configuration being determined by the on-based jumpers.

TABLE 3 - 9

Serial Cable Connections

J2/J3	RS232C/DB25S	EIA CIRCUIT
1	1	AA (GND)
2	2	BA (TX)
3	3	BB (RX)
4	4	CA (RTS)
5	5	CB (CTS)
6	6	CC (DSR)
7	7	AB (GND)
8 (Channel A only)	8	CF (DCD)
9 (Channel A only)	20	CD (DTR)
10,11,12,13,14	n/c	

3.7 8087 Request/Grant Option

The operation of the 8087 is such that it needs to take control of the processor bus from time to time as do other devices in an 8088 system. To do this the 8087 issues a bus 'Request' which will subsequently be 'Granted' by the processor. A priority chain is used to arbitrate between requesting devices. When the 8087 option is installed it must be included in the chain. If the option is not installed the socket must be excluded or bypassed. JB4 is used for this purpose.

Install JB4-1 to JB4-2 and JB4-3 to JB4-4 to include the 8087.
Install JB4-2 to JB4-3 to bypass the 8087 socket.

SECTION 4

4.0 SPECIFICATIONS

4.1 Functional Specifications

4.1.1 Word Size

Instructions: 8, 16, 24, or 32 bits

Data: 8 bits

4.1.2 Cycle Time

Clock period (T state): 200 ns for DSTD-188-5.0
125 ns for DSTD-188-8.0

4.1.3 Memory Capacity

Two 28 pin sockets are provided which may be populated with any mixture of the following devices:

2716 (2K x 8 EPROM)
2732 (4K x 8 EPROM)
2764 (8K x 8 EPROM)
27128 16K x 8 EPROM)
4802 (2K x 8 Static RAM)
2186 (8K x 8 RAM)

4.1.4 I/O Addressing

The on-board I/O addressing is hardwired to the following port addresses:

PORT	ADDRESS
BAUD RATE GENERATOR	00B8H
ON-BOARD MEMORY DISABLE LATCH	00BAH
SERIAL CH A DATA	00BCH
SERIAL CH A CONTROL	00BDH
SERIAL CH B DATA	00BEH
SERIAL CH B CONTROL	00BFH

Note. Do not use I/O addresses 00B9H and 00BBH

4.1.5 I/O Capacity

The 8088 CPU utilizes the lower 16 bits of its address bus for I/O addressing.

4.1.6 Interrupts

The DSTD-188 is designed to process mode 2 interrupts (as described in any Z80 Technical Manual). In this mode the interrupting device supplies the vector. The DSTD-188, however, does not simulate the Z80 'RETI' instruction which is used by the Z80 peripheral chips to reset their interrupt logic at the end of the interrupt service routine. This only really affects the CTC device because the other devices can be reset under software control. Thus the DSTD-188 will not support Z80-CTC in an interrupt mode of operation.

Multi-level interrupt processing is also possible with the Z80 CPU. The level of stacking is limited only by available memory space.

The DSTD-188 will also accept non-maskable interrupts which force a restart at location 00008H.

4.1.7 System Clock

DSTD-188-5.0 5.0MHz + 0.05%

DSTD-188-8.0 8.0MHz + 0.05%

4.2 Electrical Specification

4.2.1 STD Bus Interface

Bus Inputs: One 74LS load max.

Bus Outputs: $I_{OL} = 24 \text{ mA min. @ } V_{OL} = 0.5 \text{ Volts}$
 $I_{OH} = 15 \text{ mA min. @ } V_{OH} = 2.4 \text{ Volts}$

4.2.2 Serial Ports

Inputs: One 74LS load max.

Outputs: +/- 12V Current Limited to 10mA

4.2.3 Operating Temperature

0 Degrees C to 50 Degrees C

95% humidity non-condensing

4.2.4 Power Supply Requirements

+5V +/- 5% @ 2.0A

+12V +/- 5% @ 0.1A

-12V +/- 5% @ 0.1A

(excluding memory power requirements)

4.3 Mechanical Specifications

4.3.1 Card Dimensions

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm) long

0.48 in. (1.22 cm.) maximum height

0.062 in. (0.16 cm.) printed circuit board thickness

4.3.2 STD Bus Edge Connector

56 pin Dual Readout; 0.125 in. centers

Mating Connector

Viking 3VH28/1CE5 (printed circuit)

Viking 3VH28/1CND5 (wire wrap)

Viking 3VH28/1CN5 (solder lug)

4.3.3 Serial Port Connector

14 Pin Dual Readout; 0.100 inch grid

Mating Connector

Amp 3-87977-2 (housing)

Amp 86016-2 (contact)

or equivalent

SECTION 5

5.0 FACTORY NOTICES

5.1 Factory Repair Service

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. **THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL.** Enclose a letter containing the following information with the returned circuit board:

Name, address and phone number of purchaser
Date and place of purchase
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

Service Department,
dy-4 SYSTEMS INC.
888 Lady Ellen Place or
Ottawa, Ontario
K1Z 5M1 Canada

Service Department,
dy-4 SYSTEMS INC.
3582 Dubarry Rd.
Indianapolis, IN 46226

Securely package and mail the circuit board, prepaid and insured, to the same address.

5.2 Limited Warranty

dy-4 warrants this product against defective materials and workmanship for a period of 1 year. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative. There are no warranties which extend beyond those herein specifically given.

NOTICE

The antistatic bag is provided for shipment of the dy-4 PC boards to prevent damage to the components due to electrostatic discharge.

Failure to use this bag in shipment will VOID the warranty.

APPENDIX A
OPTION PROGRAMMING SUMMARY

APPENDIX A

OPTION PROGRAMMING SUMMARY

A - 1 OPTIONAL JUMPER BLOCKS

The following is a list of the option Jumper Blocks on the STD-188 card.

JB1	Serial Channel A DTE/DCE Configuration Block
JB2	Channel A DTR/DCD vs Channel B RTS/CTS (TTL side)
JB3	Z80 /M1 vs 8088 /S1 Selection Jumper Block
JB4	8087 Bus Request/Grant Block
JB5	Serial Channel B DTE/DCE Configuration Block
JB6	STD-Z80 / STD 8088 Mode Jumper Block
JB7	WAIT State Generator Jumper Block
JB8	Memory Socket Configuration Block for U11
JB9	Memory Socket Configuration Block of U12
JB10	Reset Mode Jumper Block
JB11	On-board Memory Option

A - 2 Serial Channel A DTE/DCE Configuration Block (JB1)

These jumpers allow the board to be configured as Data Terminal Equipment or Data Communications Equipment when used with a standard dy-4 SYSTEMS Cable.

B	o	o---o	o	o	JB1
A	o	o---o	o	o	
	1	2	3	4	5

A - 1 +12 volts through 3k ohms
 B - 1 Connector J2 Pin 6
 A - 2 Transmit Data
 B - 2 Connector J2 Pin 2
 A - 3 Connector J2 Pin 3
 B - 3 Receive Data
 A - 4 Request To Send
 B - 4 Connector J2 Pin 4
 A - 5 Connector J2 Pin 5
 B - 5 Clear To Send (CTS)

A - 3 Channel A DTR/DCD vs Channel B RTS/CTS (TTL side)

JB2	B	o	o	o	o	o
	A	o	o	o	o	o
		1	2	3	4	5

A - 1 Channel A DCD input (8274)
 B - 1 Channel a DTR output (8274)
 A - 2 Ground
 B - 2 +5 volts
 A - 3 RS-232C receiver output
 B - 3 RS-232C driver input
 A - 4 Channel B CTS output (8274)
 B - 4 Channel B RTS input (8274)
 A - 5 Channel B DCD input (8274)
 B - 5 Channel B DTR output (8274)

A - 4 Z80 /M1 vs 8088 /S1 Selection Jumper Block (JB3)

	1	2	3
JB3	o	o	o

pin 1 8088 /S1 signal

pin 2 driver input for P1 - 39

pin 3 Simulated M1 signal for Z80 peripherals

A - 5 8087 Bus Request/Grant Block (JB4)

JB4	1	2	3	4
	o	o---o		o

A - 6 Channel B DTE/DCE Configuration Block (JB5)

		A	B	
Connector J2 pin 9	1	o	o	Connector J2 pin 8
RS-232C Driver Output	2	o	o	Connector J3 pin 4
Connector J3 pin 5	3	o	o	RS-232C Receiver Input
RS-232C Driver Output	4	o	o	Connector J3 pin 2
Connector J3 pin 3	5	o	o	RS-232C Receiver Input
+12 volts thru 3 Kohms	6	o	o	Connector J3 pin 6

A - 7 STD-Z80 / STD 8088 Mode Jumper Block (JB6)

	o	Mode line
JB6	!	
	o	Ground

A - 8 WAIT State Generator Jumper Block (JB7)

1	o	On-board Memory Decoder Output
2	o	WAIT State Circuit Input
	!	
3	o	Ground

A - 9 Memory Socket Configuration Block (JB8,9)

	A	B	
/WE	1	o o	n/c
socket pin 23	2	o--o	Address bit 11
+5 volts	3	o--o	Socket pin 26
socket pin 1 (RDY)	4	o o	Address bit 13
Address bit 14	5	o o	Processor ready (RRDY)

(Shown Wrapped for 2732 EPROM)

A - 10 Reset Mode Jumper Block (JB10)

1	o	Push Button Input
2	o	Sync Reset Circuit

A - 11 On-board Memory Option (JB11)

o	o	JB11
1	2	

Pin 1 Decoder Input

Pin 2 Ground

APPENDIX B

STD-Z80/STD-8088 BUS PIN OUT

APPENDIX B

STD-Z80/STD-8088 BUS P \bar{I} N OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices A16-A19 are multiplexed in D0-D3 during ALE
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	
15	A7	Address Bus (output, active high). A0-A15 make up a 16-bit address bus. The address bus along with the multiplexed Address on the data bus provides for 1 Megabyte of memory. I/O addressing uses these same 16 address bits to allow the user to directly select up to 65K input or 65K output ports. A0 is the least significant address bit. During refresh time, the lower 8 bits contain a valid refresh address for dynamic memories in the system.
16	A15	
17	A6	
18	A14	
19	A5	
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Memory Write (output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

STD-Z80/STD-8088 BUS PIN OUT

- | | | |
|----|-----------|---|
| 32 | /RD | Memory Read (output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus. |
| 33 | /IORQ | Input/Output Request (output, active low).
In Z80 mode the /IORQ signal indicates that the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
In 8088 mode this pin contains the 8088 status signal '/S2'. |
| 34 | ./MEMRQ | Memory Request (output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation. |
| 35 | /IOEXP | I/O expansion, not used on dy-4 SYSTEMS DSTD. |
| 36 | /MEMEX | Memory expansion, not used on dy-4 SYSTEMS DSTD cards. |
| 37 | /REFRESH | /REFRESH (output, active low). /REFRESH indicates that the lower 8 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A8-A15 are not defined. |
| 38 | /MCSYNC | MEMORY CYCLE SYNC (OUTPUT, active low) This pin contains /ADDRESS LATCH ENABLE (ALE) from the 8088 processor. It signals to the bus that D0-D3 contains A16-A19. |
| 39 | /STATUS 1 | In Z80 mode:
Machine Cycle One (output, active low). /M1 occurs with /IORQ to indicate an interrupt acknowledge cycle. |

STD-Z80/STD-8088 BUS PIN OUT

In 8088 mode:

Status 1 (output, active low). This pin contains the 8088 status signal '/S1'.

40 /STATUS 0

Status 0 (output, active low). This pin contains the 8088 status signal '/S0'.

41 /BUSAK

Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

42 /BUSRQ

Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.

43 /INTAK

Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.

44 /INTRQ

Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop is enabled and if the /BUSRQ signal is not active. In Z80 mode, when the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.

45 /WAITRQ

WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to

enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

- | | | |
|----|-----------|--|
| 46 | /NMIRQ | Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 00008H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will override a /NMIRQ. |
| 47 | /SYSRESET | System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to OFFF0H. |
| 48 | /PBRESET | Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset. |
| 49 | /CLOCK | Bus Clock (Output, active low). Single phase system clock. This clock runs at one half processor clock rate. |
| 50 | CNTRL | Auxiliary Timing |
| 51 | PCO | Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine. |

STD-Z80/STD-8088 BUS PIN OUT

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.

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APPENDIX C
DSTD-188 PARTS LIST

APPENDIX C

DSTD-188 PARTS LIST

DY4PART	QTY	DESCRIPTION	DESIGNATION
PT012005	1	74LS05 TTL-LS	U4
PT012074	2	74LS74 TTL-LS	U3,U14
PT012164	1	74LS164 TTL-LS	U13
PT012240	1	74LS240 TTL-LS	U20
PT012244	1	74LS244 TTL-LS	U27
PT012245	3	74LS245 TTL-LS	U22,U24,U25
PT012373	1	74LS373 TTL-LS	U23
PT015030	1	P8274 USART OR NEC 7201 (PLASTIC ONLY)	U8
PT015032	1	P8284A XTAL OSCILLATOR	U15
PT015035	1	8288 BUS ORBITOR	U20
PT015039	1	8088 CPU	U9
PT016001	1	75188 OR MC1488 INTERFACE	U2
PT016002	1	75189 OR MC1489 INTERFACE	U1
PT036000	1	PAL16R4	U17
PT036001	1	PAL12L6	U5
PT036002	2	PAL16L8	U18,U19
PT036003	4	PAL16R8	U6,U7,U21,U26
PT041103	1	1/4 WATT, 10K OHM, 5% RESISTOR	R8
PT041104	1	1/4 WATT, 100K OHM, 5% RESISTOR	R4
PT041302	2	1/4 WATT, 3K OHM, 5% RESISTOR	R1,R2
PT041471	4	1/4 WATT, 470 OHM, 5% RESISTOR	R3,R5,R6,R7
PT043016	1	10 PIN, 9 RESISTOR, 1K OHM, SIP RESISTOR NETWORK	RN3
PT043017	2	10 PIN, 9 RESISTOR, 4.7K OHM, SIP RESISTOR NETWORK	RN1,RN2
PT052004	8	CK05BX331K,330pf, 200V CERAMIC CAPACITOR	C1-C8
PT052009	1	8131-100-Z5U-474M, .47uf, 50V, CERAMIC CAPACITOR	C34
PT052010	5	.1uf, 50V,(.1 LD. SP.) 8121-050-Z5U-104M, CERAMIC CAPACITOR	C17,C18,C19,C20,C23
PT053000	2	TA610M25, 10uf, 25V TANTALUM CAPACITOR	C24,C30
PT059000	19	.1uf 63V,(.2 LD. SP.)1R67104M,POLYESTER FILM CAPACITOR	C9-16,21,22,25-29,31-33,35
PT071000	1	1N4148 SIGNAL DIODE	D2
PT073001	2	1N4001 RECTIFIER	D1,D3
PT101000	1	K1135A BAUD RATE GENERATOR	U16
PT102009	1	FOX 150 15 MHZ DISCRETE CRYSTAL	Y1
PT111073	1	S208-1 CARD EJECTOR WITH PINS	
PT122003	3	CHD6960WIS 60 PIN DOUBLE ROW HEADER	JB1,JB2,JB5,JB8,JB9
PT122004	2	CHS6936WIS 36 PIN SINGLE ROW HEADER	JB3,JB4,JB6,JB7,JB10,JB11
PT123004	2	87516-3 14 PIN RIGHT ANGLE CONNECTOR (AMP ONLY)	J2,J3
PT126018	1	640359-3 18 PIN I.C. SOCKET	U15
PT126020	9	640464-3 20 PIN I.C. SOCKET	U5,6,7,17,18,19,20,21,26
PT126028	2	640362-3 28 PIN I.C. SOCKET	U11,U12
PT126040	3	640379-3 40 PIN I.C. SOCKET	U8,U9,U10
PT349201	1	DSTD 188 DY00492-H-A1-1	
PT711032	1	188 MANUAL	

APPENDIX C

DSTD-188 PARTS LIST

DY4PART	QTY	DESCRIPTION	DESIGNATION
PT012005	1	74LS05 TTL-LS	U4
PT012074	2	74LS74 TTL-LS	U3,U14
PT012164	1	74LS164 TTL-LS	U13
PT012240	1	74LS240 TTL-LS	U28
PT012244	1	74LS244 TTL-LS	U27
PT012245	3	74LS245 TTL-LS	U22,U24,U25
PT012373	1	74LS373 TTL-LS	U23
PT015030	1	P8274 USART OR NEC 7201 (PLASTIC ONLY)	U8
PT015032	1	P8284A XTAL OSCILLATOR	U15
PT015035	1	8288 BUS ORBITOR	U20
PT015040	1	8088-2 CPU	U9
PT016001	1	75188 OR MC1488 INTERFACE	U2
PT016002	1	75189 OR MC1489 INTERFACE	U1
PT036000	1	PAL16R4	U17
PT036001	1	PAL12L6	U5
PT036002	2	PAL16L8	U18,U19
PT036003	4	PAL16R8	U6,U7,U21,U26
PT041103	1	1/4 WATT, 10K OHM, 5% RESISTOR	R8
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PT041471	4	1/4 WATT, 470 OHM, 5% RESISTOR	R3,R5,R6,R7
PT043016	1	10 PIN, 9 RESISTOR, 1K OHM, SIP RESISTOR NETWORK	RN3
PT043017	2	10 PIN, 9 RESISTOR, 4.7K OHM, SIP RESISTOR NETWORK	RN1,RN2
PT052004	8	CK058X331K,330pf, 200V CERAMIC CAPACITOR	C1-C8
PT052009	1	8131-100-25U-474M, .47uf, 50V, CERAMIC CAPACITOR	C34
PT052010	5	.1uf, 50V(.1 LD. SP.) 8121-050-25U-104M, CERAMIC CAPACITOR	C17,C18,C19,C20,C23
PT053000	2	TAG10M25, 10uf, 25V TANTALUM CAPACITOR	C24,C30
PT059000	19	.1uf 63V(.2 LD. SP.)1R67104M,POLYESTER FILM CAPACITOR	C9-16,21,22,25-29,31-33,35
PT071000	1	1N4148 SIGNAL DIODE	D2
PT073001	2	1N4001 RECTIFIER	D1,D3
PT101000	1	K1135A BAUD RATE GENERATOR	U16
PT102010	1	FOX 24.00 MHZ DISCRETE CRYSTAL (FUNDAMENTAL)	Y1
PT111073	1	S208-1 CARD EJECTOR WITH PINS	
PT122003	3	CHD6940WIS 60 PIN DOUBLE ROW HEADER	JB1,JB2,JB5,JB8,JB9
PT122004	2	CHS6936WIS 36 PIN SINGLE ROW HEADER	JB3,JB4,JB6,JB7,JB10,JB11
PT123004	2	87516-3 14 PIN RIGHT ANGLE CONNECTOR (AMP ONLY)	J2,J3
PT126018	1	640359-3 18 PIN I.C. SOCKET	U15
PT126020	9	640464-3 20 PIN I.C. SOCKET	U5,6,7,17,18,19,20,21,26
PT126028	2	640362-3 28 PIN I.C. SOCKET	U11,U12
PT126040	3	640379-3 40 PIN I.C. SOCKET	U8,U9,U10
PT349201	1	DSTD 188 DY00492-H-A1-1	
PT711032	1	188 MANUAL	

PARTS LIST

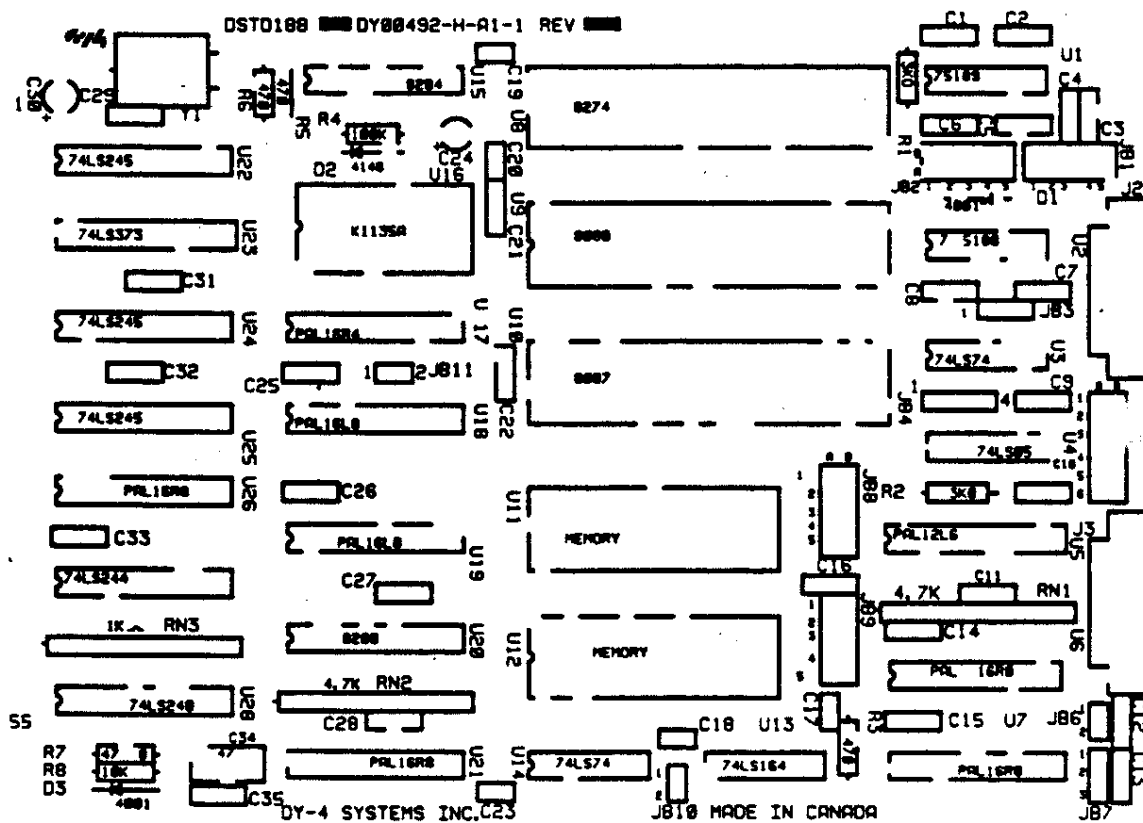


FIGURE C-1 DSTD-188-4 SILK SCREEN

APPENDIX D
SCHEMATIC

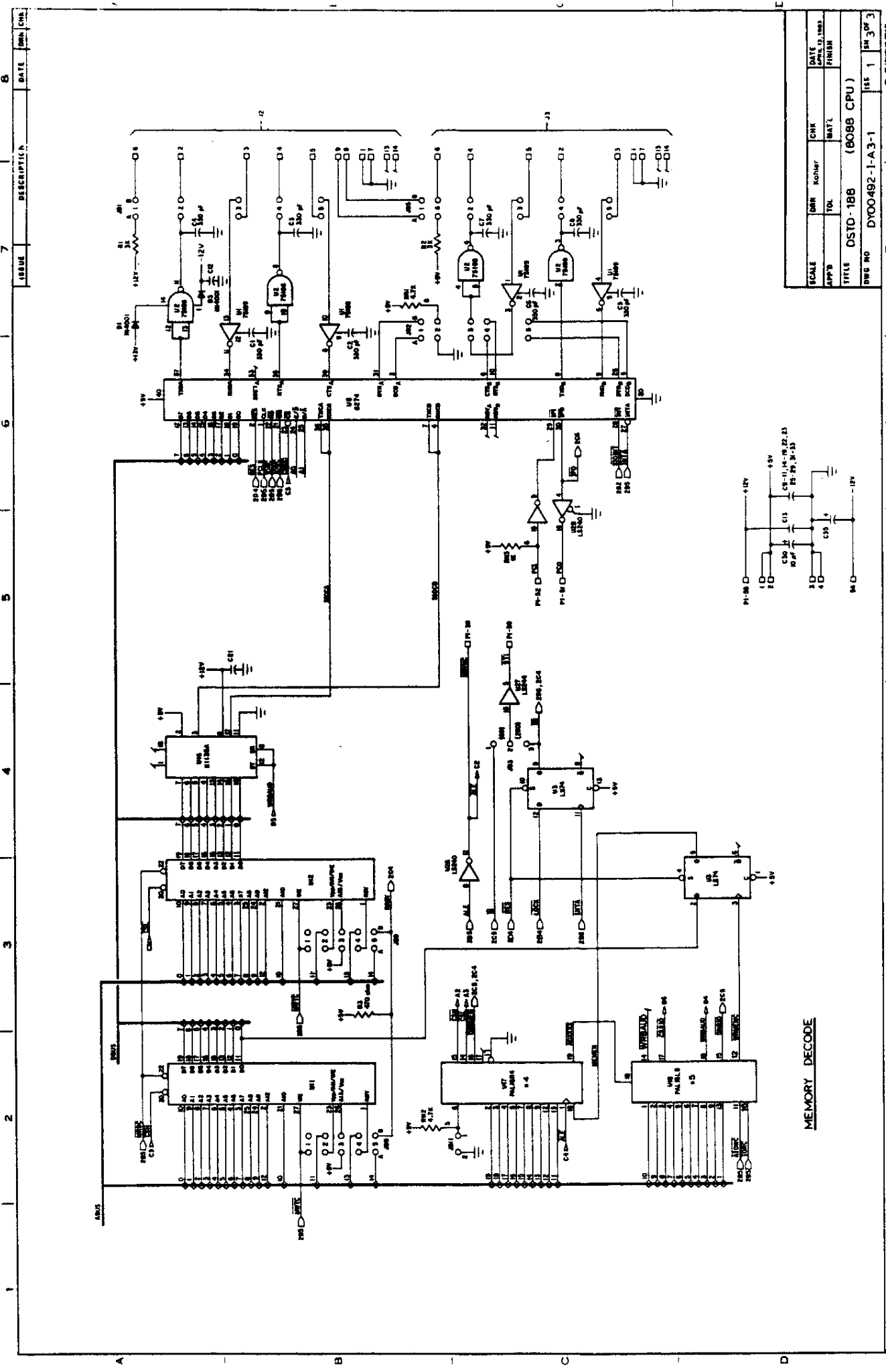
ISSUE	DESCRIPTION	DATE	DRN	CHK
-------	-------------	------	-----	-----

IC POWER PINS					
TYPE	+12	-12	+5	-5	GND
73188			14		7
73188					7
K1135A	9		2		11
PAL12L6			20		10
PAL16L8			20		10
PAL16R8			20		10
PAL16R4			20		10
74LS74			14		7
74LS244			20		10
74LS240			20		10
74LS05			14		7
74LS164			14		7
74LS245			20		10
74LS373			20		10
8274			40		20
8067			40		1,20
8288			20		10
8284			18		9
8088			40		1,20

UNUSED GATES



SCALE	DRN Köhler	CHK	DATE APRIL 13, 1982
APP'D	TOL	MAT'L	FINISH
TITLE DSTD-188 (8088 CPU)			
DWG NO. DY00492-I-A1-1	ISS 1	SH 1 OF 3	



SCALE	DATE	CHK	DATE
APP'S	APR 13, 1983	WAT/L	FINISH
TITLE	DSTD-188	(8088 CPU)	
DRG NO	DY00492-1-A3-1	105	1 30 30 3

MEMORY DECODE