

OPERATIONS MANUAL

DSTD SERIAL/PARALLEL
201 I/O
DY00438



dy-4 SYSTEMS INC.

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DSTD-201 SERIAL/PARALLEL I/O
OPERATIONS MANUAL

DY00438

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TABLE OF CONTENTS

SECTION NUMBER	PARAGRAPH NUMBER	TITLE	PAGE NUMBER
1.0		GENERAL INFORMATION	1 - 1
	1.1	Introduction Features	1 - 1
	1.2	DSTD Series General Description	1 - 1
	1.3	DSTD-201	1 - 1
	1.3.1	Serial Channels	1 - 1
	1.3.2	Parallel Channels	1 - 2
2.0		FUNCTIONAL HARDWARE DESCRIPTION	2 - 1
	2.1	Introduction	2 - 1
	2.2	Block Diagram Description	2 - 1
	2.2.1	STD BUS Interface	2 - 2
	2.2.2	Serial I/O Controller	2 - 2
	2.2.3	Baud Rate Generator	2 - 2
	2.2.4	Baud Rate Selection	2 - 2
	2.2.5	RS-232C Interface	2 - 2
	2.2.6	Current Loop	2 - 2
	2.2.7	Serial Port Configuration Jumper Block	2 - 3
	2.2.8	Parallel I/O Controller	2 - 3
	2.2.9	Driver/Receiver Circuitry	2 - 4
	2.2.10	I/O Bus Terminators	2 - 4
	2.3	Z80 Interrupts	2 - 4
	2.3.1	Interrupt Overview	2 - 4
	2.3.2	Priority Daisy Chain	2 - 4
3.0		USER SELECTABLE OPTIONS	3 - 1
	3.1	Introduction	3 - 1
	3.2	Port Address	3 - 1
	3.3	Baud Rate Selection	3 - 4
	3.4	Serial Port Configuration	3 - 6
	3.4.1	Asynchronous Operation	3 - 6
	3.4.1.1	RS-232C - DCE Configuration	3 - 6
	3.4.1.2	RS-232C - DTE Configuration	3 - 6
	3.4.1.3	Current Loop - DCE Source	3 - 7
	3.4.1.4	Current Loop - DCE Sink	3 - 7
	3.4.1.5	Current Loop - DTE Source	3 - 8
	3.4.1.6	Current Loop - DTE Sink	3 - 8

LIST OF TABLES

TABLE	3-1	JB2 Port Address Pin Assignment	3 - 2
TABLE	3-2	I/O Port Configuration	3 - 3
TABLE	3-3	Baud Rate Selection	3 - 4
TABLE	3-4	RS-232C DCE Jumper Configuration	3 - 5
TABLE	3-5	RS-232C DTE Jumper Configuration	3 - 6
TABLE	3-6	Current Loop - DCE Source	3 - 6
TABLE	3-7	Current Loop - DCE Sink	3 - 7
TABLE	3-8	Current Loop - DTE Source	3 - 7
TABLE	3-9	Current Loop - DTE Sink	3 - 8
TABLE	3-10	Synchronous Clock Strapping Options	3 - 9
TABLE	3-11	Parallel Port Strapping Options	3 - 11
TABLE	3-12	Serial Channel(s) J1 and J2 Pin Assignments	3 - 12
TABLE	3-13	Parallel Port J3 Pin Assignment	3 - 13

LIST OF FIGURES

FIGURE	1-1	DSTD-201 Module	1 - 3
FIGURE	2-1	DSTD-201 Block Diagram	2 - 6
FIGURE	2-2	Block Diagram of Parallel Port Interface	2 - 7
FIGURE	2-3	DSTD-201 Priority Interrupt Architecture	2 - 8
FIGURE	C - 1	Component Placement	C - 3

LIST OF APPENDICES

APPENDIX	A	Option Jumper Summary
APPENDIX	B	STD-Z80 BUS Pin Out
APPENDIX	C	Parts List
APPENDIX	D	Schematics

3.4.2	Synchronous Operation	3 - 9
3.4.3	Factory Configuration	3 - 10
3.5	Parallel Port Configuration Options	3 - 10
3.5.1	Port Options	3 - 10
3.5.2	Factory Configuration	3 - 10
3.6	I/O Connector Pin Assignments	3 - 11

4.0 **FUNCTIONAL SPECIFICATIONS** 4 - 1

4.1	Word Size	4 - 1
4.1.1	Cycle Time	4 - 1
4.1.2	I/O Port Addressing	4 - 1
4.1.3	I/O Capacity	4 - 1
4.1.3.1	Serial Communication Ports	4 - 1
4.1.3.2	Parallel Ports	4 - 1
4.1.4	Interrupts	4 - 2
4.2	Electrical Specifications	4 - 2
4.2.1	STDbus Interface	4 - 2
4.2.2	Parallel I/O Ports Interface	4 - 2
4.2.3	Serial Channel Interface	4 - 2
4.2.4	Operating Temperature	4 - 3
4.2.5	Power Supply Requirements	4 - 3
4.3	Mechanical Specifications	4 - 3
4.3.1	Card Dimensions	4 - 3
4.3.2	STDbus Edge Connector	4 - 3
4.3.2.1	Mating BUS Connector	4 - 3
4.3.3	Serial Channel Connectors	4 - 3
4.3.3.1	Serial Channel Mating Connectors	4 - 3
4.3.4	Parallel Port Connector	4 - 3
4.3.4.1	Parallel Port Mating Connector	4 - 4

5.0 **FACTORY NOTICES** 5 - 1

5.1	Factory Repair Service	5 - 1
5.2	Limited Warranty	5 - 1

NOTICE

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SECTION 1

1.0 GENERAL INFORMATION

1.1 Introduction

The DSTD-201 is a multifunctional serial and parallel interface module compatible with the STD BUS. The serial interface consists of two RS-232C (or 20mA current loop) channels with an independent jumper-selectable baud rate generator per channel. Each serial channel supports a wide range of protocol requirements including ASYNC, BISYNC, SDLC and HDLC. The serial I/O is designed around a Zilog/Mostek Z80-SIO controller chip.

The parallel input/output interface consists of 16 programmable I/O lines designed to provide a variety of methods for inputting and outputting data from the STD BUS. The parallel I/O interface is designed around the Zilog/Mostek Z80-PIO controller providing two independent 8 bit I/O ports with two handshake control lines per port. All I/O lines are buffered and has provisions for a variety of resistor termination options.

The daisy-chain priority interrupt logic provides for automatic interrupt vectoring for Z80 processors.

1.2 DSTD Series General Description

The DSTD series was designed to satisfy the need for low cost OEM microcomputer modules. The DSTD-Z80 Bus uses a motherboard interconnect system concept. The modules for the STD-Z80 are a compact 4.5 x 6.5 inches which provides for system partitioning by functioning by function, e.g., CPU, Memory, I/O, etc. This smaller module size makes system packaging easier while increasing MOS-LSI densities provide for increased functionality per module.

1.3 DSTD-201 Features

1.3.1 Serial Channels

- Two independent full duplex serial channels
- Configurable as either RS-232C or 20mA current loop
- Asynchronous data rates form 12.5 to 19.2K bits per second
- Configurable as either Data Terminal Equipment (DTE) or Data Communications Equipment (DCE)

- Current loop circuitry can act as either "sink" or "source"
- Current loop optically isolated
- Modem control
- Based on Z80-SIO (MK3884)
- Supports certain synchronous configurations

1.3.2 Parallel Channels

- Two independent 8 bit parallel ports with handshake
- Fully buffered
- Provision for termination networks
- Based on Z80 PIO (MK3881)



FIGURE 1-1 DSTD-201 MODULE

SECTION 2

2.0 FUNCTIONAL HARDWARE DESCRIPTION

2.1 Introduction

The DSTD-201 provides two independent serial channels and two fully buffered 8 bit parallel ports. The serial channels are based on the Z80-SIO (MK3884) LSI chip. The parallel ports are based on the Z80-PIO (MK3881) chip.

Each serial channel has a programmable baud rate generator. Both channels are capable of handling asynchronous, synchronous and synchronous bit orientated protocols such as BISYNC, SDLC, HDLC and others. The Z80-SIO will generate and check CRC codes. The data and control signals are fully buffered and may be configured to support RS-232C levels or 20mA current loop. Jumper blocks are provided to enable the channels to be wired as either Data Terminal Equipment (DTE) or Data Communications Equipment (DCE). When using the 20mA current loop option, the channel may be wired as either a loop source (active mode) or a sink (passive mode). Optical isolation is provided for both transmit and receive circuits.

The two parallel ports are based on the Z80-PIO chips. The TTL buffers are 74LS243 4 bit transceiver chips. The direction of these buffers is controlled by individual jumper straps such that when a PIO channel is operated in mode 3 (refer to Z80-PIO technical manual) 4 bits can be used as inputs and four bits as outputs. Channel A may also be configured in a bidirectional mode (PIO - mode 2). In this mode the BSTB control signal is used along with ASTB to control the buffers. Provision is made for terminating networks on both ports. In addition it is possible to install capacitors to ground on the ASTD and BSTD lines. This option is provided to allow for addition input signal smoothing in extremely noisy applications. The two signals come with factory installed resistor pull-ups.

The DSTD-201 supports all Z80 interrupt modes. Interrupt vectors are programmable at card initialization. The card has been designed to support daisy-chained interrupt priority. The four on-board data I/O channels may be masked under program control for selected interrupt processing.

A 4MHz version of DSTD-201 is also available.

2.2 Block Diagram Description

The block diagram of the DSTD-201, Figure 2-1, illustrates the flow of system address, data and control signals. The following paragraphs describe the function of each of the major blocks.

2.2.1 STD BUS Interface

The STD BUS Interface consists of an assortment of circuitry which gates various BUS control signals including interrupt requests, daisy-chained priority In/Out, 0 clock, system reset, M1, I/ORQ read and interrupt acknowledge between the BUS and the on-board peripheral chips. The STD BUS Interface also includes address buffers, bidirectional data BUS transceivers and I/O port address decoder with associated jumper block for I/O address programming by the user.

2.2.2 Serial I/O Controller

The SIO (Serial Input/Output) circuit is a programmable, dual-channel device which provides formatting of data for serial data communications. For further device description refer to Zilog/Mostek Z80-SIO chip data sheet.

2.2.3 Baud Rate Generator

The Baud Rate Generator is a dual channel device featuring individual programmable baud rates on a channel basis selected via a wire-wrapable jumper block.

2.2.4 Baud Rate Selection

The Baud Rate Selection jumper block allows the user to select via wire-wrap jumpers, any popular baud rate from 50 to 19.2K. For programming details refer to Table 3-3.

2.2.5 RS-232C Interface

EIA RS-232C driver/receivers on each of the two channels are provided for the following serial communication signals:

- Transmit Data
- Received Data
- Request to Send
- Clear to Send
- Data Set Ready
- Data Terminal Ready
- Transmit Clock
- Receive Clock

2.2.6 Current Loop

The 20mA Current Loop circuitry features several selectable options for that mode of communication. The receiver and transmitter input and output lines may be configured to function in either an active or passive mode. In the active mode the DSTD-

201 provides the 20mA current source while in the passive mode, the DSTD-201 requires that the loop current be provided by the peripheral. In both the active and passive modes, the receive and transmit circuits are optically isolated.

2.2.7 Serial Port Configuration Jumper Block

The Serial Port Configuration jumper block (one jumper block per channel) allows the user to select one of the several features which are available as options. The programming of the jumper block (via wire wrap) determines the following options:

- i) Selection of channel A/B as Data Terminal Equipment (DTE) or Data Communication Equipment (DCE).
- ii) RS-232C or 20mA current loop
- iii) Selection of either internal or external clock for synchronous operations and
- iv) Selection of either active or passive mode for 20mA current loop option

2.2.8 Parallel I/O Controller

The PIO (Parallel Input/Output) circuit is a programmable two-port device which provides a TTL compatible interface between peripheral devices and the system bus. Major features of the PIO include:

- Two independent 8 bit bi-directional ports with handshake and data transfer control
- Interrupt driven handshake for fast response
- *Any one of four distinct modes of operation may be selected for a port:*

- Byte output
 - Byte input
 - Byte bi-directional bus (Port A only)
 - Bit control mode

- Daisy-chained priority interrupt logic

For further device description refer to Zilog/Mostek Z80-PIO data sheet.

2.2.9 Driver/Receiver Circuitry

The Driver/Receiver Circuitry buffers the PIO from the user's external peripheral device while at the same time providing high drive capability to the user's interface. A block diagram of the generalized parallel port interface is illustrated in Figure 2-2. The driver/receivers may be selected to be either inverting or non-inverting types. The card as shipped from the factory contains inverting devices.

2.2.10 I/O BUS Terminators

Each parallel port has provisions for bus terminators in the form of either resistor pull-ups or impedance-matching networks. The user has the option of selecting either type and installing the respective dual-in-line resistor network in the 14 pin socket provided on the DSTD-201.

The ready handshake output line associated with each port is terminated with a factory-installed 47 ohm series resistor. This series resistor helps dampen reflections on this output line due to driving of long interface cables to the user's equipment.

Both handshake control lines (on each port) STB and RDY, are buffered via exclusive OR gates and have the additional option of allowing the user to independently control the polarity or sense of each handshake signal. This feature eases the interfacing between the DSTD-201 and the user's peripheral devices. A generalized schematic of the port interface is illustrated in Figure 2-2.

2.3 Z80 Interrupts

2.3.1 Interrupt Overview

Interrupt capability is provided to allow peripheral devices to suspend CPU operation in an orderly manner and force the Z80 processor to start executing a specific peripheral service routine. On completion of the service routine, the Z80 returns to the operation from which it was interrupted.

2.3.2 Priority Daisy-Chain

Both the SIO and PIO are Z80 peripheral devices and as such include daisy-chained priority logic which automatically provides the programmed interrupt vector (from the highest priority interrupting device) to the processor during an interrupt acknowledge. Look-ahead priority logic, Figure 2-3, have been designed to ensure that more than one peripheral card (from an interrupt speed standpoint) may be included in a larger interrupt priority loop. This is accomplished by providing both ends of the

board daisy-chain logic (PCI and PCO) at the edge card connector J4, so that the card priority within a several-card priority daisy-chained system may be implemented.

The "high" and "low" state of the PCI or PCO determines the card priority in the same fashion as for the individual peripheral chips.

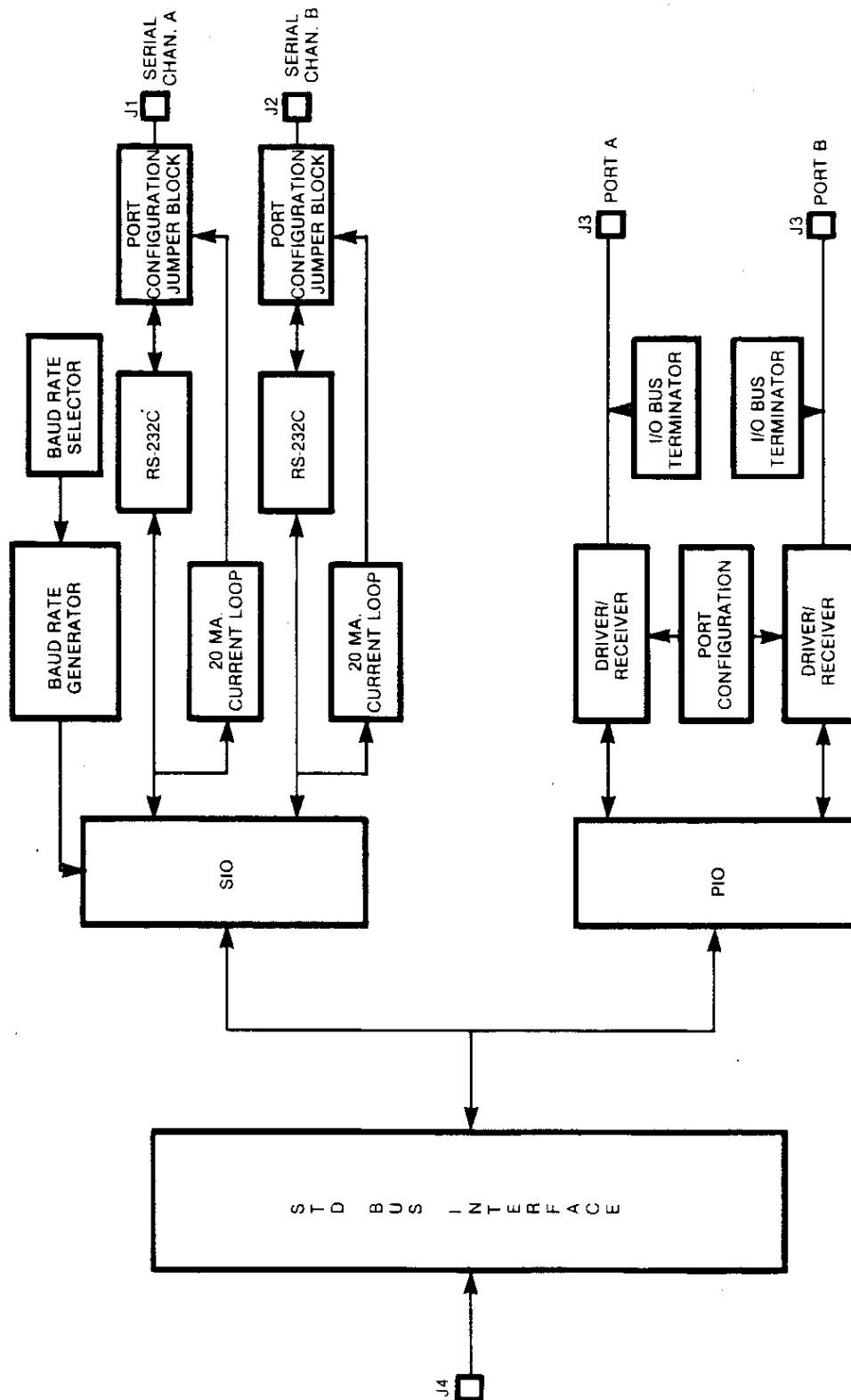


FIGURE 2-1 DSTD-201 BLOCK DIAGRAM

Ground ●
Optional *

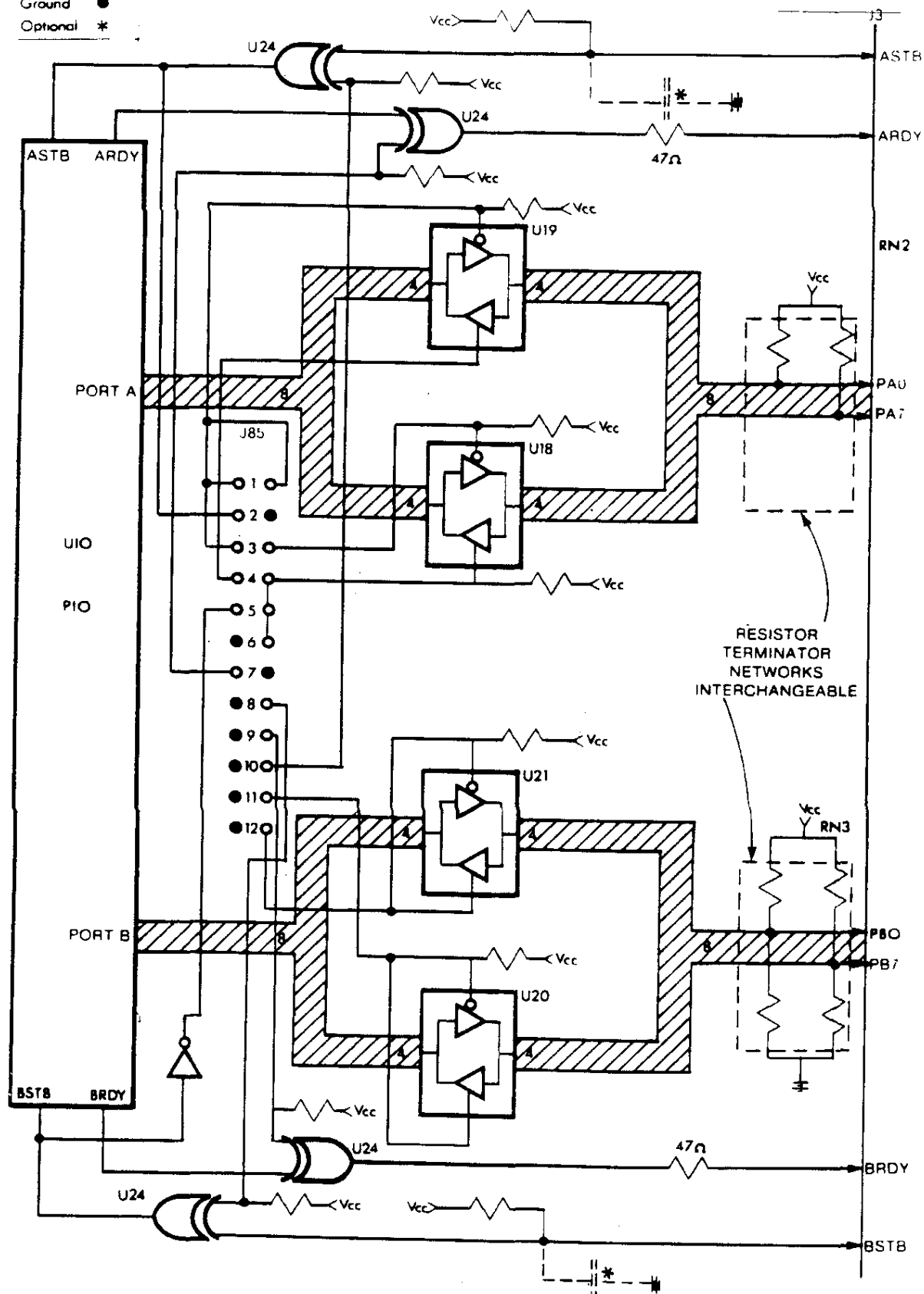


FIGURE 2-2 BLOCK DIAGRAM OF PARALLEL PORT INTERFACE

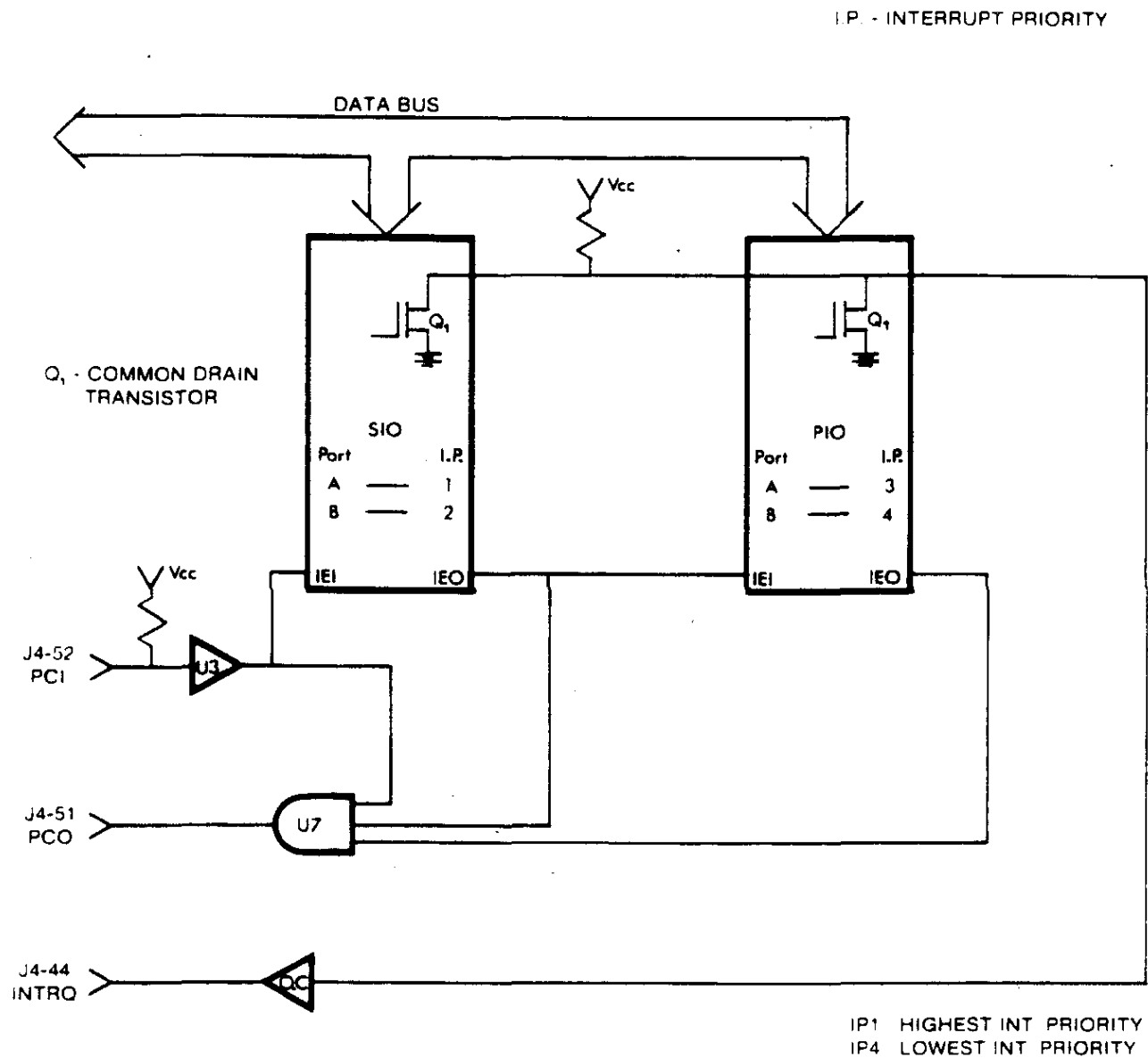


FIGURE 2-3 DSTD-201 PRIORITY INTERRUPT ARCHITECTURE

SECTION 3

3.0 USER SELECTABLE OPTIONS

3.1 Introduction

The DSTD-201 incorporates many strapable options to provide the user with a high degree of flexibility in system configuration. User jumper-programmable options include:

- i) I/O Port Address
- ii) Baud Rate Selection per serial channel
- iii) RS-232C or 20mA current loop
- iv) RS-232C DTE or DCE
- v) 20mA Current Loop active or passive
- vi) RS-232C Asynchronous and Synchronous
- vii) Parallel Ports Input or Output on a 4 bit basis
- viii) Inverting or Non-inverting polarity on parallel port handshake STD and RDY signals
- ix) Bi-directional parallel port option

The DSTD-201 also supports options which are device dependent and include the following:

- i) Inverting or Non-inverting parallel output data lines, selectable on a 4 bit nibble basis
- ii) Resistor terminator networks on parallel port data lines, either impedance matching networks or resistor pull-up networks
- iii) Resistor-capacitor filter network on both ASTB and BSTB handshake control signals

3.2 Port Address

The DSTD-201 occupies 8 contiguous I/O addresses. Its position in the I/O address space is determined by JB2 connections. Table 3-1 shows the jumper block pin numbers and the corresponding processor address bits used in the comparison. Installing a jumper implies a logic '0'. No jumper implies a logic '1'.

Example:

- 1) Base Address B8H requires jumpers between pins 2A and 2B
- 2) Base Address 50H requires jumpers between pins 1A & 1B, 3A & 3B and 5A & 5B

The board is shipped from the factory wired for address B8H corresponding to standard dy-4 software.

Table 3-2 illustrates the function of each of the 8 individual I/O Ports assigned to the DSTD-201.

TABLE 3-1

JB2 PORT ADDRESS PIN ASSIGNMENTS

PIN	ADDRESS BIT
1	A7
2	A6
3	A5
4	A4
5	A3

Logic '0' - Jumper Installed

Logic '11' - No Jumper

TABLE 3-2

I/O PORT CONFIGURATION

PORT ADDRESS								PORT FUNCTION
A7	A6	A5	A4	A3	A2	A1	A0	
x	x	x	x	x	o	o	o	PIO Port A - Data
x	x	x	x	x	o	o	1	Port A - Control
x	x	x	x	x	o	1	o	Port B - Data
x	x	x	x	x	o	1	1	Port B - Control
x	x	x	x	x	1	o	o	SIO Chan A - Data
x	x	x	x	x	1	o	1	Chan A - Control
x	x	x	x	x	1	1	o	Chan B - Data
x	x	x	x	x	1	1	1	Chan B - Control

3.3 Baud Rate Selection

Jumper Block JB1 is used to program the baud rates for the two serial channels. (JB1) consists of three rows of pins labeled A, B and C. All the 'A' row pins are connected to ground. All the 'C' row pins are pulled up to Vcc through a 1K ohm resistor. The programming inputs to the baud rate generators are connected to pins in row 'B'. Pins 2B, 4B, 6B and 8B are associated with channel A and pins 1B, 3B, 5B, 7B are associated with channel B. Each pin is either connected to the 'C' row for logic '1' or the 'A' row for a logic '0'. JB6 is provided to allow the user to use an external clock source. This feature is required for some synchronous modes. Table 3-3 shows the jumpers for programming the baud rates.

The board is shipped from the factory with both channels set for 9600 baud and with JB6-1 connected to JB6-2 and JB6-3 connected to JB6-4.

TABLE 3-3
BAUD RATE SELECTION

Baud Rate Generator Channel A/B				Synchronous X1	SIO - Programming Asynchronous		
7B/8B	5B/6B	3B/4B	1B/2B		X16	X32	X64
o	o	o	o	800	50	25	12.5
o	o	o	1	1,200	75	37.5	18.75
o	o	1	o	1,760	110	55	27.50
o	o	1	1	2,152	134.5	67.25	33.63
o	1	o	o	2,400	150	75	37.50
o	1	o	1	4,800	300	150	75
o	1	1	o	9,600	600	300	150
o	1	1	1	19,200	1,200	600	300
1	o	o	o	28,800	1,800	900	450
1	o	o	1	32,000	2,000	1,000	500
1	o	1	o	38,400	2,400	1,200	600
1	o	1	1	57,600	3,600	1,800	890
1	1	o	o	76,800	4,800	2,400	1,200
1	1	o	1	115,200	7,200	3,600	1,800
1	1	1	o	153,600	9,600	4,800	2,400
1	1	1	1	307,200	19,200	9,600	4,800

NOTE: If using current loop mode, baud rates above 1200 Baud are not recommended.

3.4 Serial Port Configurations

3.4.1 Asynchronous Operation

The following sections describe the six basic asynchronous configurations and the four synchronous configuration. Jumper blocks JB3 and JB4 determine the function of the signal pins for the serial I/O connectors J1 and J2.

3.4.1.1 RS-232C - DCE Configuration

Used when connecting a CRT or similar equipment. The signal names indicate control and data flow with respect to the CRT. Table 3-4 itemizes the jumper configurations for this mode of operation.

TABLE 3-4

RS-232C DCE JUMPER CONFIGURATION

<u>EIA</u> <u>Signal Name</u>	<u>Installed Jumpers</u> <u>JB3/JB4</u>	<u>J1/J2</u> <u>Pin Numbers</u>
RX	1A - 1B	5
TX	2A - 2B	3
CTS	3A - 3B	9
RTS	4A - 4B	7
DCD	5A - 5B	15
DTR	6A - 6B	14
DSR	-	11

3.4.1.2 RS-232C - DTE Configuration

Used when connecting to a modem or computer or similar equipment. The signal names indicate control and data flow with respect to the DSTD-201 and Table 3-5 itemizes the jumper configurations for this mode of operation.

TABLE 3-5
RS-232C DTE JUMPER CONFIGURATION

<u>EIA Signal Name</u>	<u>Installed Jumpers JB3/JB4</u>	<u>J1/J2 Pin Numbers</u>
RX	2A - 1B	5
TX	1A - 2B	3
CTS	4A - 3B	9
RTS	3A - 4B	7
DCD	6A - 5B	15
DTR	5A - 6B	14
DSR	-	11

3.4.1.3 Current Loop - DCE Source

Used when connecting to a TTY and when the DSTD-201 is "sourcing" the current. Table 3-6 itemizes the jumper configurations for this mode of operation.

TABLE 3-6
CURRENT LOOP - DCE SOURCE

<u>Loop Signal Name</u>	<u>Installed Jumpers JB3/JB4</u>	<u>J1/J2 Pin Number</u>
RX+	10A - 7B	17
RX-	9A - 8B	23
TX+	8A - 9B	25
TX-	7A - 10B	24

<u>JB3</u>	<u>JB4</u>
11A - 11B	12A - 12B
13A - 13B	14A - 14B
14A - 14B	15A - 15B
16A - 16B	17A - 17B
17A - 17B	11A - 11B

3.4.1.4 Current Loop DCE Sink

Used when connecting to a TTY and when the DSTD-201 is "sinking" current. Table 3-7 itemizes the jumper configuration for this mode operation.

TABLE 3-7
CURRENT LOOP - DCE SINK

Loop <u>Signal Name</u>	<u>Installed Jumpers</u>		<u>J1/J2 Pin Number</u>
	<u>JB3</u>	<u>JB4</u>	
RX+	9A - 7B	9A - 7B	17
RX-	10A - 8B	10A - 8B	23
TX+	8A - 9B	8A - 9B	25
TX-	7A - 10B	7A - 10B	24
	15A - 15B	16A - 16B	
	12A - 12B	13A - 13B	
	17A - 17B	11A - 11B	

3.4.1.5 Current Loop DTE Source

Used when connecting to a computer or modem and when the DSTD-201 is to "source" the current. Table 3-8 itemizes the jumper configurations for this mode of operation.

TABLE 3-8
CURRENT LOOP - DTE SOURCE

Loop <u>Signal Name</u>	<u>Installed Jumpers</u>		<u>J1/J2 Pin Number</u>
	<u>JB3</u>	<u>JB4</u>	
RX+	7A - 7B	7A - 7B	17
RX-	8A - 8B	8A - 8B	23
TX+	10A - 9B	9A - 9B	25
TX-	9A - 10B	10A - 10B	24
	11A - 11B	12A - 12B	
	13A - 13B	14A - 14B	
	14A - 14B	15A - 15B	
	16A - 16B	17A - 17B	
	17A - 17B	11A - 11B	

3.4.1.6 Current Loop - DTE Sink

Used when connecting to a computer or modem and when the DSTD-201 is "sinking" the current. Table 3-9 itemizes the jumper configuration for this mode of operation.

TABLE 3-9

CURRENT LOOP - DTE SINK

<u>Loop Signal Name</u>	<u>Installed Jumpers</u>		<u>J1/J2 Pin Number</u>
	<u>JB3</u>	<u>JB4</u>	
RX+	8A - 7B	8A - 7B	17
RX-	7A - 8B	7A - 8B	23
TX+	9A - 9B	9A - 9B	25
TX-	10A - 10B	10A - 10B	24
	12A - 12B	13A - 13B	
	17A - 17B	11A - 11B	
	15A - 15B	16A - 16B	

3.4.2 Synchronous Operation

The DSTD-201 can accommodate certain synchronous configurations. In synchronous systems the clock is transmitted along with the data. When using DSTD-201 card, both the transmit and receive clocks are provided by the DCE to the DTE.

Two uncommitted RS-232C drivers and two RS-232C receivers are available for the various synchronous configurations. These devices are accessed using jumper blocks JB7, JB8, JB9 and JB10. Connections are made by running wires from the jumper block associated with the edge connector to the RS-232C device and the RS-232C device to the baud rate generator and the SIO. Jumper block JB6 is used to access the baud rate generator and the SIO clock pins. The current loop signal pins may be used for the synchronous clock signals.

Table 3-10 shows the jumper connects for the synchronous configuration. The data and control lines are connected in the same manner as in asynchronous operation.

TABLE 3-10
SYNCHRONOUS CLOCK STRAPPING OPTIONS

Serial Channel	CONFIGURATION	
	DTE Option	DCE Option
CHANNEL A	JB6-2 to JB9-1 JB9-2 to JB3-7B	JB6-1 to JB6-2 JB1-9B to JB8-2 JB8-1 to JB3-7B
Channel B	JB6-4 to JB10-2 JB10-1 to JB4-7B	JB6-3 to JB6-4 JB1-9A to JB7-1 JB7-2 to JB4-7B

3.4.3 Factory Configuration

The board is shipped from the factory with channel A configured as a RS-232C DCE and channel B configured as a RS-232C.

3.5 Parallel Port Configuration Options

3.5.1 Ports Options

The DSTD-201 has 2 independent fully buffered 8 bit parallel ports. The ports are implemented using a Z80-PIO (MK3881) LSI chip and buffer/transceiver. Jumpers are provided to invert the sense of "strobe" and "data ready" signals. Provision has been made for terminating both 8 bit ports. A capacitor may be installed across each of the "strobe" lines. The ports may actually be configured on a nibble basis (4 bits). Jumpers allow bits 0 - 3 to setup in one direction and bits 4 - 7 in the other direction. Port A may also be set up in a bi-directional mode with the direction controlled by the "AST" signal.

Table 3-11 summarizes the strapping options for the two parallel ports.

3.5.2 Factory Configuration

The board is shipped from the factory with ports A and B unstrapped.

TABLE 3-11
PARALLEL PORT STRAPPING OPTIONS

Port	Data Bits	Function	Jumper Block JB5
Port A	Bits 0 - 3	Out	3B - 4B 1A - 2A
		In	3B - 4B
Port A	Bits 4 - 7	Out	3A - 4A 6A - 6B
		In	3A - 4A
	Bits 0 - 7	Bi-directional	1B - 2B 3A - 3B 4A - 4B 5A - 5B
	ARDY	True Inverted	7A - 7B N/C
	ASTB	True Inverted	10A - 10B N/C
Port B	Bits 0 - 3	Out	12A - 12B
		In	N/C
Port B	Bits 4 - 7	Out	11A - 11B N/C
		In	N/C
	BRDY	True Inverted	9A - 9B N/C
	BSTB	True	8A - 8B N/C

3.6 I/O Connector Pin Assignments

Tables 3-12 and 3-13 give the signal names and pin numbers for the serial and parallel channels. Serial Channel A is accessed through J1; Serial Channel B is accessed through J2 and both parallel ports are accessed through J3. For connector locations refer to Figure 1-1.

TABLE 3-12

SERIAL CHANNEL(S) J1 AND J2 PIN ASSIGNMENTS

<u>Pin Number</u>	<u>Description</u>	<u>Signal Name</u>
1	Protective Ground (AA)	GND
3	Transmitted Data (BA)	TX
5	Received Data (BB)	RX
7	Request to Send (CA)	RTS
9	Clear to Send (CB)	CTS
11	Data Set Ready (CC)	DSR
13	Signal Ground (AB)	SGND
14	Data Terminal Ready (CD)	DTR
15	Carrier Detect (CF)	CD
17,22	RX+ 20mA - loop	RX
18	Polarization Pin	
23	RX-, 20mA - loop	RX-
24	TX-, 20mA - loop	TX-
25	TX+, 20mA - loop	TX

* Note that the pin numbers have been chosen to allow the use of a ribbon cable to mate with a standard DB25 type connector.

TABLE 3-13
PARALLEL PORT J3 PIN ASSIGNMENT

<u>Pin Number</u>	<u>Description</u>	<u>Signal Name</u>
1	Port A Ready - Output	ARDY
2	Port A Strobe - Input	ASTB
3	Port A Data bit 7 - MSB	PA7
4	Port A Data bit 5	PA5
5	Port A Data bit 3	PA3
6	Port A Data bit 1	PA1
7	Port B Data bit 0 LSB	PB0
8	Port B Data bit 2	PB2
9	Port B Data bit 4	PB4
10	Port B Data bit 6	PB6
11	Port B Strobe - Input	BSTB
12	Port B Ready - Output	BRDY
13		--
14	Ground	GND
15	Ground	GND
16	Port A Data bit 6	PA6
17	Port A Data bit 4	PA4
18	Port A Data bit 2	PA2
19	Port A Data bit 0-LSB	PA0
20	Port B Data bit 1	PB1
21	Port B Data bit 3	PB3
22	Port B Data bit 5	PB5
23	Port B Data bit 7-MSB	PB7
24	Ground	GND
25	Ground	GND
26		--

SECTION 4

4.0 FUNCTIONAL SPECIFICATIONS

4.1 Word Size

Data 8 bits
I/O Addressing 8 bits

4.1.1 Cycle Time

	Min.	Max.
DSTD-201-2.5	250KHz	2.5MHz
DSTD-201-4.0	250KHz	4.0MHz

4.1.2 I/O Port Addressing

On-board user-programmable, refer to Table 3-1 and 3-2 for programming details.

4.1.3 I/O Capacity

The DSTD-201 supports two serial I/O channels and two 8 bit parallel I/O ports.

4.1.3.1 Serial Communication Ports

Each of the two identical full duplex serial ports may support either synchronous or asynchronous operation. The SIO contains special control registers and circuitry to permit implementation of asynchronous, SDLC, BiSync, MonoSync and HDLC formats.

Each serial channel has its own baud rate generator which may be user programmed for the desired baud rate. For programming details refer to Table 3-3.

4.1.3.2 Parallel Ports

Each of the two identical parallel ports may be jumper programmed in 4 bit nibbles as either In Only, Out Only or Bi-directional. The bi-directional option applies to port 1 only. Each 8 bit port (Port A and Port B) provides for automatic handshake.

4.1.4 Interrupts

The DSTD-201 supports vectored interrupt generation via both the SIO and PIO controller chips. Each device is interrupt vector programmable upon initialization. Also the DSTD-201 supports full daisy-chain interrupt priority. The parallel ports, using mode 3 (see PIO Data Sheet) may be configured to generate an interrupt if the I/O data pattern does not match a proprogrammed mask register within the PIO.

4.2 Electrical Specifications

4.2.1 STD BUS Interface

Bus Inputs : one 74LS load max

Bus Outputs: I_{OL} 24mA minimum @ V_{OL} 0.5 Volts
 I_{OH} 15mA minimum @ V_{OH} 2.4 Volts

4.2.2 Parallel I/O Ports Interface

Transceiver type 74LS243 Non Inverting

I_{OL} 24mA minimum @ V_{OL} 0.5 Volts
 I_{OH} 15mA minimum @ V_{OH} 2.4 Volts

Or Tranceiver type 74242 Inverting

I_{OL} 24mA minimum @ V_{OL} 0.5 Volts
 I_{OH} 155mA minimum @ V_{OH} 2.4 Volts

Resister Pull-up 1K ohm

Or Resistor Terminator 280/330 ohms

*These chips are supplied with the board as delivered from the factory. Alternate transceiver chips and resistor packs may be installed by the user as desired.

1K ohm pull-up resistors are provided on both STB handshake control lines and a series 47 ohm terminator is provided with each RDY output strobe line.

4.2.3 Serial Channel Interface

Each serial channel may be configured for either 20ma current loop or RS-232C operation. Refer to Section 3.4 for programming details.

4.2.4 Operating Temperature
0 degrees Celsius to 60 degrees Celsius.

4.2.5 Power Supply Requirements
5VDC \pm 5% @ 0.75 Amps Max.
12VDC \pm 5% @ 0.06 Amps Max.

4.3 Mechanical Specifications

4.3.1 Card Dimensions
4.5 inches (11.43cm) wide by 6.50 inches (16.52cm) long
0.48 inches (1.22cm) maximum height
0.062 inches (0.16cm) printed circuit board thickness

4.3.2 STD BUS Edge Connector
56 Pin dual readout; 0.125 inch centers

4.3.2.1 Mating BUS Connector
Viking 3VH28/1CE5 (PCB)
Viking 3VH28/1CND5 (Wire Wrap)
Viking 3VH28/1CN5 (Solder Lug)

4.3.3 Serial Channel Connectors
2-26 Pin Dual 0.100 inch grid flat cable type male connectors
(headers)

4.3.3.1 Serial Channel Mating Connectors
Ansley 609-2600M (flat cable) or equivalent

4.3.4 Parallel Port Connector
1-26 Pin Dual 0.100 inch grid flat cable type male connector
(header)

4.3.4.1 Parallel Port Mating Connector

Ansley 609-2600M (flat cable) or equivalent

Winchester PGB26A - housing)

For use with discrete wires

Winchester 100-700COS - contacts)

SECTION 5

5.0 FACTORY NOTICES

5.1 Factory Repair Service

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. **THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL.** Enclose a letter containing the following information with the returned circuit board:

Name, address and phone number of purchaser
Date and place of purchase
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

dy-4 SYSTEMS INC.,
888 Lady Ellen Place,
Ottawa, Ontario
K1Z 5M1, Canada

Securely package and mail the circuit board, prepaid and insured, to the same address.

5.2 Limited Warranty

Dy-4 warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

NOTICE

The antistatic bag is provided for shipment of the dy-4 PC boards to prevent damage to the components due to electrostatic discharge.

Failure to use this bag in shipment will VOID the warranty.

APPENDIX A
OPTION JUMPER SUMMARY

APPENDIX A OPTION JUMPER SUMMARY

A-1 Jumper Block Functional Assignment

JB1 - Baud Rate Selection
 JB2 - Module I/O Port Address Selection
 JB3 - Serial Channel A DCE/DTE Configuration Selection
 JB4 - Serial Channel B DCE/DTE Configuration Selection
 JB5 - Parallel Ports A and B Configuration Selection
 JB6 - Asynchronous/Synchronous Mode Selection
 JB7 to JB10 - Synchronous Configuration Selection

A-2 JB1 Baud Rate Selection

JB1				
	A	B	C	
1	0	0	0	- Bit 0 channel B
2	0	0	0	- Bit 0 channel A
3	0	0	0	- Bit 1 channel B
4	0	0	0	- Bit 1 channel A
5	0	0	0	- Bit 2 channel B
6	0	0	0	- Bit 2 channel A
7	0	0	0	- Bit 3 channel B
8	0	0	0	- Bit 3 channel A
9	0	0		- Baud Rate Generator Test Points

- 1) Baud rate generator pins connected to row B of JB1.
- 2) For a logic '1' connect pin on row C to respective pin on row B.
- 3) For a logic '0' connect pin on row A to respective pin on row B.

JB2 Module I/O Port Address Selection

JB2

	A	B
1	0	0
2	0	0
3	0	0
4	0	0
5	0	0
6		
7		
8		
9		

- Address Bit A7

- Address Bit A6

- Address Bit A5

- Address Bit A4

- Address Bit A3

- Refer to Schematic for Details

- 1) Address Decoder(A2) pins connected to Row B of JB2 pins 1 to 5.
- 2) Row A of JB2, pins 1 to 5 connected to ground.
- 3) For a logic '1' no jumper installed between A & B rows.
- 4) For a logic '0' install jumper between respective pin on A & B rows.

JB3 Serial Channel A DCE/DTE Configuration Selection

A-Side Definition	JB3		B-Side Definition
	A	B	
RS-232C, Chan. A Tx Data -	0 1 0		- Rx, Pin 5 of Connector J2
RS-232C, Chan. A Rx Data-	0 2 0		- Tx, Pin 3 of Connector J2
RS-232C, Chan. A RTS	0 3 0		- CTS, Pin 9 of Connector J2
RS-232C, Chan. A CTS	0 4 0		- RTS, Pin7 of Connector J2
RS-232C, Chan. A DTR	0 5 0		- DCD, Pin 15 of Connector J2
RS-232C, Chan. A DCD	0 6 0		- DTR, Pin 14 of Connector J2
	0 7 0		- R _x +, Pin 17 & 22 of Connector J2
	0 8 0		- R _x -, Pin 23 of Connector J2
	0 9 0		- Tx-, Pin 25 of Connector J2
	0 100		- Rx+, Pin 24 of Connector J2
	0 110		
Current Loop Configuration	0 120		
	0 130		
	0 140		--- Current Loop Configuration
	0 150		
	0 160		
	0 170		

- 1) For RS-232C DCE Configuration refer to Table 3-4.
- 2) For RS-232C DTE Configuration refer to Table 3-5.
- 3) For Current Loop DCE Source Configuration refer to Table 3-6.
- 4) For Current Loop DCE Sink Configuration refer to Table 3-7.

- 5) For Current Loop DTE Source Configuration refer to Table 3-8.
- 6) For Current Loop DTE Sink Configuration refer to Table 3-9.

A-5 JB4 Serial Channel B DCE/DTE Configuration Selection

- 1) Jumper Block JB4 layout same as for JB3, refer to paragraph A-4 for details.
- 2) DCE/DTE configuration for both RS-232C and Current Loop outlined in paragraph A-4 for Channel A also covers Channel B.

A-6 JB5 Parallel Ports A & B Configuration Selection

		JB5			
		B		A	
Port A ₀₋₃ Output Enable	-	0	1	0	- Port A ₀₋₃ Output Enable
ASTB	-	0	2	0	- Ground
Port A ₀₋₃ Output Enable	-	0	3	0	- Port A ₄₋₇ Output Enable
Port A ₀₋₃ Input Enable	-	0	4	0	- Port A ₄₋₇ Input Enable
BSTB	-	0	5	0	- Port A ₄₋₇ Input Enable
Ground	-	0	6	0	- Port A ₄₋₇ Input Enable
ARDY Polarity Control	-	0	7	0	- Ground
Ground	-	0	8	0	- BSTB Polarity Control
Ground	-	0	9	0	- BRDY Polarity Control
Ground	-	0	10	0	- ASTB Polarity Control
Ground	-	0	11	0	- Port B ₄₋₇ Input/Output Select
Ground	-	0	12	0	- Port B ₀₋₃ Input/Output Select

- 1) For Ports A and B Configuration refer to Table 3-11.

A-7

JB6 Asynchronous/Synchronous Mode Selection

JB6	

1	- Baud Rate Generator Clock Chan. B
2	- SIO Clock Input Chan. B
3	- Baud Rate Generator Clock Chan. A
4	- SIO Clock Input Chan. A

- 1) For Asynchronous Operation JB6-1 is connected to JB6-2 and JB6-3 is connected to JB6-4.
- 2) For Synchronous Operation these jumpers are removed.

A-8

JB7 to JB10 Synchronous Configuration Selection

- 1) Each of these jumper blocks have only two pins.
- 2) For Synchronous clock strapping refer to Table 3-10.

APPENDIX B
STD-Z80 BUS PIN OUT AND DESCRIPTION

APPENDIX B

STD-Z80 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	Ground - System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	Address Bus (Tri-state, output, active high).
15	A7	
16	A15	
17	A6	
18	A14	

STD-Z80 BUS PIN OUT

19	A5	A0-A15 make up a 16-bit address bus. The address bus provides the address for memory (up to 65k bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Memory Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Memory Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-State output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 Systems DSTD.

STD-Z80 BUS PIN OUT

36	/MEMEX	Memory expansion, not used on dy-4 Systems DSTD cards.
37	/REFRESH	/REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic zero and the upper 8 bits of the address bus contains the I register.
38	/DEBUG	/DEBUG (Input) used in conjunction with DDT-80 operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the /DEBUG line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
39	/M1	Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the opcode fetch cycle of an instruction. Note that during the execution of a 2-byte opcodes, /M1 will be generated as each opcode is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
40	STATUS 0	DMA priority chain input.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

- | | | |
|----|---------|---|
| 42 | /BUSRQ | <p>Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.</p> |
| 43 | /INTAK | <p>Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.</p> |
| 44 | /INTRQ | <p>Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.</p> |
| 45 | /WAITRQ | <p>WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.</p> |

46	/NMIRQ	Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will over-ride a /NMIRQ.
47	/SYSRESET	System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H and set Interrupt Mode 0.
48	/PBRESET	Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset.
49	/CLOCK	Processor Clock (Output, active low). Single phase system clock.
50	CNTRL	Auxiliary Timing
51	PCO	Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

STD-Z80 BUS PIN OUT

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.

APPENDIX C
PARTS LIST

PARTS LIST

QTY	DESIGNATOR	MICRO CIRCUIT	PART NO.	DESCRIPTION
1	U5		74LS00	QUAD 22 I/P NAND
1	U15		7406 (7416)	HEX INVERTER
1	U7		74LS11	TRIPLE 3 I/P AND
1	U6		74LS27	TRIPLE 3 I/P OR
2	U8,24		74LS86	2 I/P XOR
4	U18,21		74LS243	QUAD TRANSCEIVER
1	U3		74LS244	OCTAL BUFFER
1	U1		74LS645	OCTAL TRANSCEIVER
1	U2		74LS682	OCTAL COMPARATOR
2	U12,16		75188	RS232C RECEIVER
2	U11,17		75189	RS232C DRIVER
1	U4		K11351	BAUD RATE GEN
1	U9		MK3884N[-4]	SIO
1	U10		MK3881N[-4]	PIO
4	U13,14,22,23		4N36	OPTO ISOLATOR

RESISTOR

8	R3,4,6,14,25,R1,R2,R16		1K	1/4w	5%
2	R21,24		47ohm	1/4w	5%
*1	R5		680ohm	1/4w	5%
10	R8-12,17,20,22		470ohm	1/4w	5%
4	R26-29		100K	1/4w	5%
2	R13,23		150ohm	1/4w	5%
2	R7,15		3K	1/4w	5%
1	RN1	109-1826	1K	SIP	
2	*RN2,RN3	*1424-1839 (1413-472G)	Terminating Dip		

CAPACITORS

1	C1	TAG10M25	10 uf
2	C4,5	TAG4R7M25	4.7 uf
15	C2,3,6-15	8121-N071- 651-104M	0.1 uf
*8	C20,24-30	CK05BX331K	

TRANSISTOR

4	Q1-4	2N3904	NON Transistor
---	------	--------	----------------

DIODE

4	D1-4	1N4148	Signal Diode
2	D5,6	1N4001	Rectifier Diode

QTY	DESIGNATOR	MICRO CIRCUIT	PART NO.	DESCRIPTION
CONNECTOR				
2	J2,3		87476-3	Connector
1	J1		CHD6926W1R	Connector
2	JB3,4		CHD6934W1S	Header
2	JB1,2		CHD6920W1S	Header
2	JB16,7,8,9,10		CHS6910W1S	Header
1	JB5		CHD6926W1S	Header

SOCKETS				
2	U9,U11		640379-1	40 Pin
10	U18,U19,U20,U21		640358-1	16 Pin
	RN2,RN3,U11,U12			
	U16,U17			

* User Optional

APPENDIX D
SCHEMATIC

UNUSED GATES

PARTS LISTS			
DESIGNATION	QTY	TYPE	DESCRIPTION
Q1 - 4	4	TRANSISTOR 2N3904	
		CAPACITOR	
C1	1	TANT.	10 μ F
C4, 5	2	"	4.7 μ F
C6, 13, 19, 21	4	CERAMIC	0.1 μ F
C2, 3, 6-13, 16-18, C20, 29 C23-30	15 6	CERAMIC	0.01 μ F
		CONNECTOR	
J2, 3	2	RH 62 26D 2R	
J1	1	MS-1002	
D1-4	4	DIODE 1N4148	
DB1-10	10	HEADER SAE 6600	
		RESISTOR	
R3, 4, 6, 14, 25	5		1K 1/4W 52
R21, 24	2		47 Ω
R5	1		680 Ω
RB-12, 17-20, 22	10		470 Ω
R26-29	4		100K
R13, 23	2		150 Ω
R7, 15	2		3K
RN1	1	SIP	47K
RN2, RN3	2	DIP	
U5	1	74LS00	QUAD 2 I/P NAND
U15	1	7406	HEX INVERTER
U7	1	74LS11	TRIPLE 3 I/P AN
U6	1	74LS27	TRIPLE 3 I/P OR
U8, 24	2	74LS86	2 I/P XOR
U18-21	4	74LS243	QUAD TRANSCEIVER
U3	1	74LS244	OCTAL BUFFER
U1	1	74LS645	OCTAL TRANSCEIVER
U2	1	74LS682	OCTAL COMPARATOR
U12, 16	2	75188	RS232C RECEIVER
U11, 17	2	75189	RS232C DRIVER
U4	1	K1135A	BAUD RATE GEN
U9	1	MK3884N	510
U10	1	MK3881N	P10
U13, 14, 22, 23	4	4N36	OPTOISOLATOR
	1	PCB	

1, 2 \square +5

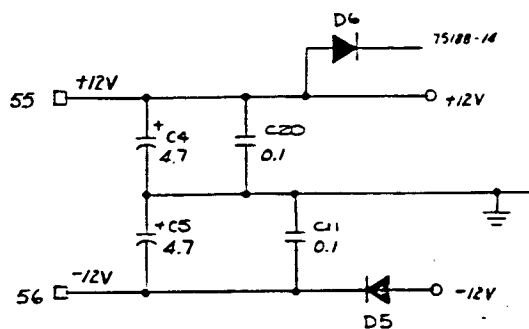
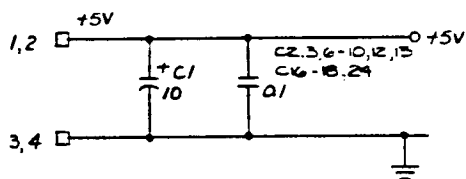
3, 4 \square

55 \square +11

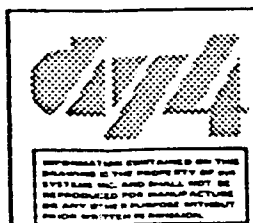
56 \square -12

ATES

TYPE	-12V	+12V	+5V	GND
74LS00			14	7
7406			14	7
74LS11			14	7
74LS27			14	7
74LS86			14	7
74LS245			14	7
74LS244			20	10
74LS645			20	10
74LS682			20	10
75188	1			7
75189			14	7
4135A		9	2	11
MK3884N			9	31
MK3881N			26	11

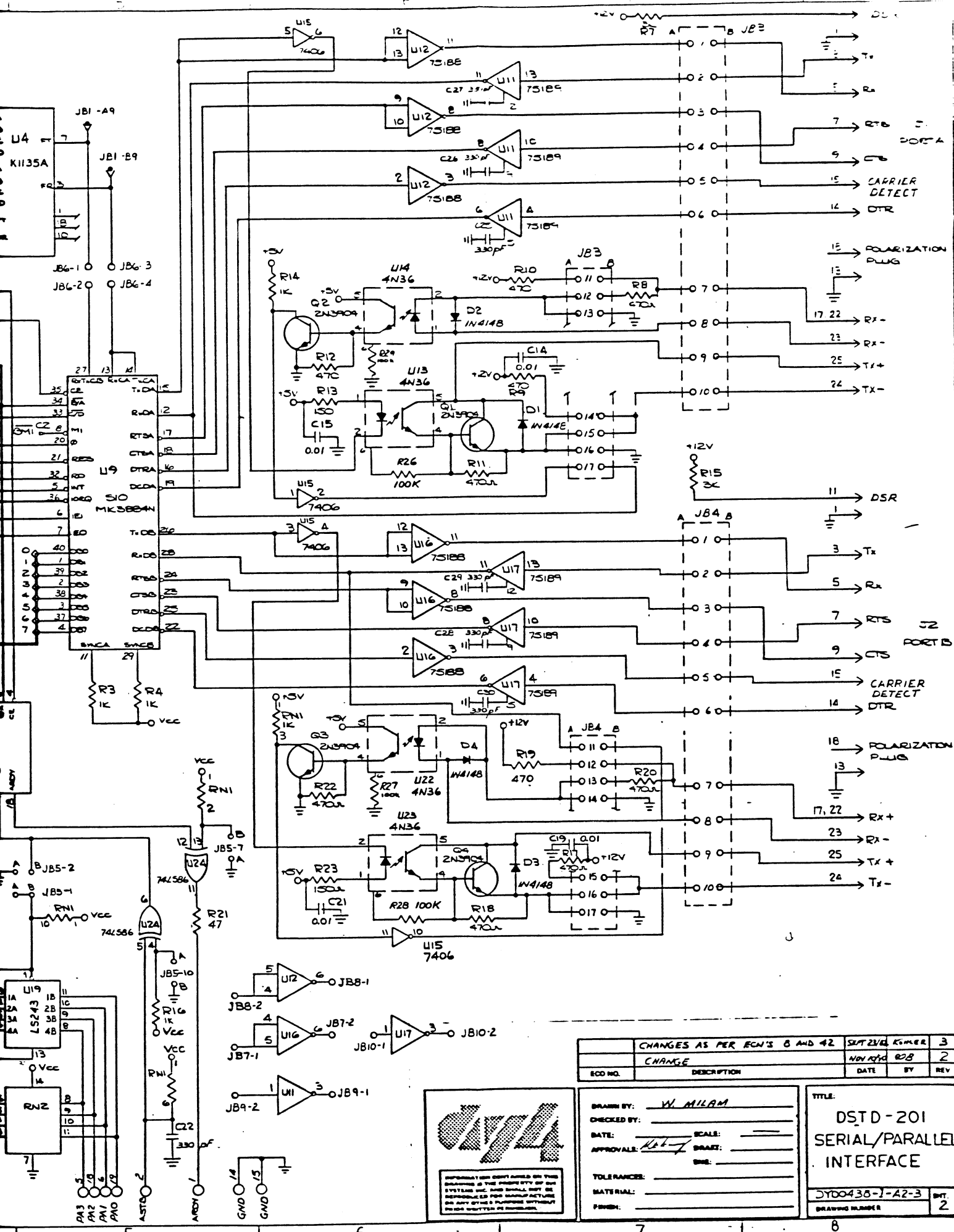


	CHANGES AS PER ECN'S 8 AND 42	23 SEP 82	EWLER
	Production Update	11 NOV 80	SE
ECO NO.	DESCRIPTION	DATE	BY



DRAWN BY: _____
 CHECKED BY: B. Scott
 DATE: 11 Nov 80 SCALE: _____
 APPROVALS: _____ DRAFT: _____
 ENG: _____
 TOLERANCES: _____
 MATERIAL: _____
 FINISH: _____

TITLE:
 DSTD-201
 SERIAL/PARALLEL
 INTERFACE
 DTD0438-1-A1-3
 DRAWING NUMBER



CHANGES AS PER ECN'S 8 AND 42		SEP 21/88	KEMER	3
CHANGE		NOV 19/88	028	2
ECO NO.	DESCRIPTION	DATE	BY	REV

DRAWN BY: W. MILAM
 CHECKED BY: _____
 DATE: _____ SCALE: _____
 APPROVAL: [Signature] DRAFT: _____
 TOLERANCES: _____
 MATERIAL: _____
 FINISH: _____

TITLE:
**DS1D-201
 SERIAL/PARALLEL
 INTERFACE**
 000430-1-A2-3
 DRAWING NUMBER
 2