

DSTD-202

QUAD SERIAL COMMUNICATIONS MODULE OPERATIONS MANUAL

COVERING PARTS NUMBER

PD 920200

PD 920201

DY00446-H-A1-1

NOTICE

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TABLE OF CONTENTS

SECTION	PARAGRAPH	DESCRIPTION	PAGE
1.0		GENERAL INFORMATION	1 - 1
	1.1	Introduction	1 - 1
	1.2	DSTD Series General Description	1 - 1
	1.3	DSTD-202 Features	1 - 1
2.0		FUNCTIONAL HARDWARE DESCRIPTION	2 - 1
	2.1	Introduction	2 - 1
	2.2	Block Diagram Description	2 - 1
	2.2.1	STD BUS Interface	2 - 1
	2.2.2	Serial Channel Controller	2 - 3
	2.2.3	Base Baud Rate Generator Clock	2 - 3
	2.2.4	Programmable Dividers	2 - 3
	2.2.5	Clock Configuration Blocks	2 - 3
	2.2.6	RS-232C Buffers	2 - 3
	2.2.7	DTE/DCE Configuration Blocks	2 - 4
	2.2.8	Status Input Register	2 - 4
3.0		USER SELECTABLE OPTIONS	3 - 1
	3.1	Introduction	3 - 1
	3.2	Address Selection	3 - 1
	3.2.1	Serial I/O Address	3 - 1
	3.2.2	Status Register Address	3 - 1
	3.3	Base Baud Rate Clock	3 - 2
	3.4	I/O Port Assignment	3 - 3
	3.5	Counter/Timer Interrupt Vectors	3 - 3
4.0		SPECIFICATIONS	4 - 1
	4.1	Functional Specifications	4 - 1
	4.1.1	Word Size	4 - 1
	4.1.2	Cycle Time	4 - 1
	4.1.3	I/O Addressing	4 - 1
	4.1.4	Serial Communication Ports	4 - 1
	4.1.5	Counter/Timer Channels	4 - 1
	4.1.6	Input Status Registers	4 - 1
	4.1.7	Interrupts	4 - 1
	4.1.7.1	System Interrupt Units	4 - 2
	4.2	Electrical Specifications	4 - 2
	4.2.1	STD Bus Interface	4 - 2
	4.2.2	Power Supply Requirements	4 - 2
	4.3	Operating Temperature	4 - 2
	4.4	Mechanical Specifications	4 - 2
	4.4.1	Card Dimensions	4 - 2
	4.4.2	STD BUS Edge Connector	4 - 2
	4.4.2.1	Mating Bus Connectors	4 - 2
	4.4.3	Serial Channel Connectors	4 - 3

5.0	FACTORY NOTICES	5 - 1
5.1	Factory Repair Service	5 - 1
5.2	Limited Warranty	5 - 1

LIST OF APPENDICES

Appendix	Description	Page
A	Option Jumper Summary	A - 1
B	STD-Z80 Bus Signals	B - 1
C	DSTD-202 Parts List	C - 1
D	Schematic	D - 1
E	Factory Preset Jumpers	E - 1
F	User Jumper Worksheets	F - 1

LIST OF TABLES

Table	Description	Page
3 - 1	Configuration of Baud Rate Generator (s)	3 - 3
3 - 2	DSTD-202 On-Board I/O Port Assignment	3 - 4
3 - 3	DSTD-202 Counter/Timer Interrupt Vectors	3 - 4

LIST OF FIGURES

Figure	Description	Page
1 - 1	DSTD-202 Quad Serial Communications Module	1 - 2
2 - 1	DSTD-202 Block Diagram	2 - 2
C - 1	DSTD-202 Silk Screen	C - 2

SECTION 1

1.0 GENERAL INFORMATION

1.1 Introduction

The dy-4 SYSTEMS DSTD-202 is a 4 channel RS-232C communications module. It is based on the Z80-SIO DART which provides full asynchronous capabilities. The module has software programmable baud rate generators on a channel basis, four auxiliary counter/timer channels and an 8 bit switch input to allow the user to input configuration information.

The daisy chain priority interrupt logic provides for automatic interrupt vectoring for Z80 processors.

1.2 DSTD Series General Description

The DSTD series was designed to satisfy the need for low cost OEM microcomputer modules. The DSTD-Z80 BUS uses a motherboard interconnect system concept. The modules for the STD-Z80 BUS are a compact 4.5 x 6.5 inches which provides for system partitioning by function, e.g. CPU, Memory, I/O, etc. This smaller module size makes system packaging easier while increasing MOS-LSI densities provide high functionality per module.

1.3 DSTD-202 Features

- * Four independent full duplex serial channels
- * Asynchronous operation
- * Operates as DTE or DCE
- * Independent software programmable Baud-rate clocks
- * Receiver data registers quadruply-buffered
- * Transmitter data registers double-buffered
- * Selectable I/O address
- * 4MHz option
- * Modem control on each channel
- * Four independent (12 Pin) channel connectors
- * Four auxiliary programmable counter/timer channels
- * 8-bit status input register (User jumperable)

SECTION 2

2.0 FUNCTIONAL HARDWARE DESCRIPTION

2.1 Introduction

The DSTD-202 utilizes four Z80 microprocessor peripheral chips. Two Z80-SIO DART chips control the serial channels and two Z80-CTC (3881) chips allow software programmability of the baud rates. The baud rate clock is generated from a crystal controlled oscillator and down counter. Option straps on the down counter allow further flexibility in selecting the baud rates.

Each serial channel has a set of option blocks to allow it to be configured for almost any application. The first jumper block allows the channel to be programmed as Data Terminal Equipment (DTE) or Data Communications Equipment (DCE). Two other option blocks control the source and direction of the transmit and receive clocks on a per channel basis.

The board has an eight bit status register which can be read by the system microprocessor. This register may be used to convey configuration information to the system software. Programming of the register is via wirewrap jumpers.

2.2 Block Diagram Description

Figure 2-1 is a block diagram illustrating the major logical blocks of the DSTD-202 module. The following paragraphs describe the function of each of the blocks.

2.2.1 STD BUS Interface

The STD BUS interface buffers the data bus, low order address bus and the control lines. It contains the I/O decode logic to select the serial channels, baud rate generators and the status register. The serial channels occupy sixteen contiguous I/O address.ports. The switch register is one I/O port and may be positioned independently of the serial channels.

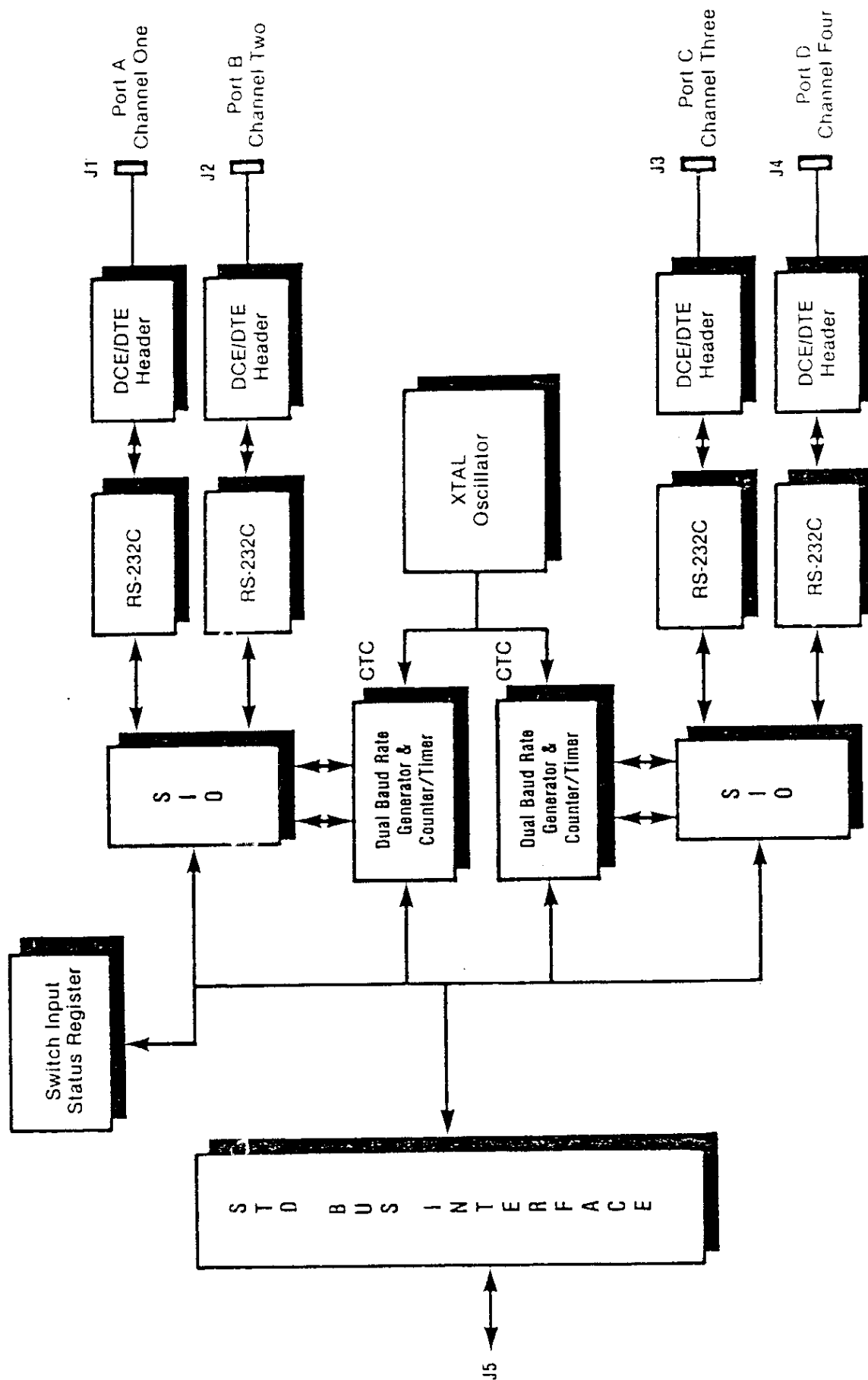


Figure 2-1 DSTD-202 Block Diagram

2.2.2 Serial Channel Controller

The serial channel controllers are implemented using two Mostek/Zilog Serial Input/Output LSI chips. This chip handles the serial to parallel and parallel to serial conversions and the data synchronizing. It provides an interface between the communication control lines and the processor bus.

2.2.3 Base Baud Rate Generator Clock

The baud rate generator clock is a crystal based oscillator. It can be strapped to provide two different base clocks. In the standard board these clocks are 1.2288 MHz and 0.6144 MHz. The base clock provides the input to the four software programmable baud rate generators. The board as shipped from the factory is strapped for a base clock of 1.2288 MHz which provides for asynchronous data rates from 37.5 baud to 76.8k baud.

2.2.4 Programmable Dividers

The programmable dividers are implemented using two Mostek/Zilog counter/timers LSI chips. Each chip provides 4 channels. Two timing channels are assigned to each communications channel. The first timing channel is used as a programmable divider and provides the transmit and receiver clocks. The second timing channel may be used by the system software to provide system timing for its associated communications channel. The base clock for this timing channel is 76.8KHz thus allowing for the generation of time intervals of approximately every 5 ms.

2.2.5 Clock Configuration Blocks

The clock configuration jumper blocks are used to set up the source of the transmit and receive clocks for each serial channel. For asynchronous mode the transmit and receive clock are typically derived from the on-board programmable dividers.

2.2.6 RS-232C Buffers

These buffers provide the level shifting between the on-board TTL logic and external RS-232C equipment. Provision is made for a certain amount of signal shaping (conditioning) on the receiver buffers. The transmit buffers provide short circuit current limiting of 8 milliamps.

2.2.7 DTE/DCE Configuration Blocks

The DTE/DCE jumpers allow each channel to be quickly and easily configured as either "data communications equipment" or "data terminal equipment". The blocks allow the use of a common or standard cable for both configurations. Each channel has a separate block for the control and data lines.

2.2.8 Status Input Register

The status input register consists of an 8 bit tri-state buffer and a jumper block. The jumper block allows the user to program each of the bits to a logic '0' or logic '1'. This eight bit byte is placed on the data bus when the status register is accessed.

SECTION 3

3.0 USER SELECTABLE OPTIONS

3.1 Introduction

The following sections discuss the user selection or user programmable options. This manual concentrates on the "hardware selectable options" with only a brief discussion of the system or software options. The user is referred to the operation manuals for the serial controller chips and the counter timer chips published by the chip manufacturers (Zilog, Mostek). In addition the user is referred to the EIA RS-232C Standards for asynchronous communication equipment.

3.2 Address Selection

The board is accessed using programmed I/O instructions. The Rboard occupies seventeen I/O address ports. Sixteen contiguous ports are used for the serial channels; four for each channel. The seventeenth I/O port is the switch register and is positioned independently of the serial channel ports.

3.2.1 Serial I/O Address

The sixteen serial I/O ports are positioned using jumper block JB19. The jumper blocks consist of 3 rows of four pins. These pins are used to program the 'A' side of a four bit comparator. The 'B' side of the comparator is connected to the address bus bits A4 to A7. Programming the comparator involves connecting the inputs to a logic '1' or a logic '0'. Row B of JB19 is the input to the comparator. Row A is a logic '1' and row C is a logic '0'. Each pin on row B must be connected to either row A or row C.

PINS	PROCESSOR ADDRESS BITS
1A, B, C	A4
2A, B, C	A5
3A, B, C	A6
4A, B, C	A7

3.2.2 Status Register Address

The status register address is set using jumper block JB17. This jumper block consists of two 8 pin rows. The pins in Row A are connected to ground (logic '0'). The pins in row B are connected to the inputs of an eight bit comparator. Installing a jumper programs the corresponding comparator input to a logic '0'

leaving the jumper cut programs the corresponding comparator input to a logic '1'. The address jumpers are defined as follows.

PINS	PROCESSOR ADDRESS BITS
1A - B	A7
2A - B	A6
3A - B	A5
4A - B	A4
5A - B	A3
6A - B	A2
7A - B	A1
8A - B	A0

3.3 Base Baud Rate Clock

The base baud rate clock is generated from a crystal controlled oscillator and a divider. Selecting a base clock involves choosing the appropriate tapping on the divider chain. Changing the base clock changes the range of baud rates available under software control. There are two ranges.

J15 Jumper	Base Frequency	Asynchronous Range (x16)
1A - 1B	(Factory use only)	
2A - 2B	1.2288 MHz	75 to 76.8k baud
3A - 3B	0.6144 MHz	37.5 to 38.4k baud

The card is shipped from the factory with the base clock set at 1.2288 MHz. Only one jumper in JB15 should be installed.

The base clock is further divided down by a programmable divider implemented using a channel in a Z80 Counter/Timer Circuit. The divider can be set to divide by 1 to 256. The output of the programmable divider can then be connected to the SIO chip. In asynchronous modes this signal can be further divided internally by 64, 32 or 16.

Table 3-1 shows the common baud rates and their corresponding divider ratios for base clock of 1.2288MHz. The table also shows the percentage deviation from nominal values.

The SIO has internal counter chains which can be set for x16, x32, or x64 in asynchronous modes.

Table 3-1 shows the asynchronous baud rates using the SIO's internal x16 divider. Using the x32 divider halves the baud rates (ie 150 to 38,400 baud). Using the "x64" divider halves the baud rates again. (ie. 75 to 19,200 baud).

TABLE 3 - 1
CONFIGURATION OF BAUD RATE GENERATOR(S)

Divider	Frequency	Asynchronous x16	% Deviation
1	1,228,800	76,800	
2	614,400	38,400	
4	307,200	19,200	
8	153,600	9,600	
16	76,800	4,800	
21	58,500	3,600	+1.6
32	38,400	2,400	
38	323,400	2,000	+1.0
43	385,800	1,800	-0.7
64	19,200	1,200	
128	9,600	600	
175	7,020	440	-0.2
256	4,800	300	

3.4 I/O Port Assignment

The sixteen ports related to the four serial channels are positioned as per paragraph 3.2.1. The functional assignment of each port is illustrated in Table 3-2. The base address shown in the Table assumes that the 4 bits of JB19 are programmed for a 'B' hexadecimal. These 4 bits may be programmed to any hexadecimal number.

3.5 Counter/Timer Interrupt Vectors

There are two CTC's used on the DSTD-202. Their interrupt vectors are assigned independently (just as the interrupt vectors of the SIO's are assigned independently). The second and fourth channels of both CTC's are designated as "auxiliary timers". Note that setting up the interrupt vectors can only be done using channel "0" of the CTC's. For CTC programming details refer to either Zilog or Mostek data sheet for the CTC.

TABLE 3-2

DSTD-202 ON-BOARD I/O PORT ASSIGNMENT

Port Number	Port Address	Function	Connector
A	B0	Data	J1
	B1	Control	
	B2	Baud Rate	
	B3	Aux Timing	
B	B4	Data	J2
	B5	Control	
	B6	Baud Rate	
	B7	Aux Timing	
C	B8	Data	J3
	B9	Control	
	BA	Baud Rate	
	BB	Aux Timing	
D	BC	Data	
	BD	Control	
	BE	Baud Rate	
	BF	Aux Timing	

TABLE 3-3

DSTD-202 COUNTER/TIMER INTERRUPT VECTORS

CTC 1	Channel 1	Port A Baud	XXXXX000
	2	Port A Aux	010
	3	Port B Baud	100
	4	Port B Aux	110
CTC 2	Channel 1	Port C Baud	YYYYY000
	2	Port C Aux	010
	3	Port D Baud	100
	4	Port D Aux	110

SECTION 4

4.0 SPECIFICATIONS

4.1 Functional Specifications

4.1.1 Word Size

Data	8 bits
I/O Addressing	8 bits

4.1.2 Cycle Time

	MIN.	MAX.
DSTD-202-2.5	250 KHz	2.5 MHz
DSTD-202-4.0	250 KHz	4.0 MHz

4.1.3 I/O Addressing

On-board user-programmable, refer to paragraph 3.2.1 for programming details.

4.1.4 Serial Communication Ports

Each serial channel has its own baud rage generator which may be user programmed for the desired baud rate via software. For programming details refer to paragraph 3.3.

4.1.5 Counter/Timer Channels

The DSTD-202 has four counter/timer channels which may be programmed via software. Refer to paragraph 2.2.4 for programming details.

4.1.6 Input Status Registers

The board contains an 8 bit input status register which may be programmed by the user for system application use.

4.1.7 Interrupts

The DSTD-202 supports vectored interrupt generation via both the SIO and CTC controller chips. Each device is interrupt vector programmable upon initialization. Also, the DSTD-202 supports full daisy chain interrupt priority.

4.1.7.1 System Interrupt Units

SIU - 4

4.2 Electrical Specifications

4.2.1 STD Bus Interface

Bus Inputs One 74LS Load max.

Bus Outputs I_{OL} - 24 mA min. @ $V_{OL} = 0.5VDC$ I_{OH} - -15 mA min. @ $V_{OH} = 2.4VDC$

4.2.2 Power Supply Requirements

+5VDC $\pm 5\%$ @ 1.1 Amps Max-12VDC $\pm 5\%$ @ 0.20 Amps Max-12VDC $\pm 5\%$ @ 0.20 Amps Max

4.3 Operating Temperature

0 degrees to 60 degrees Celsius

4.4 Mechanical Specifications

4.4.1 Card Dimensions

4.5 Inches (11.43 cm.) wide by 6.50 Inches (16.51 cm.) long

0.48 Inches (1.22 cm.) maximum height

0.062 Inches (0.16 cm.) printed circuit board thickness

4.4.2 STD BUS EDGE Connector

56 Pin dual readout; 0.125 inch centers

4.4.2.1 Mating Bus Connector

VIKING 3VH28/1CE5 (PCB)

VIKING 3VH28/1CND5 (Wirewrap)

VIKING 3VH28/1CN5 (Solder Lug)

4.4.3

Serial Channel Connectors

4 - 12 Pin Dual 0.100 inch grid

Mating Connector AMP 87631-8 or equivalent

SECTION 5

5.0 FACTORY NOTICES

5.1 Factory Repair Service

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. **THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL.** Enclose a letter containing the following information with the returned circuit board:

Name, address and phone number of purchaser
Date and place of purchase
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

dy-4 SYSTEMS INC.,
888 Lady Ellen Place,
Ottawa, Ontario
K1Z 5M1, Canada

Securely package and mail the circuit board, prepaid and insured, to the same address.

5.2 Limited Warranty

Dy-4 warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

NOTICE

The antistatic bag is provided for shipment of the dy-4 PC boards to prevent damage to the components due to electrostatic discharge.

Failure to use this bag in shipment will **VOID** the warranty.

APPENDIX A
OPTION JUMPER SUMMARY

APPENDIX A

A - 1 The following is a summary of the DSTD-202 option jumper blocks:

JB 1	Channel 1 DTE/DCE configuration block
JB 2	Channel 2 DTE/DCE configuration block
JB 3	Channel 3 DTE/DCE configuration block
JB 4	Channel 4 DTE/DCE configuration block
JB 5	Channel 1 Clock configuration block TTL side
JB 6	Channel 1 Clock configuration block RS-232C side
JB 7	Channel 2 Clock configuration block TTL side
JB 8	Channel 2 Clock configuration block RS-232C side
JB 9	Channel 3 Clock configuration block TTL side
JB 10	Channel 3 Clock configuration block RS-232C side
JB 11	Channel 4 Clock configuration block TTL side
JB 12	Channel 4 Clock configuration block RS-232C side
JN 13	Factory set options
JB 14	Factory set options
JB 15	Base baud rate Clock option block
JB 16	Switch register
JB 17	Switch register I/O address programming block
JB 18	BUSAK chain
JB 19	Serial Channel I/O address programming block

A - 2 DTE/DCE configuration blocks JB 1,2,3 and 4

Transmit data (out)	1	o	o	Connector Pin 2
Connector Pin 4	2	o	o	Receive Data
RTS (out)	3	o	o	Connector Pin 3
CTS (in)	4	o	o	Connector Pin 5
Connector Pin 6	5	o	o	DTR (out)
DCD (in)	6	o	o	Connector Pin 7
Connector Pin 9	7	o	o	RTS (out) •
DCD (in)	8	o	o	Connector Pin 3
+12V through 3k	9	o	o	Connector Pin 7

- A - 3 CLOCK configuration blocks (TTL side) JB5, 6, 7, 8, 9,
 Clock configurations - RS-232C side (JB6,8,10,12)
 (see Appendix F)

	A	B	C
1	o	o	o
2	o	o	o
3	o	o	o

1A Receive Clock Drivers Output
 2A RS-232C Receiver Input
 3A Transmit Clock Driver Output
 1B Connector Pin 12 (EIA DD)
 2B Connector Pin 10 (EIA DA)
 3B Connector Pin 11 (EIA DB)
 1C RS-232C Receiver Input
 2C RS-232C Driver Output
 3C RS-232C Receiver Input

- A - 4 Clock Configurations TTL side (JB5,7,9,11)
 (see Appendix F)

	A	B	C
1	o	o	o
2	o	o	o
3	o	o	o

1A,2B,3A RS-232C Driver Input
 LA On-board Clock Source
 1B SIO Receive Clock
 3B RS-232C Driver
 1C RS-232C Receiver Output
 2C RS-232C Receiver Output
 33C RS-232C Receiver Output

- A - 5 Base Baud Rate Clock JB15

	A	B	
Factory use only	1	o	o
1.2288 MHz	2	o	o
0.6144 MHz	3	o	o

Clock Output

A - 6 Switch Register JB16

	1	2	3	4	5	6	7	8
C	o	o	o	o	o	o	o	o
B	o	o	o	o	o	o	o	o
A	o	o	o	o	o	o	o	o

A1 - A8 - connect to VCC logical '1'
 C1 - C8 - connect to GND logical '0'
 B1 - Switch Register bit 0
 B2 - Switch Register bit 1
 B3 - Switch Register bit 2
 B4 - Switch Register bit 3
 B5 - Switch Register bit 4
 B6 - Switch Register bit 5
 B7 - Switch Register bit 6
 B8 - Switch Register bit 7

A - 7 Switch Register I/O address programming block JB17

Programming the I/O address block involves installing a Jumper for a logic '0' or leaving the jumper out for a logic '1' to create an 8 bit value which is compared with the address bus.

	1	2	3	4	5	6	7	8
B	o	o	o	o	o	o	o	o
A	o	o	o	o	o	o	o	o

A1-A8 Connect to GND
 B1 Compared with I/O address bit 7
 B2 Compared with I/O address bit 6
 B3 Compared with I/O address bit 5
 B4 Compared with I/O address bit 4
 B5 Compared with I/O address bit 3
 B6 Compared with I/O address bit 2
 B7 Compared with I/O address bit 1
 B8 Compared with I/O address bit 0

A - 8 BUSAK chain JB18

This Jumper is normally installed in Z80 based systems.

A - 9 Serial I/O address programming block

This block sets the position of the 16 I/O ports associated with the 4 serial channels. Row A is connected to VCC providing a logic '1' and row C is connected to GND providing a logic '0'. Each of the 4 address comparator input (B1 - B2) must be connected to

a logic '0' or logic '1'.

	1	2	3	4
C	o	o	o	o
B	o	o	o	o
A	o	o	o	o

A1 - A4	logic '1'
C1 - C4	logic '0'
B1	compared with address bit 4
B2	compared with address bit 5
B3	compared with address bit 6
B4	compared with address bit 7

TABLE A-1

DSTD-202 STANDARD CABLE CONNECTORS FOR DB25S CONNECTORS

SIGNAL NAME	DS1D-202 BOARD CONNECTOR PIN NUMBER	DB25S CONNECTOR PIN NUMBER	E1A
Ground	1	1	AA
Transmitted Data	2	2	BA
Request To Send	3	4	CA
Received Data	4	3	BB
Clear To Request	5	5	CB
Data Terminal Ready	6	20	CD
DATA Set Ready	7	6	CC
Ground	8	7	AB
Data Carrier Detect	9	8	CF
Transmission Timing (DTE SOURCE)	10	24	DA
Transmission Timing (DCE SOURCE)	11	15	DB
Receiver Timing (DCE SOURCE)	12	17	DD

APPENDIX B

STD-Z80 BUS PIN OUT

APPENDIX B

STD-Z80 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	Ground - System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	
15	A7	
16	A15	
17	A6	Address Bus (Tri-state, output, active high).
18	A14	

STD-Z80 BUS PIN OUT

19	A5	A0-A15 make up a 16-bit address bus. The address bus provides the address for memory (up to 65k bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A6	
31	/WR	Memory Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Memory Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-State output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 Systems DSTD.

STD-Z80 BUS PIN OUT

36	/MEMEX	Memory expansion, not used on dy-4 Systems DSTD cards.
37	/REFRESH	/REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic zero and the upper 8 bits of the address bus contains the I register.
38	/DEBUG	/DEBUG (Input) used in conjunction with DDT-80 operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the /DEBUG line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
39	/M1	Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the opcode fetch cycle of an instruction. Note that during the execution of a 2-byte opcodes, /M1 will be generated as each opcode is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
40	STATUS 0	DMA priority chain input.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

STD-Z80 BUS PIN OUT

- 42 /BUSRQ Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.
- 43 /INTAK Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.
- 44 /INTRQ Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.
- 45 /WAITRQ WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

46	/NMIRQ	Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will over-ride a /NMIRQ.
47	/SYSRESET	System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H and set Interrupt Mode 0.
48	/PBRESET	Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset.
49	/CLOCK	Processor Clock (Output, active low). Single phase system clock.
50	CNTRL	Auxiliary Timing
51	PCO	Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

STD-Z80 BUS PIN OUT

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.

APPENDIX C
PARTS LIST

APPENDIX C

DSTD-202 PARTS LIST

PRODUCT PART LIST
PD920200 - DSTD 202 2.5 REV 1

84/04/12

Page 1

DY4PART	QTY	DESCRIPTION	DESIGNATION
PT012009	1	74LS08 TTL-LS	U17
PT012011	1	74LS11 TTL-LS	U18
PT012085	1	74LS85 TTL-LS	U27
PT012244	3	74LS244 TTL-LS	U20,U24,U26
PT012245	1	74LS245 TTL-LS	U23
PT012393	1	74LS393 TTL-LS	U21
PT012682	1	74LS682 TTL-LS	U25
PT013004	1	74S04 TTL-S	U22
PT015013	2	MK3882n (280-CTC) 2.5 MHZ CTC	U13,U14
PT015021	2	MK3887n 2.5 MHZ S10/2	U15,U16
PT016001	6	75188 OR MC1488 INTERFACE	U1,U2,U3,U4,U5,U6
PT016002	6	75189 OR MC1489 INTERFACE	U7,U8,U9,U10,U11,U12
PT026002	1	PAL16L8	U19
PT041331	1	1/4 WATT, 330 OHM, 5% RESISTOR	R3
PT041471	2	1/4 WATT, 470 OHM, 5% RESISTOR	R4,R5
PT041472	3	1/4 WATT, 4.7K OHM, 5% RESISTOR	R1,R2,R6
PT043002	1	6 PIN, 5 RESISTOR, 4.7K OHM SIP RESISTOR NETWORK	RN1
PT043017	1	10 PIN, 9 RESISTOR, 4.7K OHM, SIP RESISTOR NETWORK	RN2
PT051006	2	85200/4.7uf, 40V RADIAL ELECTROLYTIC CAPACITOR	C31,C33
PT052004	24	CK05BX331K,330pf, 200V CERAMIC CAPACITOR	C5-14,16-23,25-29,30,32
PT052005	1	CK05BX471K, 470pf, 200V CERAMIC CAPACITOR	C45
PT053000	1	TA010M25, 10uf, 25V TANTALUM CAPACITOR	C44
PT059000	21	.1uf 63V, (.2 LD. SP.)1R37104M,POLYESTER FILM CAPACITOR	C1-4,15,24,29,34-37,39-43
PT059000	0	.1uf 63V, (.2 LD. SP.)1R37104M,POLYESTER FILM CAPACITOR	C46,C47,C48,C49,C50
PT073001	2	1N4001 RECTIFIER	D1,2
PT102006	1	FOX 19.6608 MHZ DISCRETE CRYSTAL	Y1
PT122003	3	CHD6960WIS 60 PIN DOUBLE ROW HEADER	JB1-JB12,JB15,JB16,JB17,JB19
PT122004	2	CHS6936WIS 36 PIN SINGLE ROW HEADER	JB5-JB12,JB16,JB18,JB19
PT123003	4	87516-2 12 PIN RIGHT ANGLE CONNECTOR (AMP ONLY)	J1-4
PT124020	1	640464-3 20 PIN I.C. SOCKET	U19
PT124029	2	640362-3 28 PIN I.C. SOCKET	U13,U14
PT124040	2	640372-3 40 PIN I.C. SOCKET	U15,U16
PT129003	41	.1 INSULATED SHORTING JACK #15-38-1024 OR #450-2212-01-03-10	
PT344601	1	DSTD 202 DY00446-H-A1-1	
PT711006	1	202 MANUAL	

APPENDIX C

DSTD-202 PARTS LIST

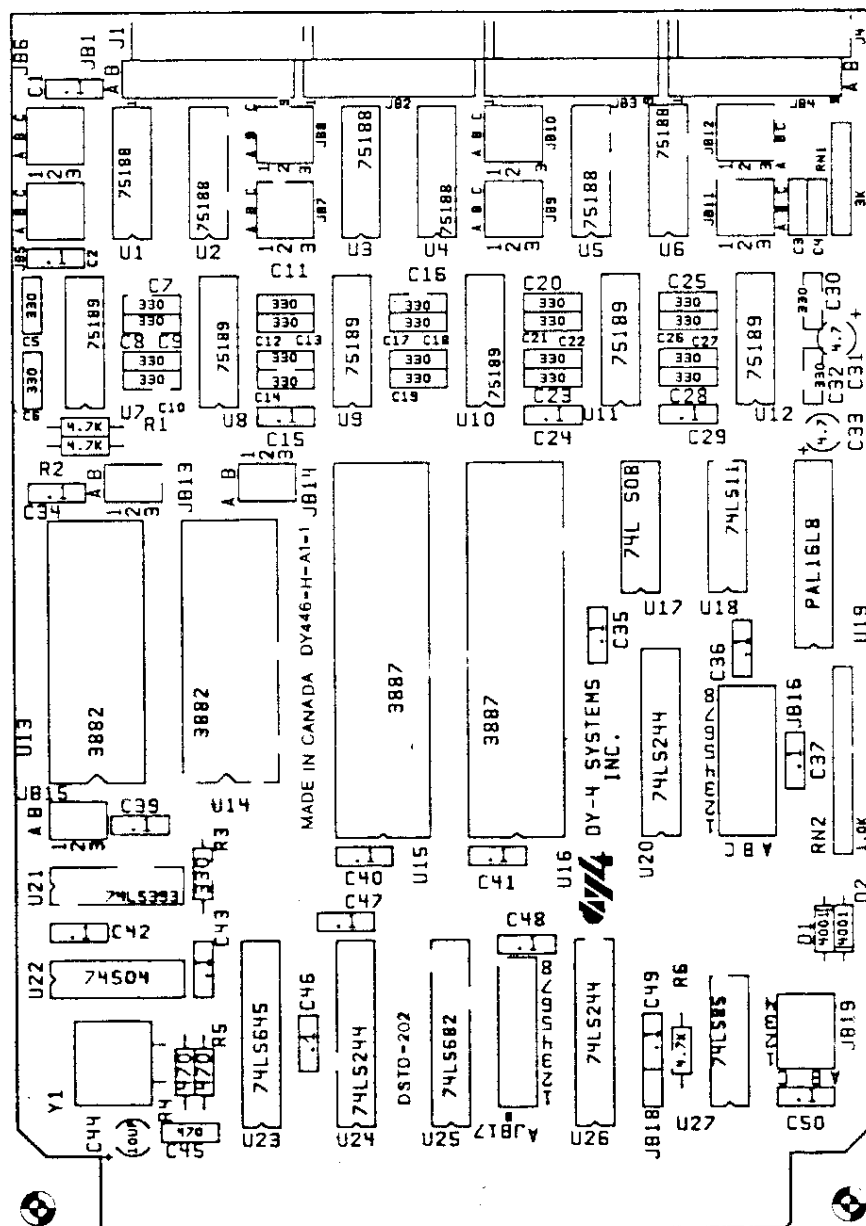
PRODUCT PART LIST
PDP20201 - DSTD 202 4.0 REV 1

84/04/12

Page 1

DY4PART	QTY	DESCRIPTION	DESIGNATION
PT012008	1	74LS08 TTL-LS	U17
PT012011	1	74LS11 TTL-LS	U18
PT012085	1	74LS85 TTL-LS	U27
PT012244	3	74LS244 TTL-LS	U20,U24,U26
PT012245	1	74LS245 TTL-LS	U23
PT012393	1	74LS393 TTL-LS	U21
PT012482	1	74LS682 TTL-LS	U25
PT013004	1	74S04 TTL-S	U22
PT015014	2	MK3882n-4 (280A-CTD) 4.00 MHZ CTD	U13,U14
PT015022	2	MK3887n-4 (280A-S10/2) 4.00 MHZ S10/2	U15,U16
PT016001	6	75188 OR MC1488 INTERFACE	U1,U2,U3,U4,U5,U6
PT016002	6	75189 OR MC1489 INTERFACE	U7,U8,U9,U10,U11,U12
PT036002	1	PAL16L8	U19
PT041331	1	1/4 WATT, 330 OHM, 5% RESISTOR	R3
PT041471	2	1/4 WATT, 470 OHM, 5% RESISTOR	R4,R5
PT041472	3	1/4 WATT, 4.7K OHM, 5% RESISTOR	R1,R2,R6
PT043002	1	6 PIN, 5 RESISTOR, 4.7K OHM SIP RESISTOR NETWORK	RN1
PT043017	1	10 PIN, 9 RESISTOR, 4.7K OHM, SIP RESISTOR NETWORK	RN2
PT051006	2	85200/4.7uf, 40V RADIAL ELECTROLYTIC CAPACITOR	C31,C33
PT052004	24	CK05BX331K,330pf, 200V CERAMIC CAPACITOR	C5-14,16-23,25-26,30,32
PT052005	1	CK05BX471K, 470pf, 200V CERAMIC CAPACITOR	C45
PT053000	1	TAG10M25, 10uf, 25V TANTALUM CAPACITOR	C44
PT059000	21	.1uf 63V, (.2 LD. SP.)1R67104M,POLYESTER FILM CAPACITOR	C1-4,15,24,29,34-37,39-43,
PT059000	0	.1uf 63V, (.2 LD. SP.)1R67104M,POLYESTER FILM CAPACITOR	C46,C47,C48,C49,C50
PT073001	2	1N4001 RECTIFIER	D1,2
PT102006	1	FOX 19.6608 MHZ DISCRETE CRYSTAL	Y1
PT122003	3	CHD6960W1S 60 PIN DOUBLE ROW HEADER	JB1-JB12,JB15,JB16,JB17,JB19
PT122004	2	CHS6930W1S 36 PIN SINGLE ROW HEADER	JB5-JB12,JB16,JB18,JB19
PT123003	4	87516-2 12 PIN RIGHT ANGLE CONNECTOR (AMP ONLY)	J1-4
PT126020	1	640464-3 20 PIN I.C. SOCKET	U19
PT126029	2	640362-3 28 PIN I.C. SOCKET	U13,U14
PT126040	2	640379-3 40 PIN I.C. SOCKET	U15,U16
PT129006	41	.1 INSULATED SHORTING JACK #15-38-1024 OR #450-2212-01-03-10	
PT344601	1	DSTD 202 DY00446-H-A1-1	
PT711006	1	202 MANUAL	

FIGURE C-1 DSTD-202 SILK SCREEN

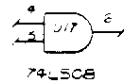


APPENDIX D
SCHEMATIC

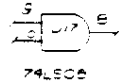
ISSUE	DESCRIPTION	DATE	DRN	CHK
-------	-------------	------	-----	-----

TYPE	+5V _I	-5V _I	+12V _I	-12V _I	GND
74LS02	14				7
74LS04	14				7
74LS08	14				7
74LS11	14				7
74LS85	6				8
74LS138	16				9
74LS244	20				10
74LS373	14				7
74LS645	20				10
74LS682	20				10
75100	14				7
75109	4				7
3002	24				1
3007	9				31

UNUSED GATES



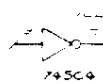
74LS08



74LS08



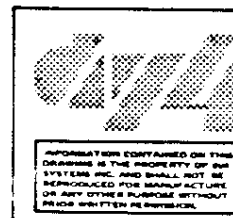
74LS04



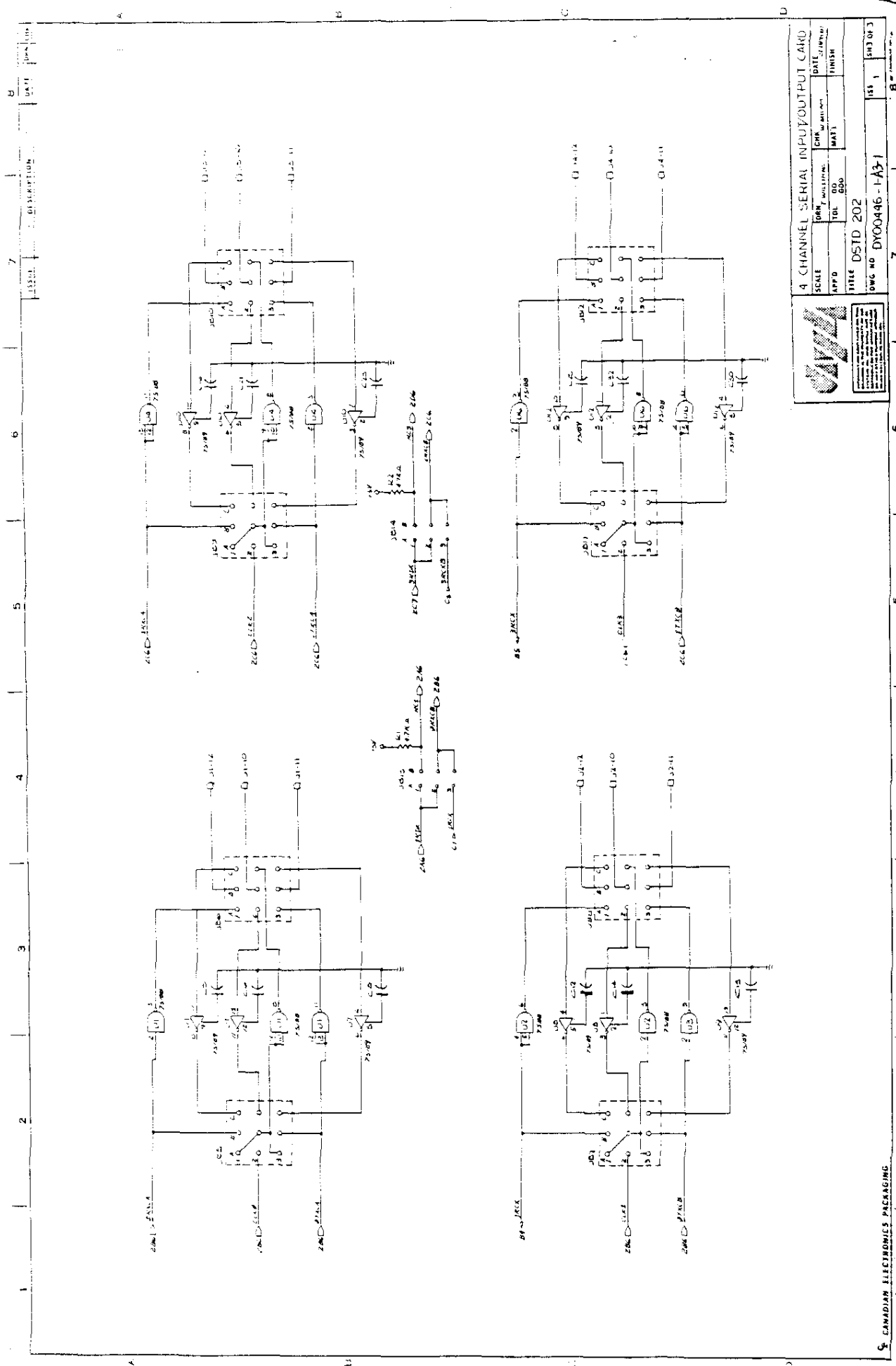
74LS04



74LS04

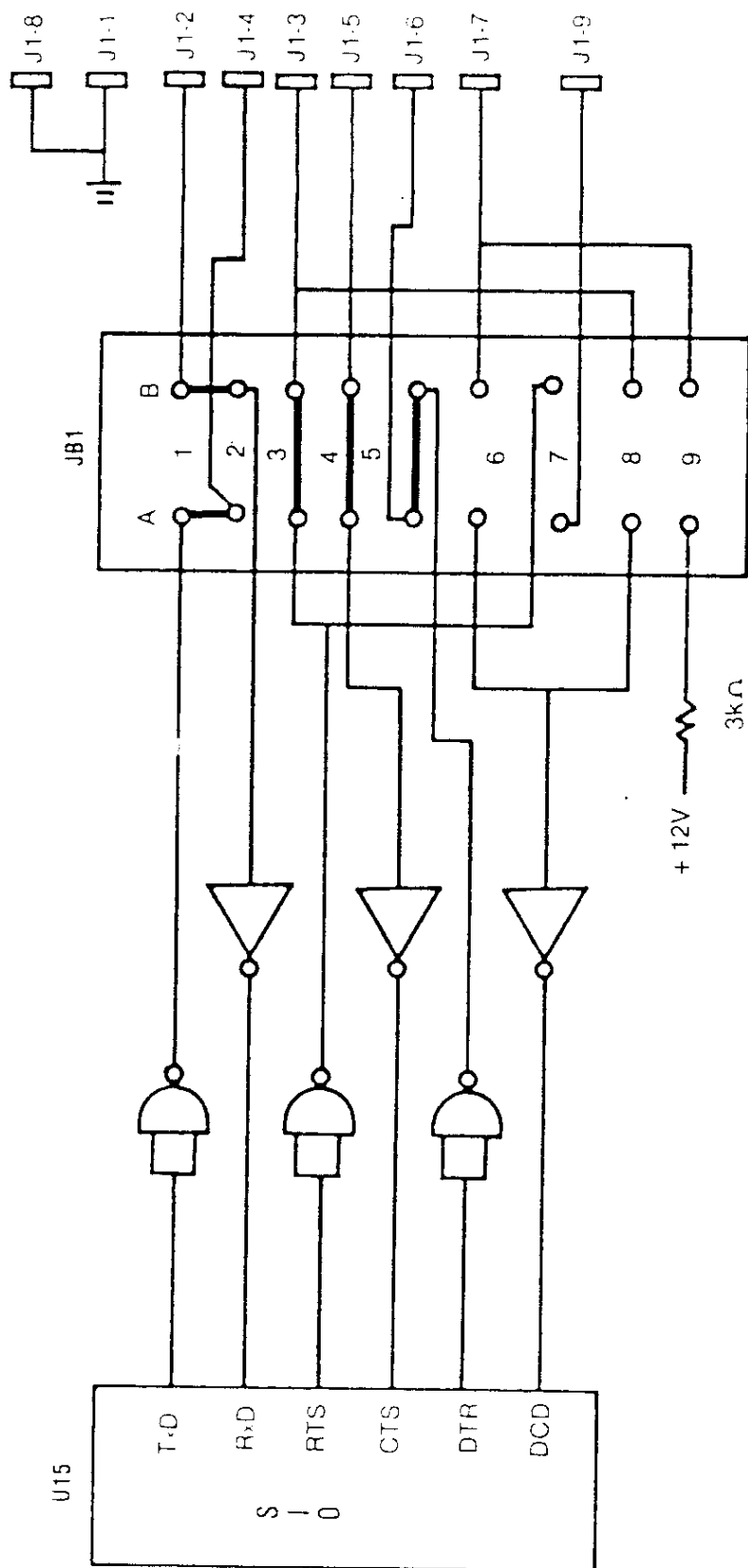


4 CHANNEL SERIAL INPUT/OUTPUT CARD			
SCALE	DRN WILLIAMS	CHK W. MILAM	DATE 27 APR 81
APP'D	TOL .00 .000	MAT'L	FINISH
TITLE DSTD 202			
DWG NO. DY00446-1-A1-1			ISS 1 SH 1 OF



4 CHANNEL SERIAL INPUT/OUTPUT CARD			
SCALE	DATE	CHK BY	DATE
APPD	TOL	DO	FINISH
TITLE D51D 202			
DWG NO DY00446-1A3-1			
155 1 8			

APPENDIX E
FACTORY PRESET JUMPERS



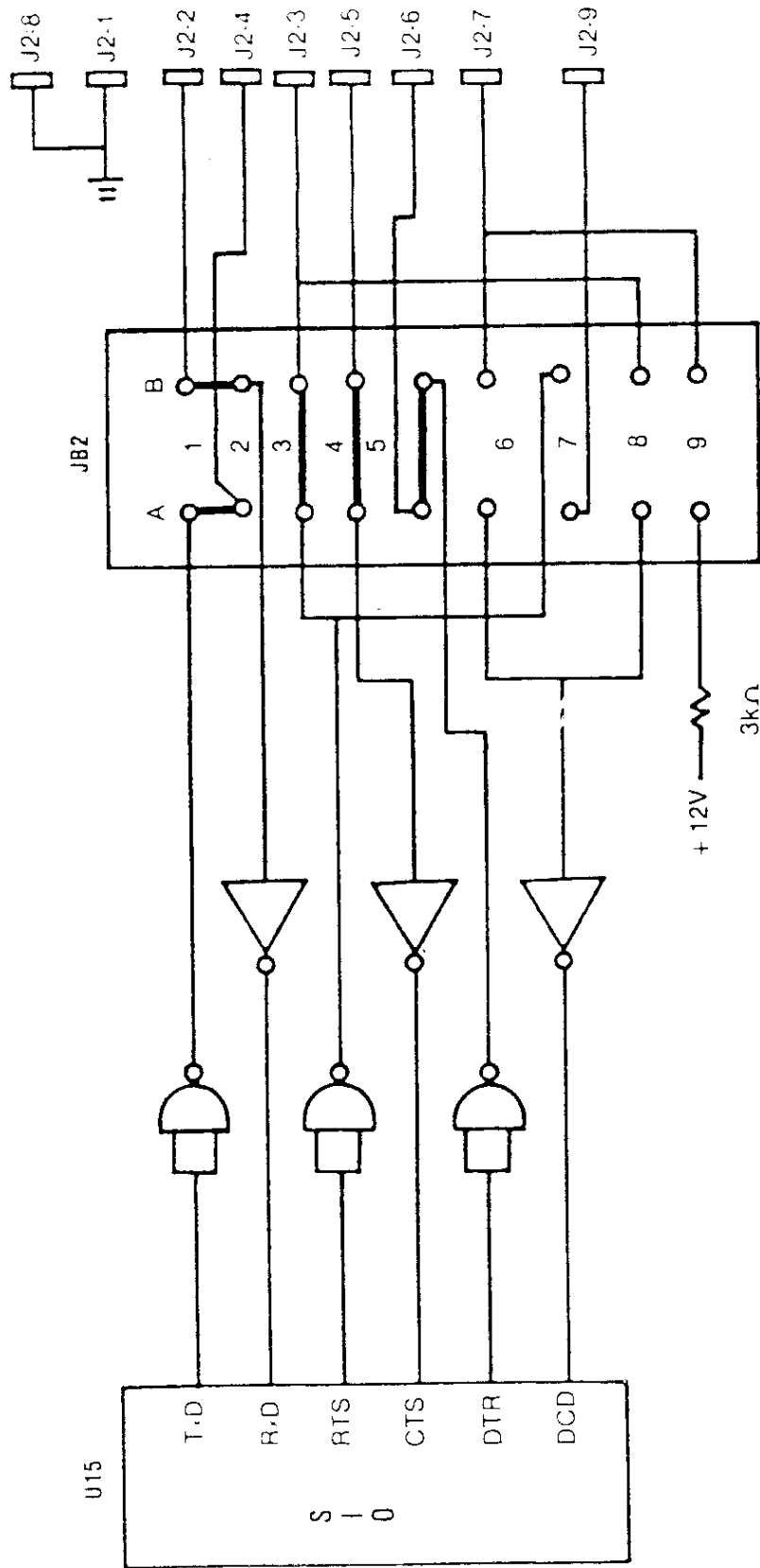


Figure E-2 - Port B DCE/OTE Header Programmer

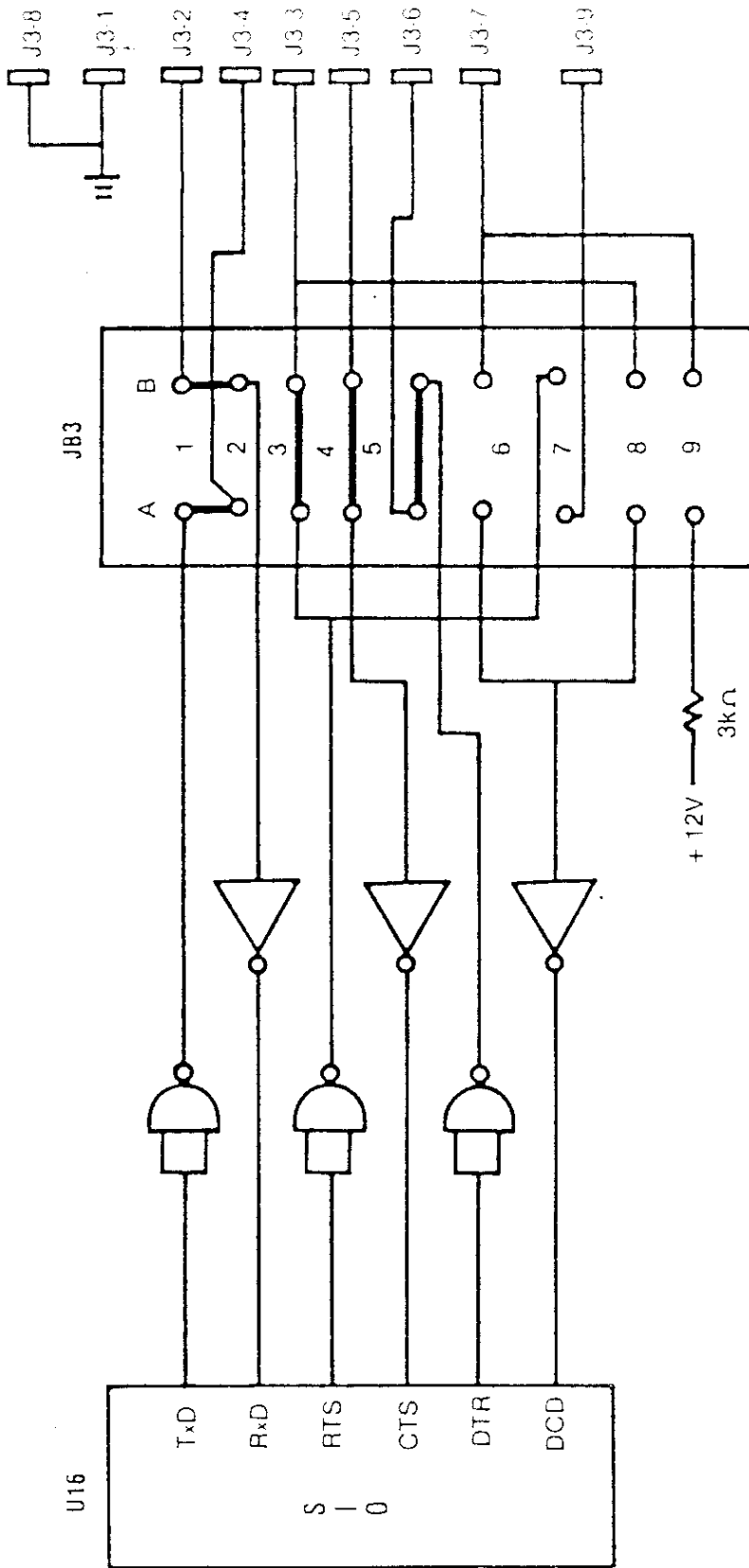


Figure E-3 - Port C DCE/DTE Header Programmer

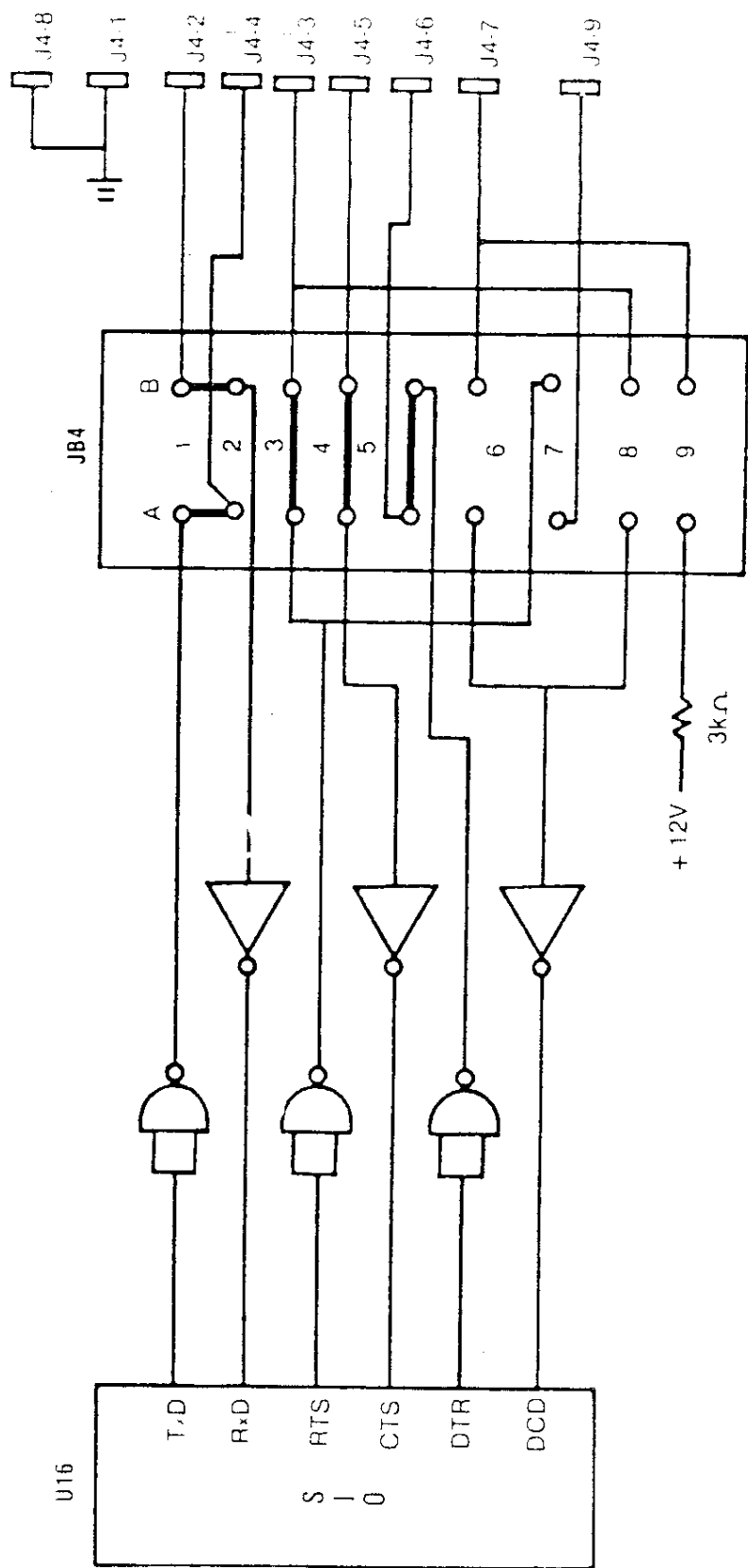


Figure E-4 - Port D DCE/DTE Header Programmer

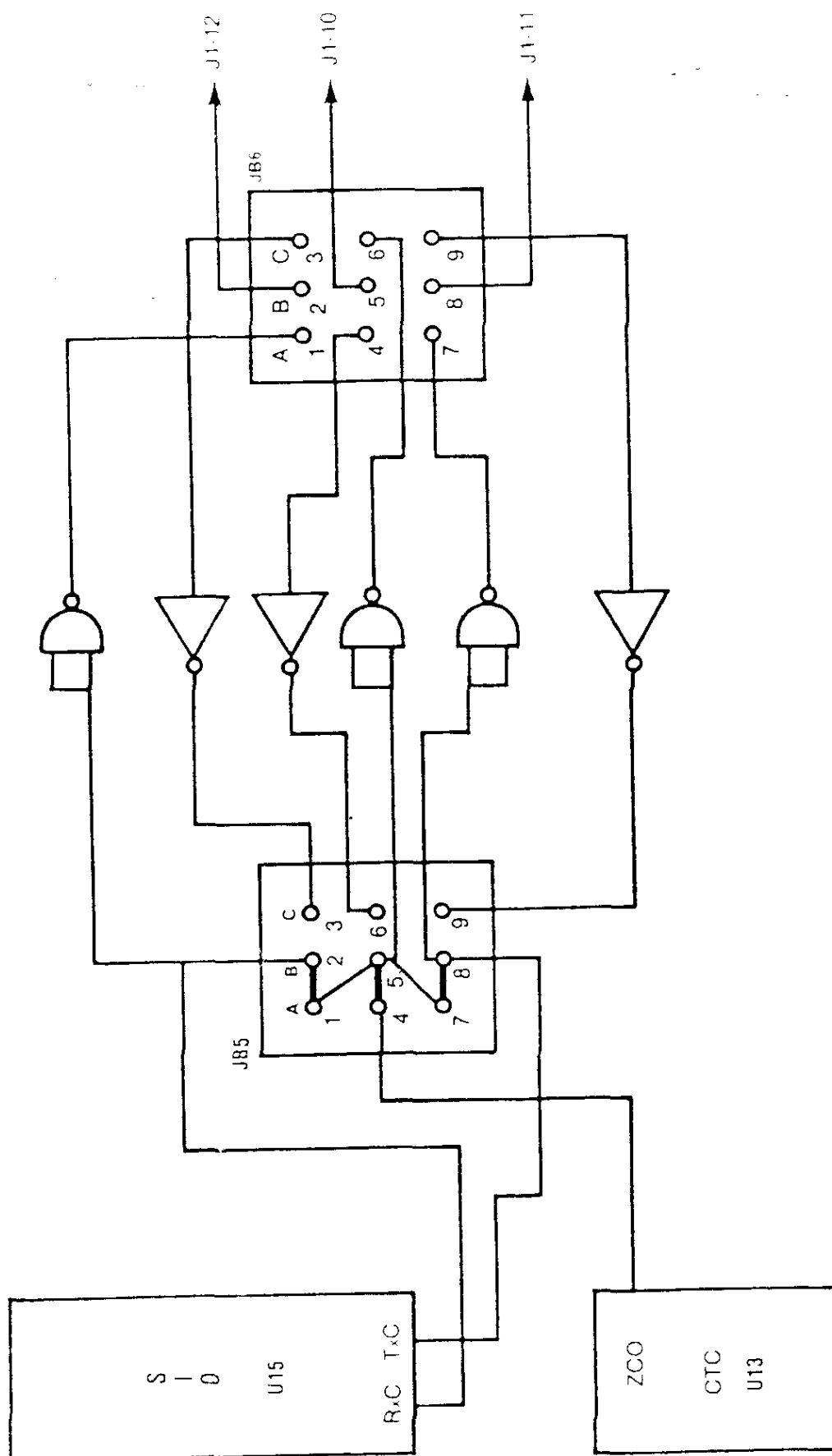


Figure E-5 Port A Clock Jumper Configuration

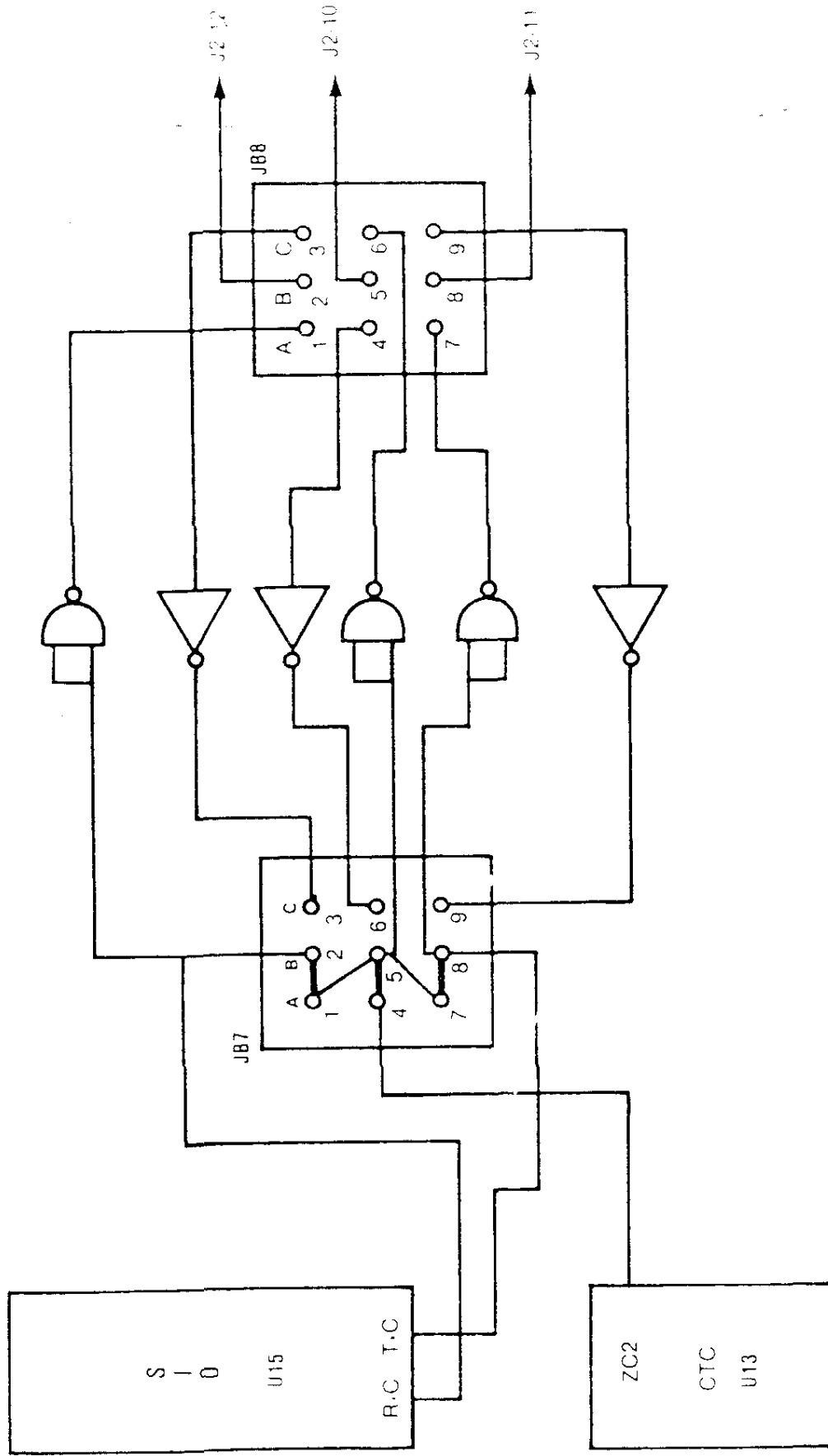


Figure E-6 Port B Clock Jumper Configuration

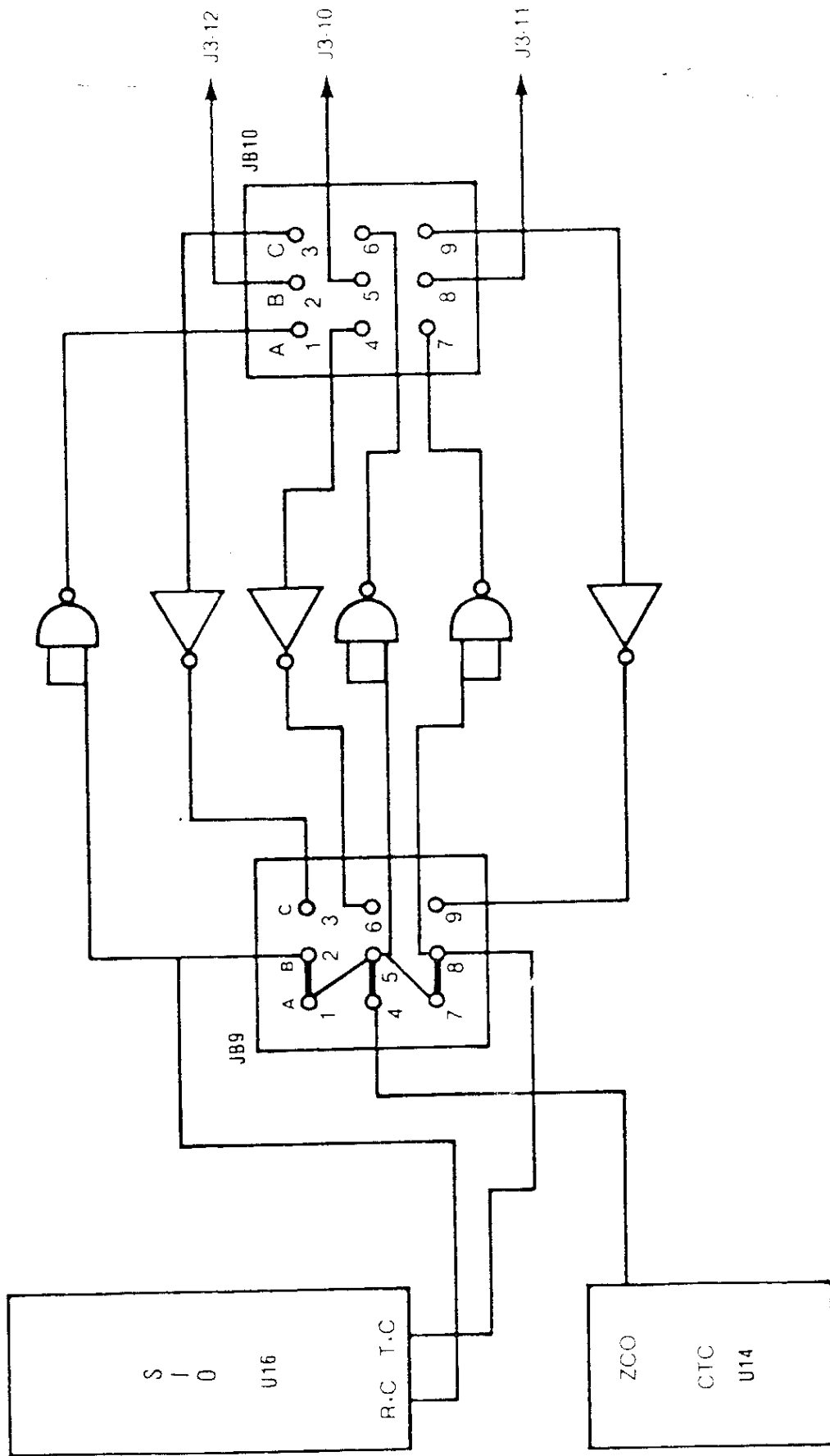


Figure E-7 Port C Clock Jumper Configuration

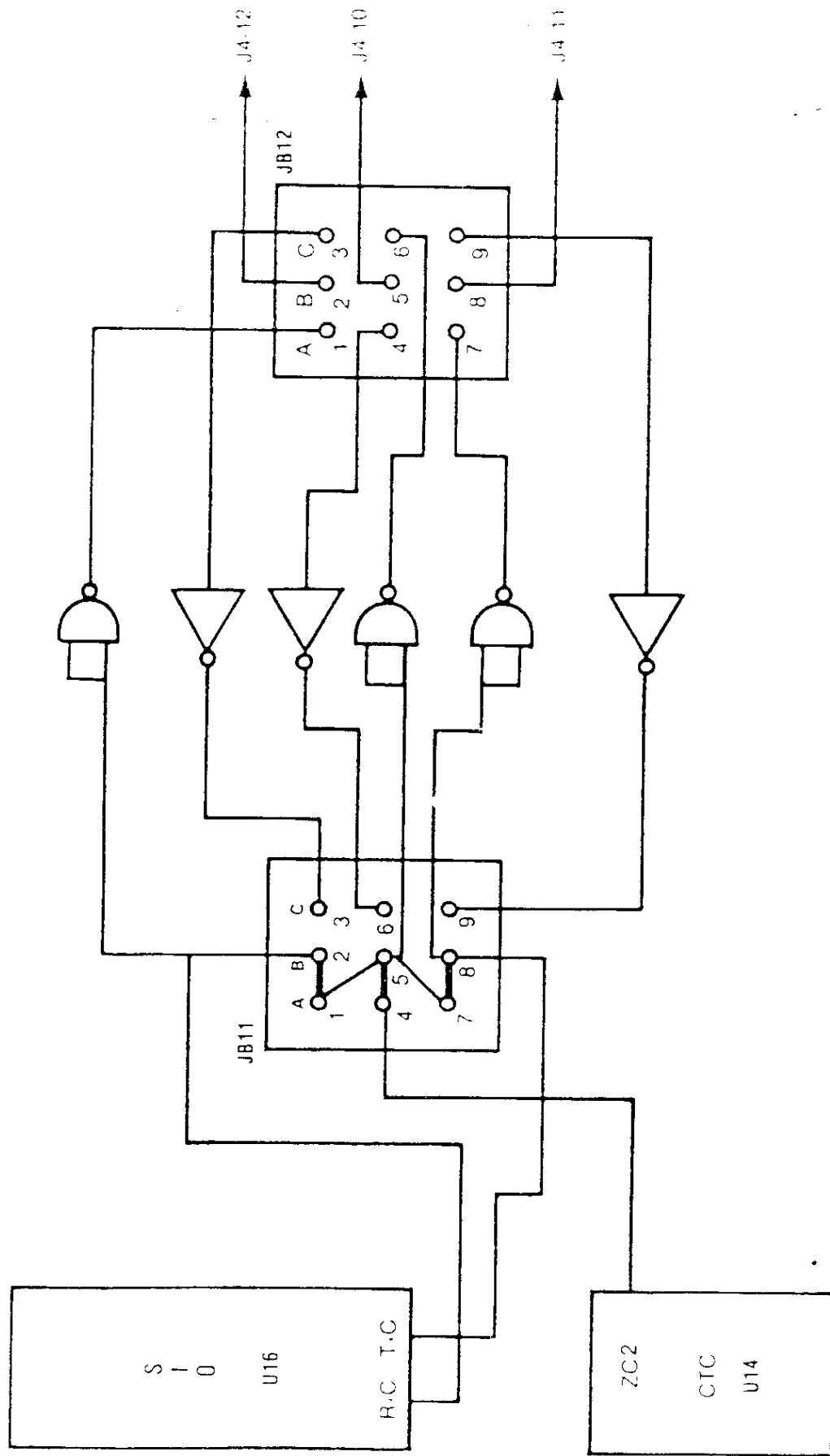
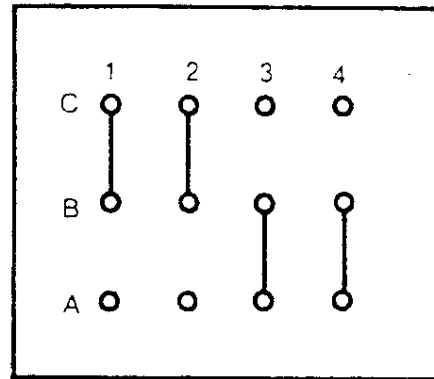


Figure E-8 Port D Clock Jumper Configuration

JB19



Base Address B0H

Figure E-9 I/O Port Address Jumper

APPENDIX F
USER JUMPER WORKSHEETS

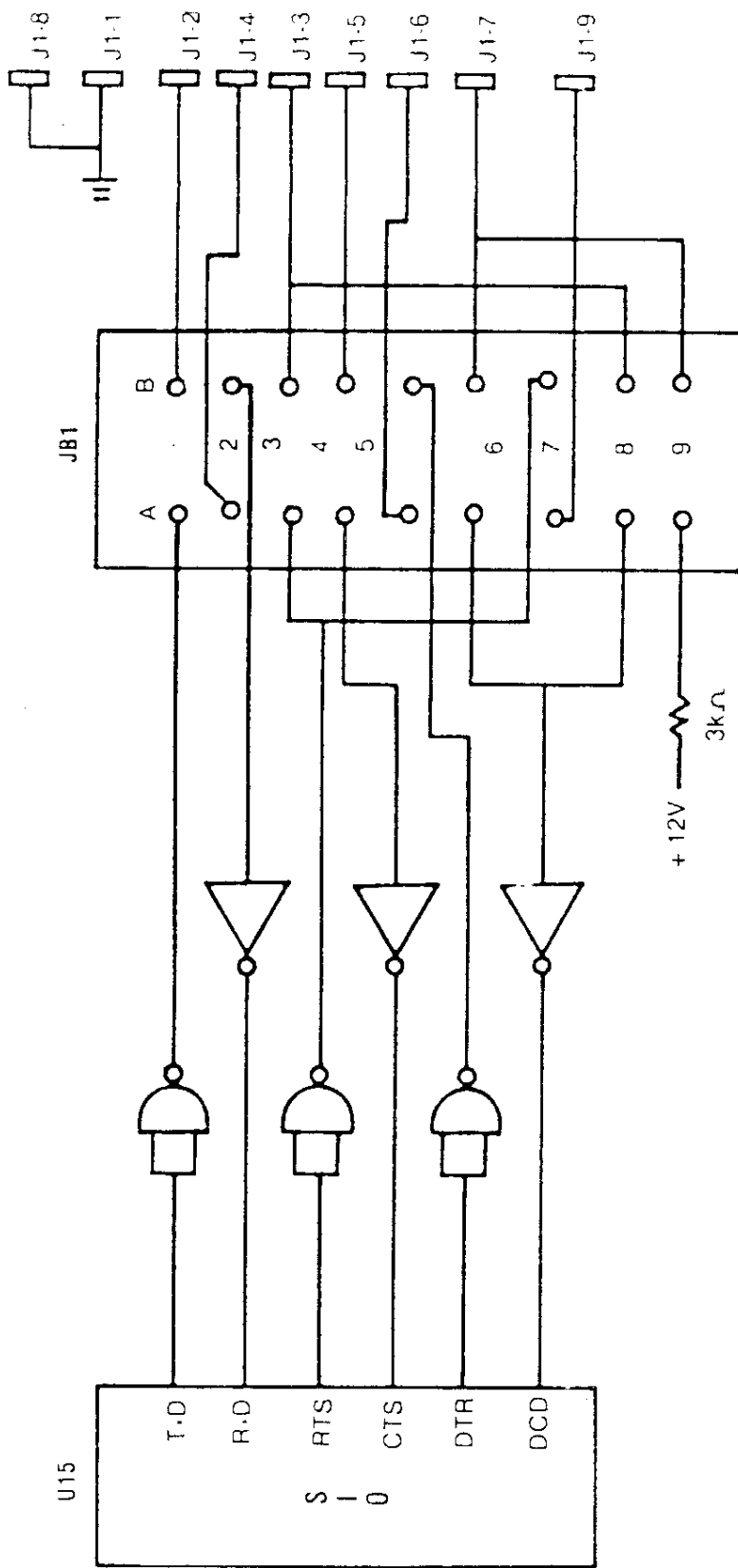


Figure F-1 - Port A DCE/DTE Header User Assignment

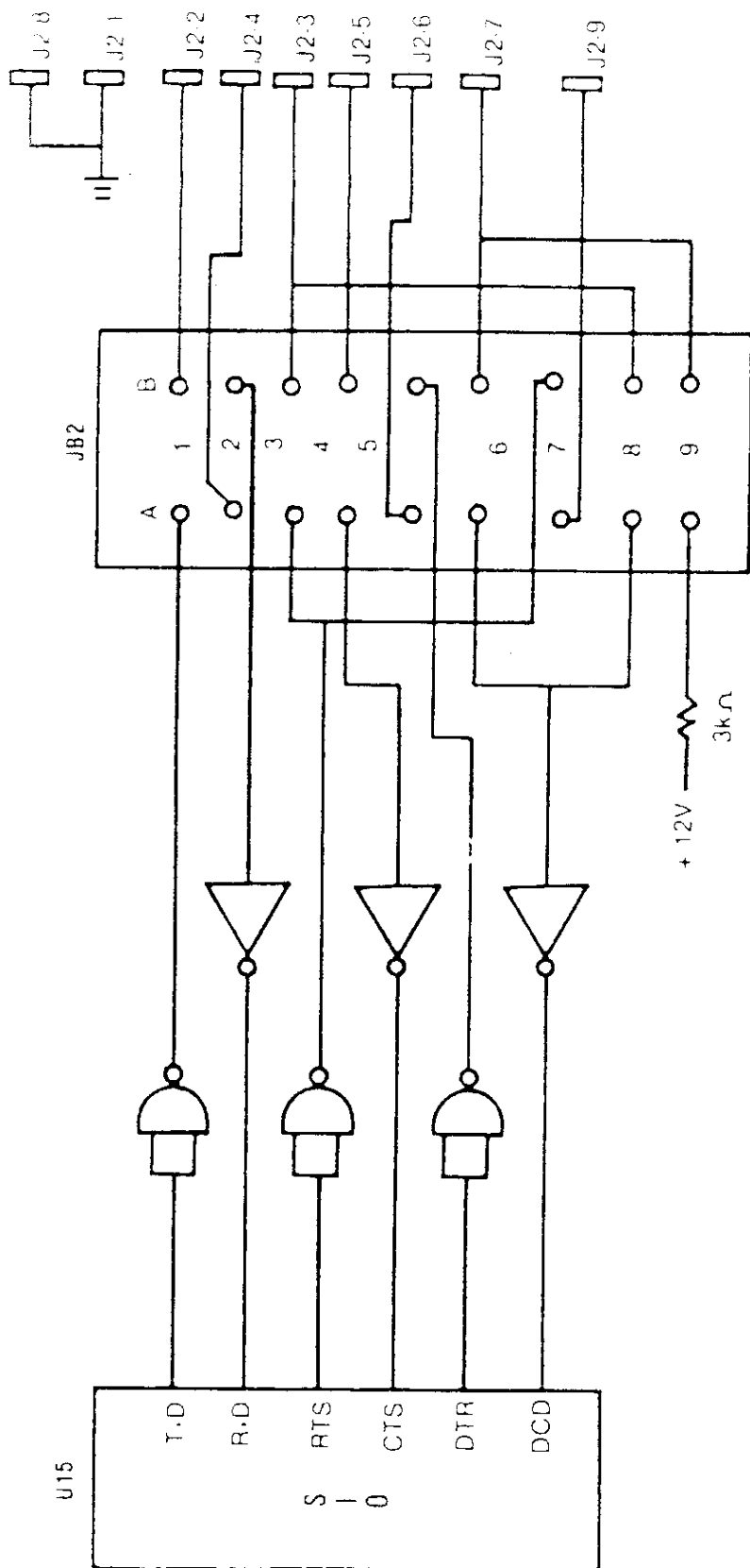


Figure F-2 - Port B DCE/DTE Header User Assignment

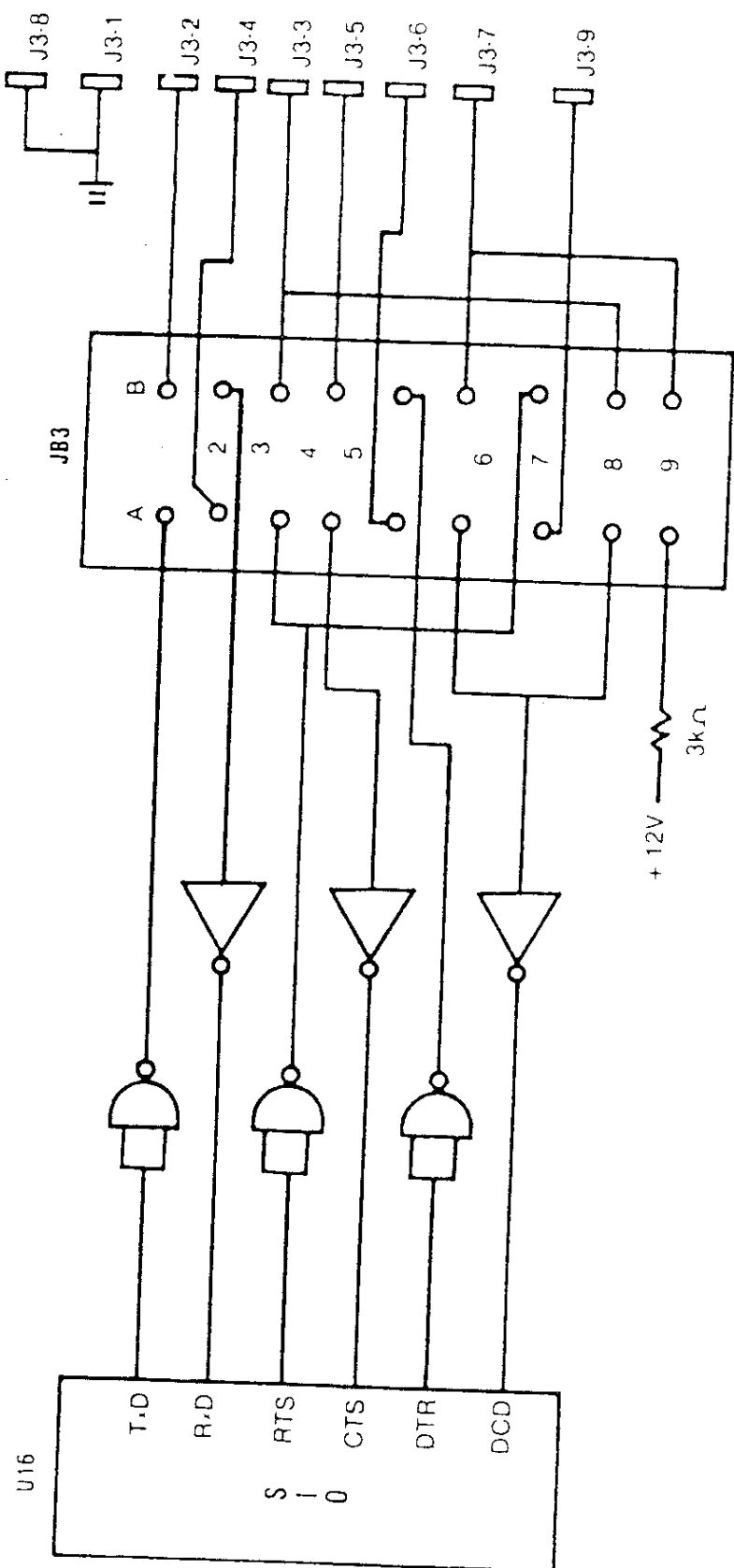


Figure F-3 - Port C DCE/DTE Header User Assignment

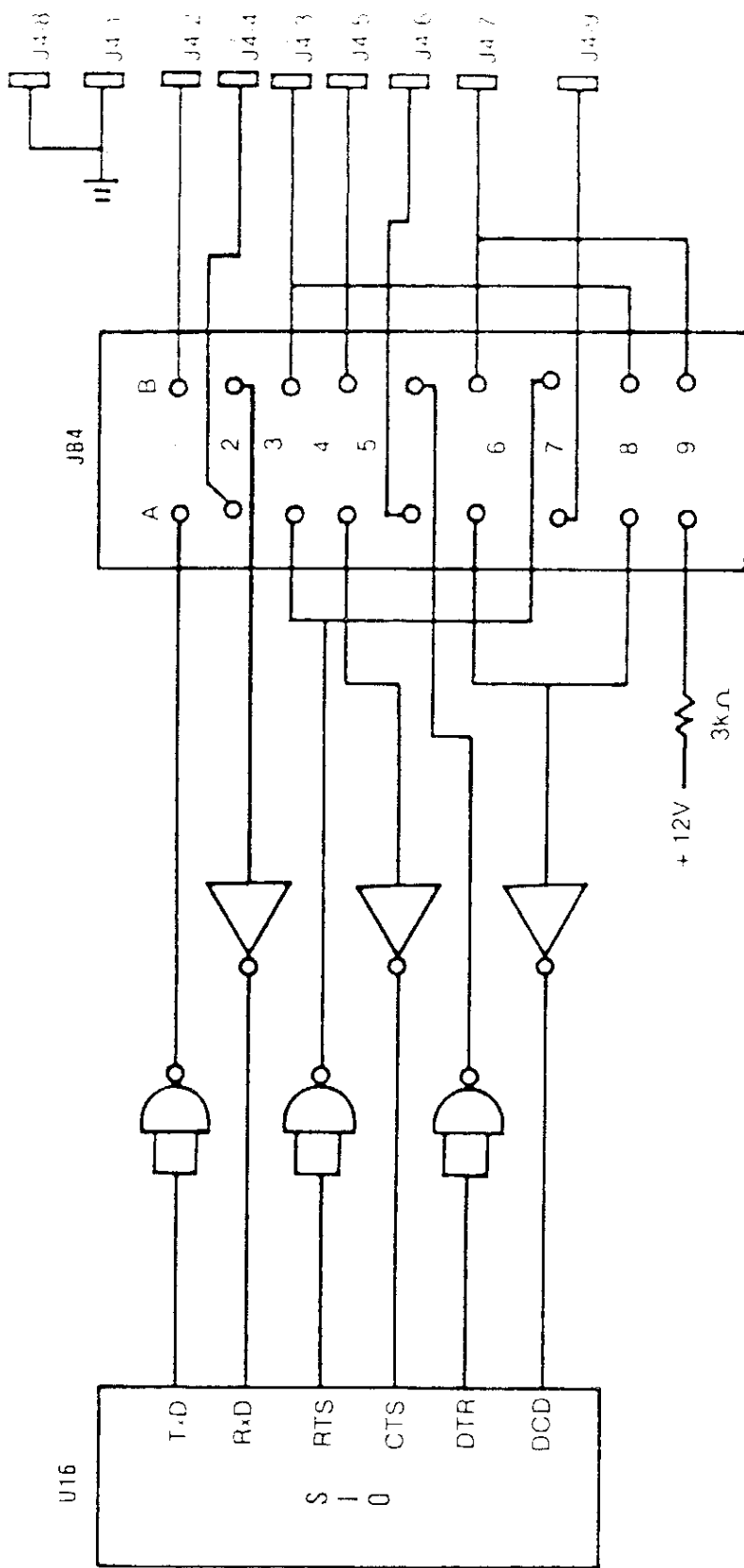


Figure F-4 - Port D DCE/DTE Header User Assignment

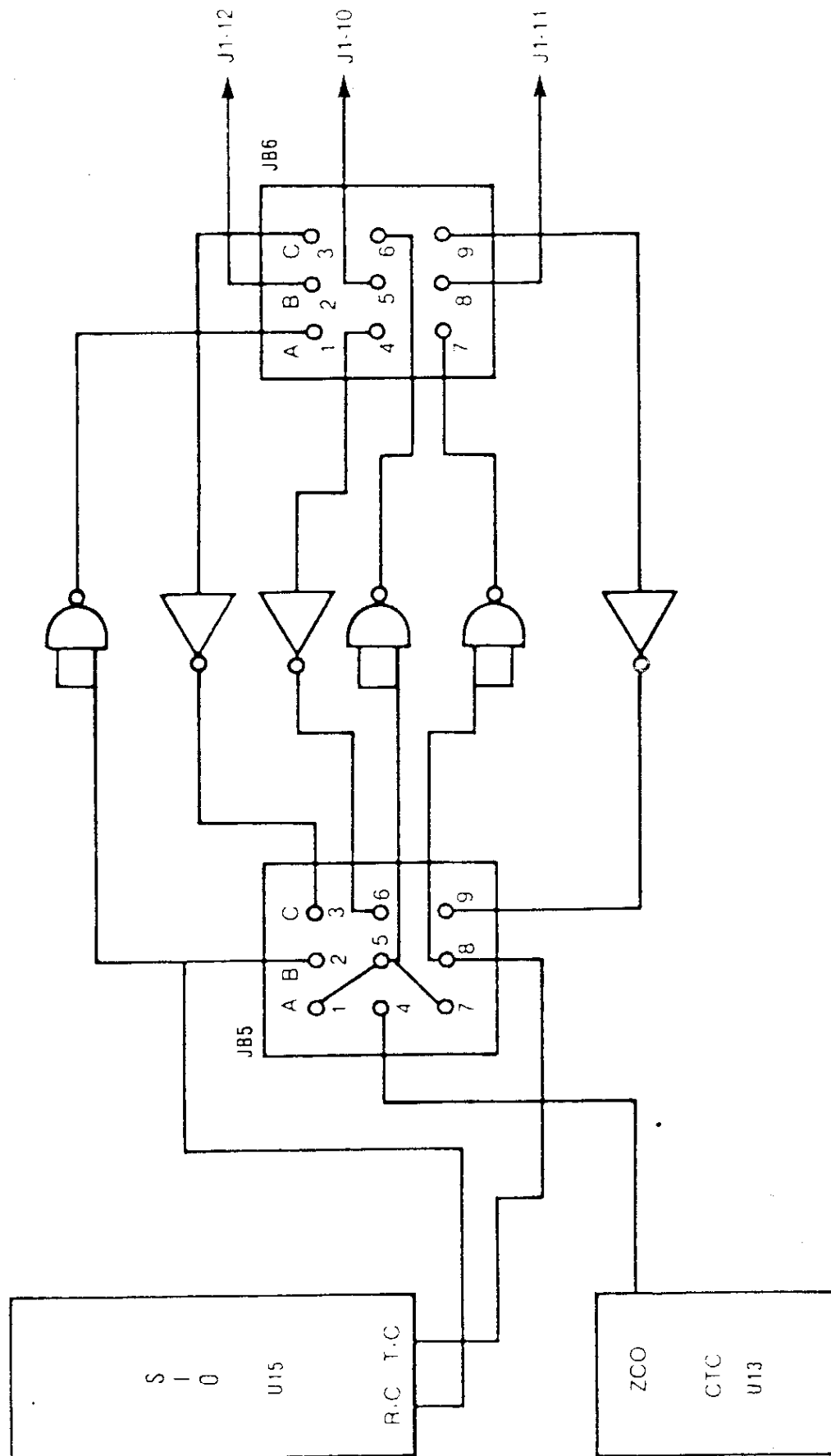


Figure F-5 Part A Clock Jumper Configuration User Assignment

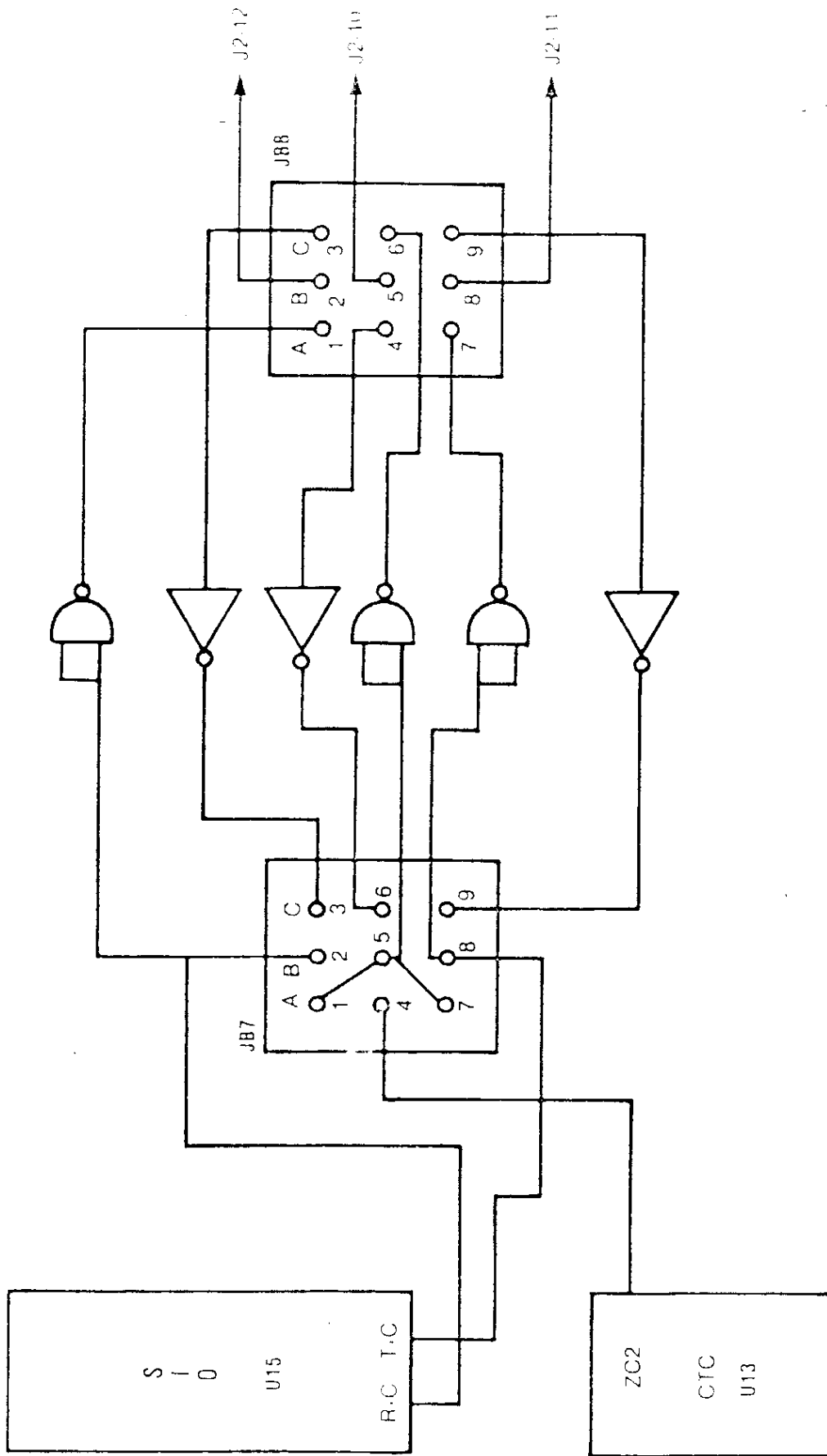


Figure F-6 Port B Clock Jumper Configuration User Assignment

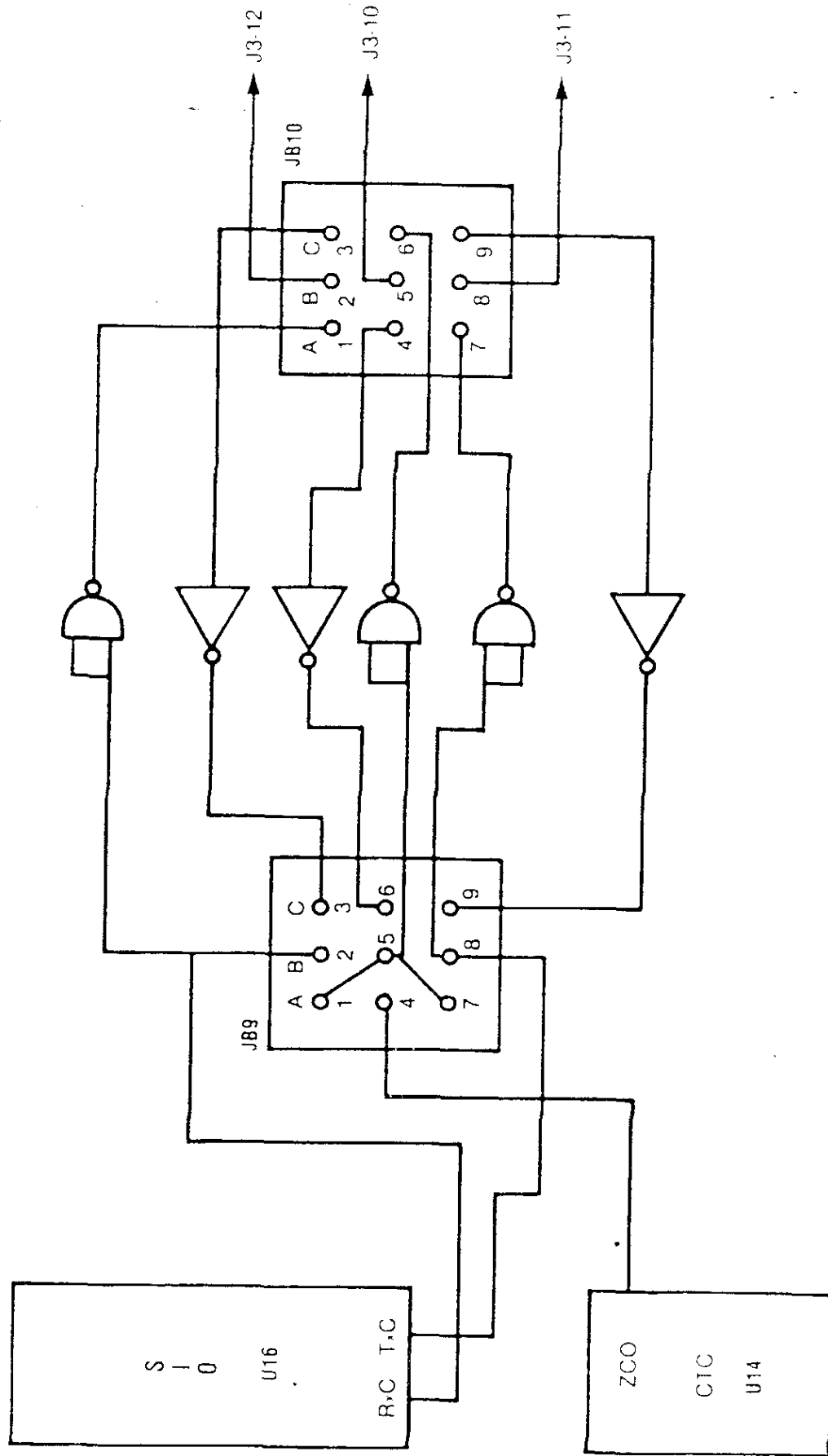
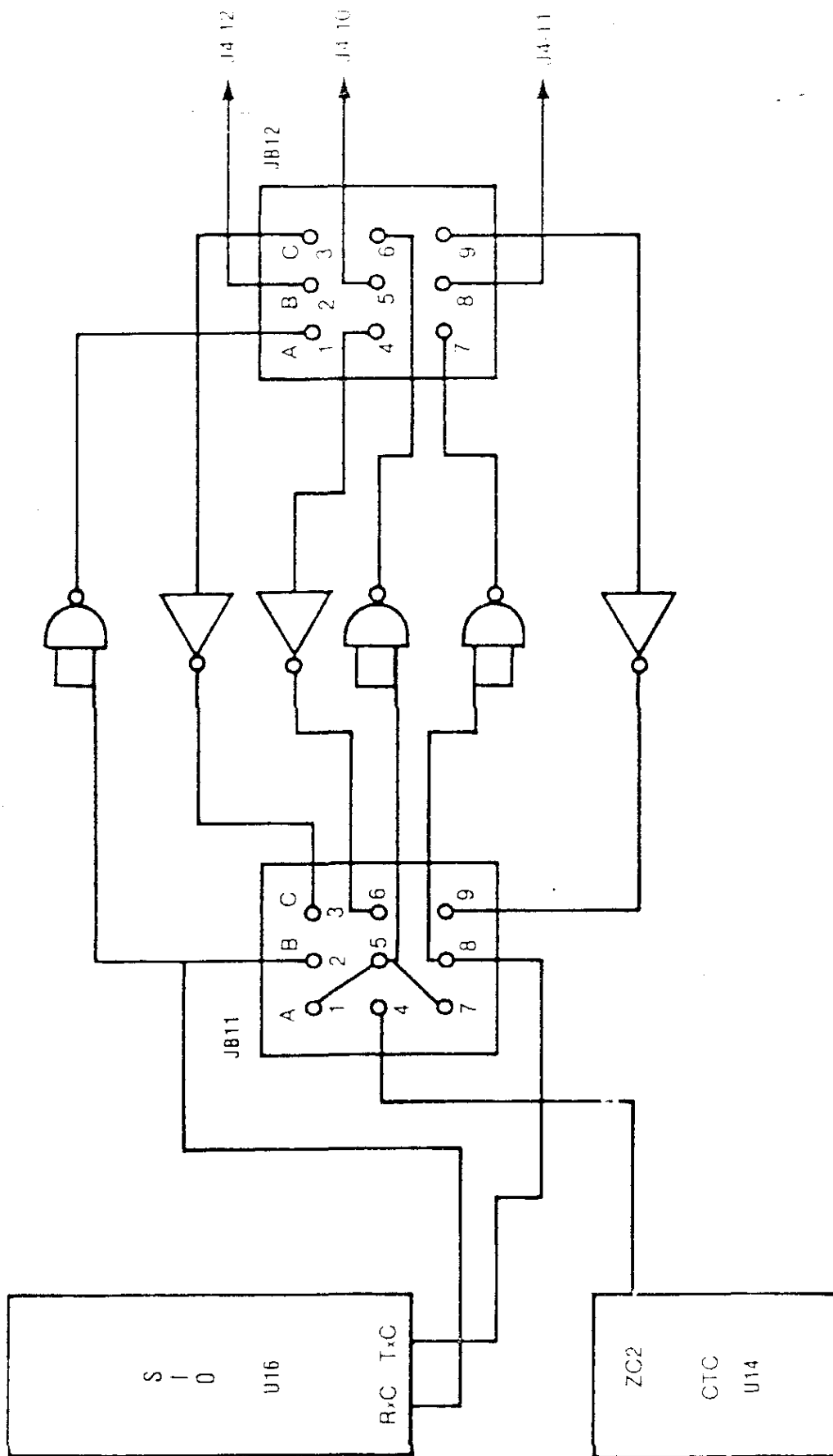


Figure F-7 Port C Clock Jumper Configuration User Assignment



F-9

Figure F-8 Port D Clock Jumper Configuration User Assignment