

# OPERATIONS MANUAL

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**DSTD  
328** 256K DYNAMIC  
MEMORY  
MODULE

FOR THE  
DSTD-188 8088 CARD  
DY00513

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**dy-4 Systems Inc.**

DOCUMENT NO. DSTD-328-M  
REVISION A

STD-328  
256K DYNAMIC MEMORY MODULE  
FOR THE DSTD-188 8088 CARD  
OPERATIONS MANUAL

DY00513

PREPARED BY: dy-4 SYSTEMS INC.

DATED: APRIL 10th, 1983

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## Acknowledgements

Z-80 is a Trademark of Zilog, Inc.

## SECTION 1

### 1.0 GENERAL INFORMATION

#### 1.1 Introduction

The DSTD-328 is a 256 kilobyte dynamic RAM card designed as a companion card to the DSTD-188. The DSTD-188 is a 8088 based CPU card with a 1 megabyte addressing capability. The DSTD-328 is positioned within the 1 megabyte address space using a hardwired jumper block. The card can be enabled and disabled under software control allowing more than four cards to be used in a system using paging techniques. The DSTD-188 provides the dynamic RAM refresh function.

#### 1.2 DSTD Series General Description

The dy-4 SYSTEMS DSTD Series of Z80 and 8088 STD-Bus compatible products was designed to satisfy the need for high performance microcomputer modules that could be quickly and inexpensively integrated into a variety of end-user applications. The popular STD-Bus motherboard interconnect system concept provides expandability as needs change. Support by numerous manufacturers provides the user with a choice from scores of compatible products.

The modules are a compact 4.5 x 6.5 inches (11.4 X 16.5 cm) which provides for system partitioning by function, i.e. CPU, Memory, I/O, etc. dy-4 SYSTEMS has been able to combine most popular functions on single cards to reduce system card count and cost.

#### 1.3 DSTD-328 Features

The dy-4 SYSTEMS DSTD-328 is a very dense dynamic memory module designed for use with dy-4 SYSTEMS DSTD Series STD Bus products.

The DSTD-328 supports the full 20 bit address bus of the 8088 using the data bus to receive the top 4 address bits.

It is available configured with or without Parity generation/checking logic. The optional parity generation and checking circuitry provides error detection automatically. The error condition is latched to allow checking on completion of memory transfers or accesses.

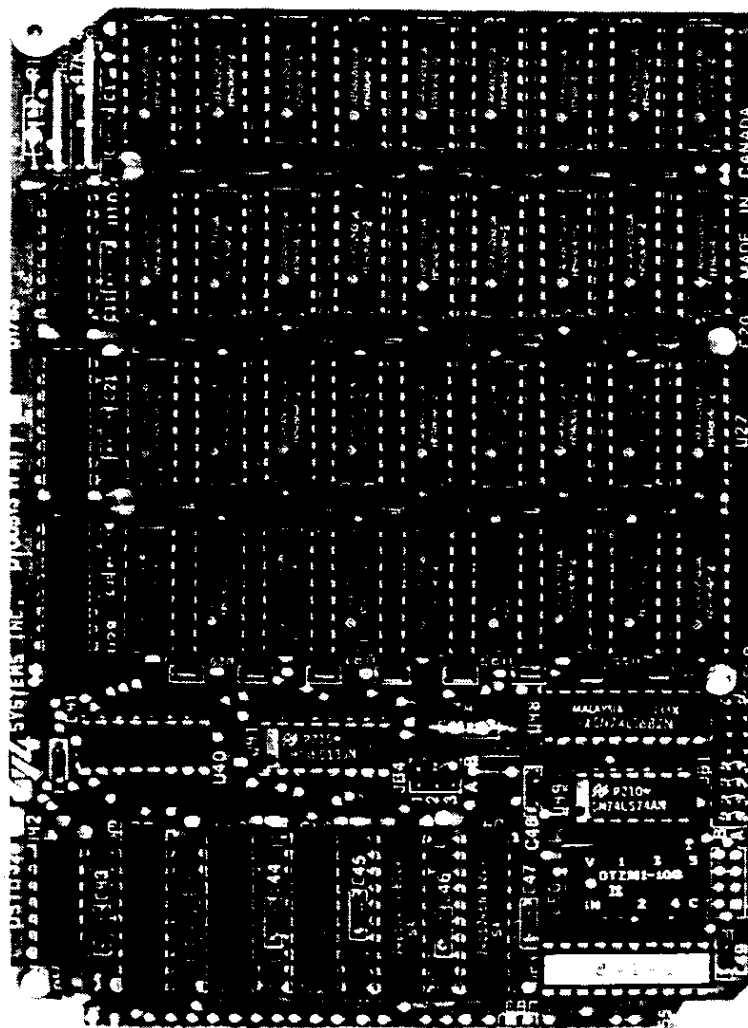


Figure 1 - 1

DSTD-328 256K DYNAMIC MEMORY MODULE WITH PARITY

## SECTION 2

### 2.0 FUNCTIONAL DESCRIPTION

#### 2.1 Introduction

The DSTD-328 is a 256 kilobyte dynamic RAM card designed to be a companion card to the DSTD-188 8088 CPU card. The card can be positioned in any one of the four 256 kilobyte pages in the 1 megabyte address space of the 8088. It features the ability to be enabled and disabled under software control to extend the memory capabilities beyond 1 megabyte using paging techniques. The card generates, stores and checks parity on all 256 kilobytes.

[ The DSTD-188 is an 8088 based CPU card designed to run on both the 8088 STD Bus AND the Z80 STD Bus. In the Z80 mode the card's bus signals and signal timing emulate those of a Z80 CPU card, including refresh cycles. This allows the DSTD-188 to make use of the large number of existing Z80 peripheral cards. ]

#### 2.2 Block Diagram Description

The block diagram for the DSTD-328 is shown in figure 2 - 1. The following paragraphs discuss the functions of the various blocks.

##### 2.2.1 STD BUS Interface

The interface logic includes all the buffers for the address, data and control signals, ensuring that the card represents only one TTL load to the bus.

The interface also includes the logic to "capture" the upper four address bits. The data bus is used to extend the direct address capability of the bus from 64 kilobytes to the 1 megabyte required by the 8088. During the first part of a memory cycle the high order four address bits are placed on the data bus by the processor card. The /ALE signal (pin 38) clocks these bits into a latch for subsequent decoding.

##### 2.2.2 Page Decoding

The card is positioned in one of the four pages using a hardwired jumper block. The page decoding circuitry initiates a memory cycle and enables the data bus transceiver.

### 2.2.3 Card Enabling

The DSTD-328 can be enabled and disabled under software control. This is done using an I/O port. Writing a '1' to bit 6 of the port enables the card and writing a '0' to bit 6 of the port disables the card. The address of the I/O port is set using a jumper block (JB1). When more than one card is used in a system, each card would be assigned to a different I/O port number. Because this card runs with Z80 peripheral cards only the bottom 8 bits of the address bus are decoded during an I/O cycle.

The board powers-up disabled and is disabled by a system reset. This means that more than one card can be assigned to the same page. The software chooses which pages to enable. The RAM is still refreshed when it is disabled.

The parity error register is accessed using the same I/O port. See section 2.2.4

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PAR	C/E	x	x	x	x	x	x

PAR	Parity Error	1	=	error detected
		0	=	no error detected
C/E	Card Enable	1	=	enable the card
		0	=	disable the card
x	not used			

### 2.2.4 Parity Logic

If Parity is used, an additional bit of data is stored in parallel with each byte so that there is always an odd number of high bits (1's) stored. When the data is retrieved, parity is checked automatically. If the number of high bits counted is not odd, a flag is set in the parity error register indicating an error. This flag remains set until it is cleared by writing to the card's I/O port. Thus although parity checking is done on a byte basis, parity error reporting is typically done on a block basis. That is, the parity error flag is checked periodically, for instance, after disk transfers.

Note that a parity error may be generated if a location in RAM is read before it has been written. After power-up the state of the RAM including the parity bit is indeterminate and memory locations must be written at least once before the parity will be correct.



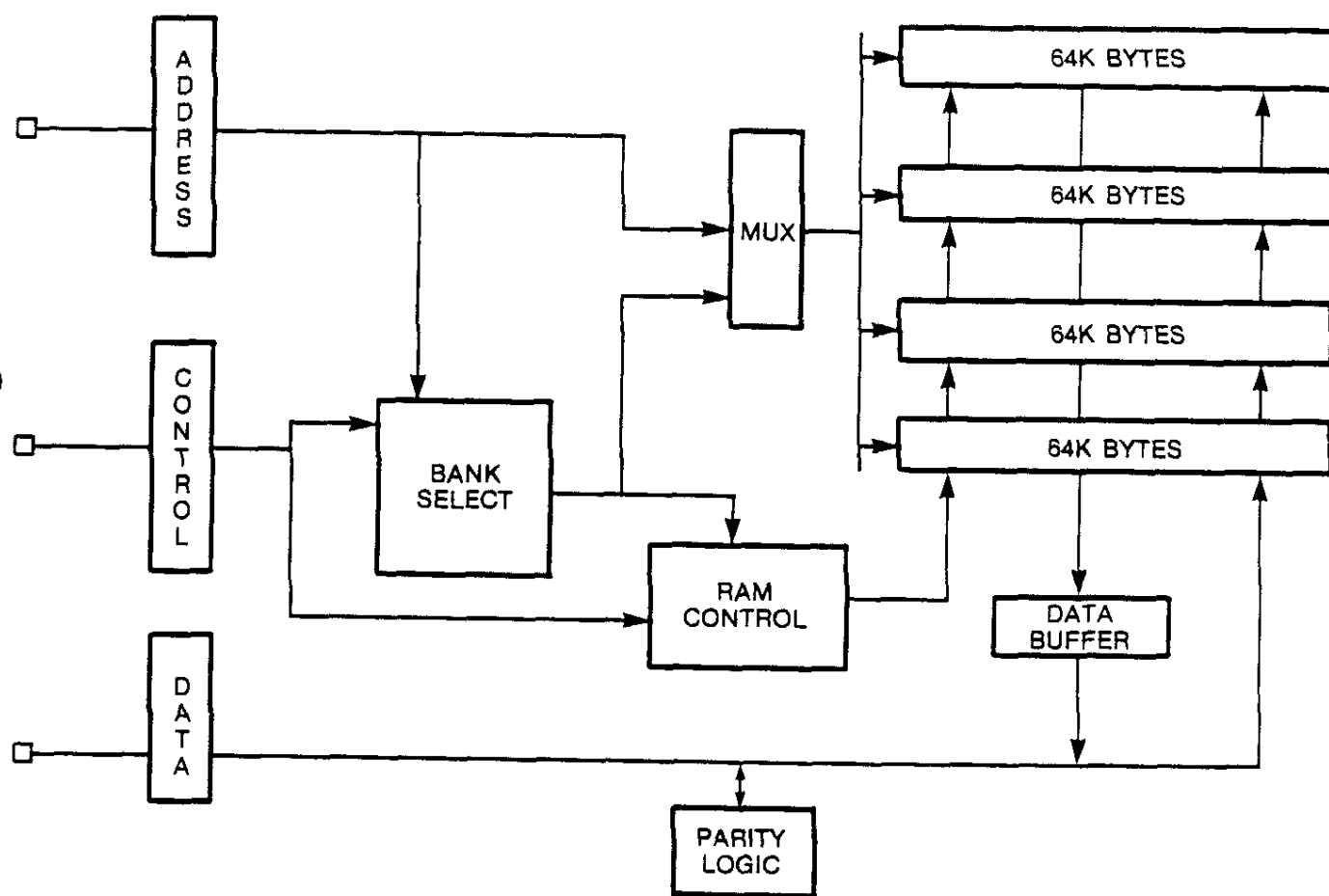


FIGURE 2 - 2 DSTD-328 BLOCK DIAGRAM

## SECTION 3

## 3.0 USER SELECTABLE OPTIONS

## 3.1 Introduction

The following sections discuss the user selectable or user programmable options. The manual concentrates on the hardware selectable options with only a brief discussion of the system and software options.

## 3.2 Card Address Selection (JB1)

The DSTD-328 may be addressed at any one of 256 possible I/O locations. This selection is made using Jumper Block JB1. Shunting adjacent pins creates a low logic level (a '0'), leaving a pair open creates a high logic level (a '1'). These bit values are compared with the lower 8 bits of the address bus. When the two match, the card control registers may be written to and read from. An example is shown in Figure 3-1.

FIGURE 3 - 1

## Card Address Selection JB1

1A	o---o	1B	<-- compares with address bit 7
2A	o o	2B	<-- compares with address bit 6
3A	o o	3B	<-- compares with address bit 5
4A	o o	4B	<-- compares with address bit 4
5A	o---o	5B	<-- compares with address bit 3
6A	o---o	6B	<-- compares with address bit 2
7A	o---o	7B	<-- compares with address bit 1
8A	o---o	8B	<-- compares with address bit 0

OPEN = '1'  
SHORTED = '0'  
FACTORY SETTING = 70H, as shown

## 3.3 RAM Timing (JB2)

Some special applications require modifications to the normal RAM control signal timing relationships. This jumper block is not normally installed. Consult the factory if changes are required.

### 3.4 Page Address Selection (JB4)

The DSTD-328 can be positioned in any of the four 256 kilobyte pages of the 8088's 1 megabyte address space using jumper block JB4. Once the card is positioned it can be turned on and off under software control using an I/O port. Table 3 - 3 shows the jumper block connections.

TABLE 3 - 1

#### PAGE ADDRESS SELECTION

00000H to 3FFFFH	JB4-2B to 3B
40000H to 7FFFFH	JB4-2B to 3A
80000H to BFFFFH	JB4-2B to 2A
C0000H to FFFFFH	JB4-2B to 1A

### 3.5 DMA Priority Chain (JB3)

The STD-Z80 Bus was not originally designed to accommodate more than one DMA device. A problem could exist when two DMA controllers attempted to access the bus at the same time. dy-4 SYSTEMS has developed a technique whereby multiple DMA devices can operate in a prioritized fashion similar to the existing interrupt priority chain provided on the STD Bus.

dy-4 SYSTEMS backplanes incorporate a DMA priority daisy chain using the /BUSAK and /STATUS 0 signal lines (pins 41 and 40 respectively.) Effectively, the DMA device closest to the processor will get control of the bus if two or more are competing for it because it will receive the bus acknowledge signal, preventing those cards further away from the processor from sensing it. If that card did not request the bus, the /BUSAK flows through to be recognized by the next highest DMA device.

Jumper block JB3 of the DSTD-328 allows this signal chain to be carried forward by shunting traces 40 and 41 on the bus. If not used with a dy-4 SYSTEMS backplane, this jumper block should be left open. Figure 3-2 describes this option.

FIGURE 3 - 2

#### DMA Priority Chain

1A o---o 1B

SHORTED = DMA Priority Chain flows through the card  
 OPEN = Multiple DMA devices not supported, non dy-4  
 SYSTEMS backplane  
 FACTORY SETTING = shorted, as shown

## SECTION 4

## 4.0 SPECIFICATIONS

## 4.1 Electrical Specifications

## 4.1.1 Maximum System Clock

DSTD-328x-5.0 5.0MHz + 0.05%

DSTD-328x-8.0 8.0MHz + 0.05%

## 4.1.2 STD BUS Interface

Bus Inputs: One 74LS load max.

Bus Outputs:  $I_{OL} = 24 \text{ mA min. @ } V_{OL} = 0.5 \text{ Volts}$   
 $I_{OH} = 15 \text{ mA min. @ } V_{OH} = 2.4 \text{ Volts}$

## 4.1.3 Operating Temperature

0 Degrees C to 50 Degrees C  
95% humidity non-condensing

## 4.1.4 Power Supply Requirements

DSTD328 5V +/- 5% @ 1.8A

## 4.2 MECHANICAL SPECIFICATIONS

## 4.2.1 Card Dimensions

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm)  
long

0.48 in. (1.22 cm.) maximum height

0.062 in. (0.16 cm.) printed circuit board  
thickness

## 4.2.2 STD Bus Edge Connector

56 pin Dual Readout; 0.125 in. centers  
Mating Connector

Viking 3VH28/1CE5 (printed circuit)  
Viking 3VH28/1CND5 (wire wrap)  
Viking 3VH28/1CN5 (solder lug)

## SECTION 5

## 5.0 FACTORY NOTICES

## 5.1 Factory Repair Service

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. **THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL.** Enclose a letter containing the following information:

Name, address and phone number of purchaser  
Date and place of purchase  
Brief description of the difficulty

Mail a copy of this letter **SEPARATELY** to the closest office:

dy-4 SYSTEMS INC.  
888 Lady Ellen Place  
Ottawa, Ontario  
K1Z 5M1, Canada

-or-

dy-4 SYSTEMS INC.  
3582 Dubarry Rd.  
Indianapolis, IN 46226

Securely package and mail the circuit board, prepaid and insured, to the same address.

## 5.2 Limited Warranty

Dy-4 warrants this product against defective materials and workmanship for a period of one year from date of purchase. This warranty does not apply to any product that has been subjected to misuse, accident, or improper installation, application, or operation, nor does it apply to any product that has been repaired or altered by other than our authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

## NOTICE

The antistatic bag is provided for shipment of dy-4 products to prevent damage to the components due to electrostatic discharge. Failure to use this bag in shipment will **VOID** the warranty.

APPENDIX A  
OPTION JUMPER SUMMARY INCLUDING  
FACTORY SETTINGS

## APPENDIX A

## OPTION JUMPER SUMMARY

## A - 1 Optional Jumper Blocks

The DSTD-328 has the following jumpers.

JB1	Module address selection
JB2	Memory Timing
JB3	DMA chain
JB4	Memory Page Selection

## A - 2 Card Address Selection

This jumper block sets the module's I/O address port.

	1	2	3	4	5	6	7	8
A	o	o	o	o	o	o	o	o
B	o	o	o	o	o	o	o	o
A1 to A8	Ground							
B1	Address Bit 0							
B2	Address Bit 1							
B3	Address Bit 2							
B4	Address Bit 3							
B5	Address Bit 4							
B6	Address Bit 5							
B7	Address Bit 6							
B8	Address Bit 7							

## A - 3 RAM Timing (JB2)

This jumper block is not normally installed and is preset at the factory.

	1	2	3	4		
A	o	o	o	o		
B	o	o	o	o		
A1	no connect				B1	Delay line tap 4
A2	CAS Enable				B2	Delay line tap 2
A3	Delay line tap 1				B3	Address Mux Control
A4	Delay line tap 3				B4	Delay line tap 5



**A - 4                    DMA Chain (JB3)**

This jumper should be installed only when the card is used in a dy-4 SYSTEMS backplane.

o	BUSAK	(pin 40)
o	BA0	(pin 41)

**A - 5                    Memory Page Selection (JB4)**

To select a page install one of four jumpers.

	A	B	
Page 3 decoded	1	o   o	no connect
Page 2 decoded	2	o   o	RAM control circuitry
Page 1 decoded	3	o   o	Page 0 decoded

APPENDIX B  
STD-Z80 BUS PIN OUT AND  
DESCRIPTION

## APPENDIX B

### STD-Z80/STD-8088 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices. A16-A19 are multiplexed in D0-D3 during ALE.
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	
15	A7	Address Bus (output, active high).  A0-A15 make up a 16-bit address bus. The address bus along with the multiplexed Address on the data bus provides for 1 Megabyte of memory. I/O addressing uses these same 16 address bits to allow the user to directly select up to 65K input or 65K output ports. A0 is the least significant address bit. During refresh time, the lower 8 bits contain a valid refresh address for dynamic memories in the system.
16	A15	
17	A6	
18	A14	
19	A5	
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Memory Write (output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

# STD-Z80/STD-8088 BUS PIN OUT

32	/RD	Memory Read (output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (output, active low). In Z80 mode the /IORQ signal indicates that the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time. In 8088 mode this pin contains the 8088 status signal '/S2'.
34	/MEMRQ	Memory Request (output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 SYSTEMS DSTD.
36	/MEMEX	Memory expansion, not used on dy-4 SYSTEMS DSTD cards.
37	/REFRESH	/REFRESH (output, active low). /REFRESH indicates that the lower 8 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A8-A15 are not defined.
38	/MCSYNC	MEMORY CYCLE SYNC (OUTPUT, active low) This pin contains /ADDRESS LATCH ENABLE (ALE) from the 8088 processor. It signals to the bus that D0-D3 contains A16-A19.
39	/STATUS 1	In Z80 mode: Machine Cycle One (output, active low). /M1 occurs with /IORQ to indicate an interrupt acknowledge cycle.

# STD-Z80/STD-8088 BUS PIN OUT

In 8088 mode:

Status 1 (output, active low). This pin contains the 8088 status signal '/S1'.

40        /STATUS 0

Status 0 (output, active low). This pin contains the 8088 status signal '/S0'.

41        /BUSAK

Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

42        /BUSRQ

Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.

43        /INTAK

Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.

44        /INTRQ

Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop is enabled and if the /BUSRQ signal is not active. In Z80 mode, when the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.

45        /WAITRQ

WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to

## STD-Z8C/STD-8088 BUS PIN OUT

enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

- |    |           |  |
|----|-----------|--|
| 46 | /NMIRQ    | Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 00008H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will override a /NMIRQ. |
| 47 | /SYSRESET | System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to OFFF0H.  |
| 48 | /PBRESET  | Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset.   |
| 49 | /CLOCK    | Bus Clock (Output, active low). Single phase system clock. This clock runs at one half processor clock rate.   |
| 50 | CNTRL     | Auxiliary Timing   |
| 51 | PCO       | Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.   |

# STD-Z80/STD-8088 BUS PIN OUT

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

## NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.

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APPENDIX C  
DSTD-328 PARTS LIST



## APPENDIX C

## DSTD-328 PARTS LIST

QTY	DESIGNATION	PART NUMBER
INTEGRATED CIRCUITS		
1	U49	74LS74
1	U37	74S138
1	U40	74LS174
1	U41	74LS139
3	U43,46,47	74LS245
1	U42	74S280
2	U44,45	74LS373
1	U48	74LS682
2	U38,39	DS3648
36	U1 - 36	4164-150/200
1	U50	DTZM - 100/250
1	U51	PAL16L8
DISCRETE COMPONENTS		
1	RN1	4306-101-472
1	RN2	4308-102-470
1	R3	4.7K 1/4 watt
2	R1,2	47 1/4 watt
5	C2,20,22,40,42	10uF Tant.Cap
44	C1,3-19,21,23-39,41	
	C43-49	0.1uF ceramic
3	JB1,2,4	CHD6900W1S
36	16 Pin sockets	640358-3 AMP
1	20 Pin socket	640464-1 AMP

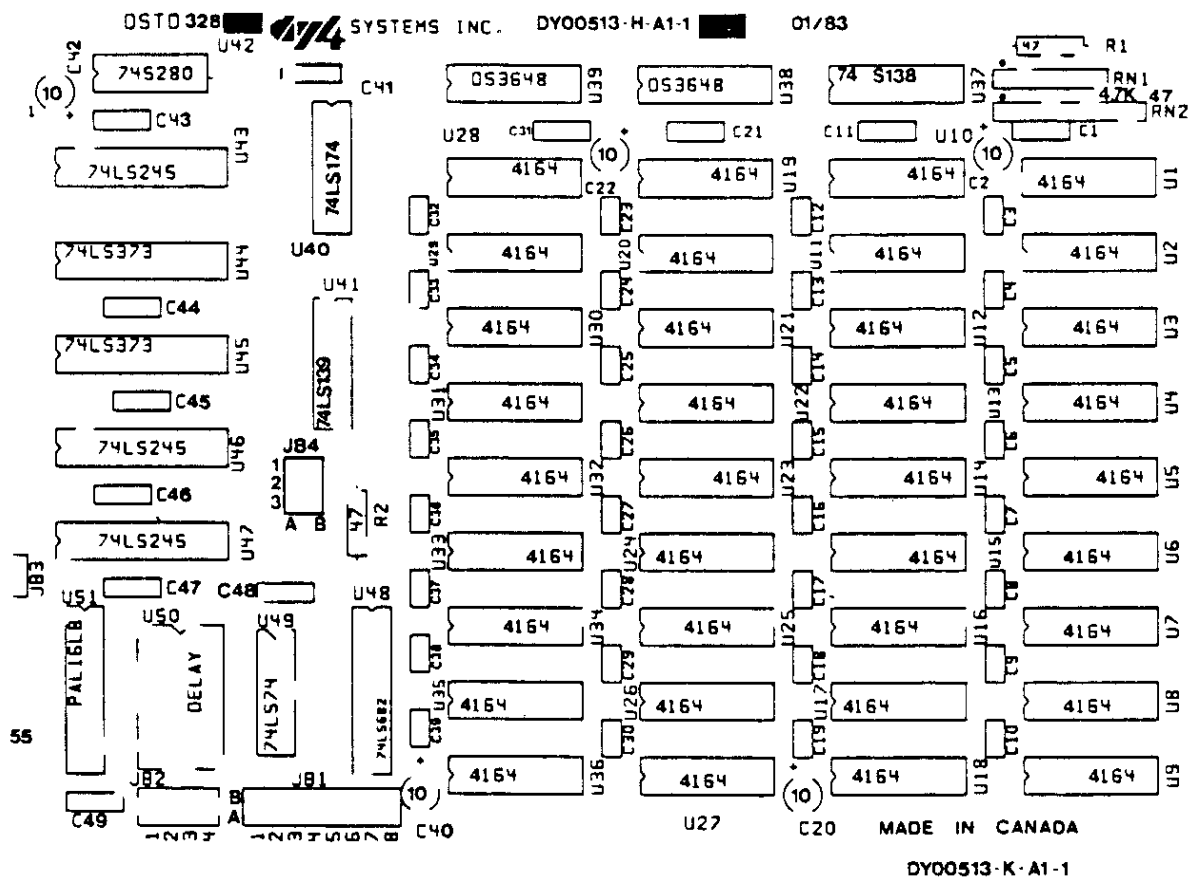
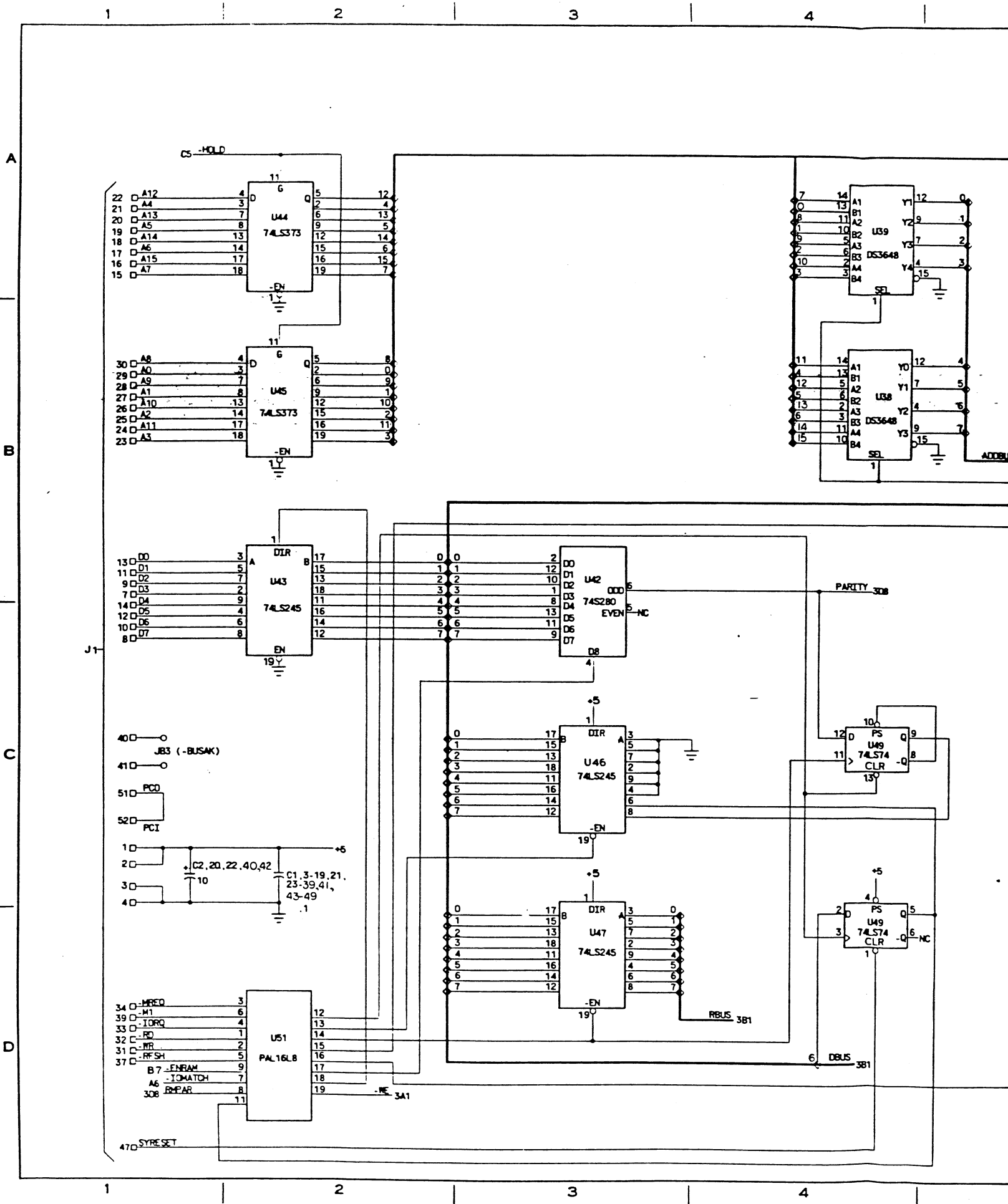


FIGURE C-1 DSTD-328 SILK SCREEN

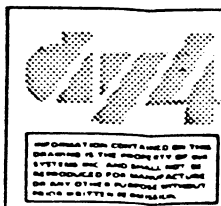
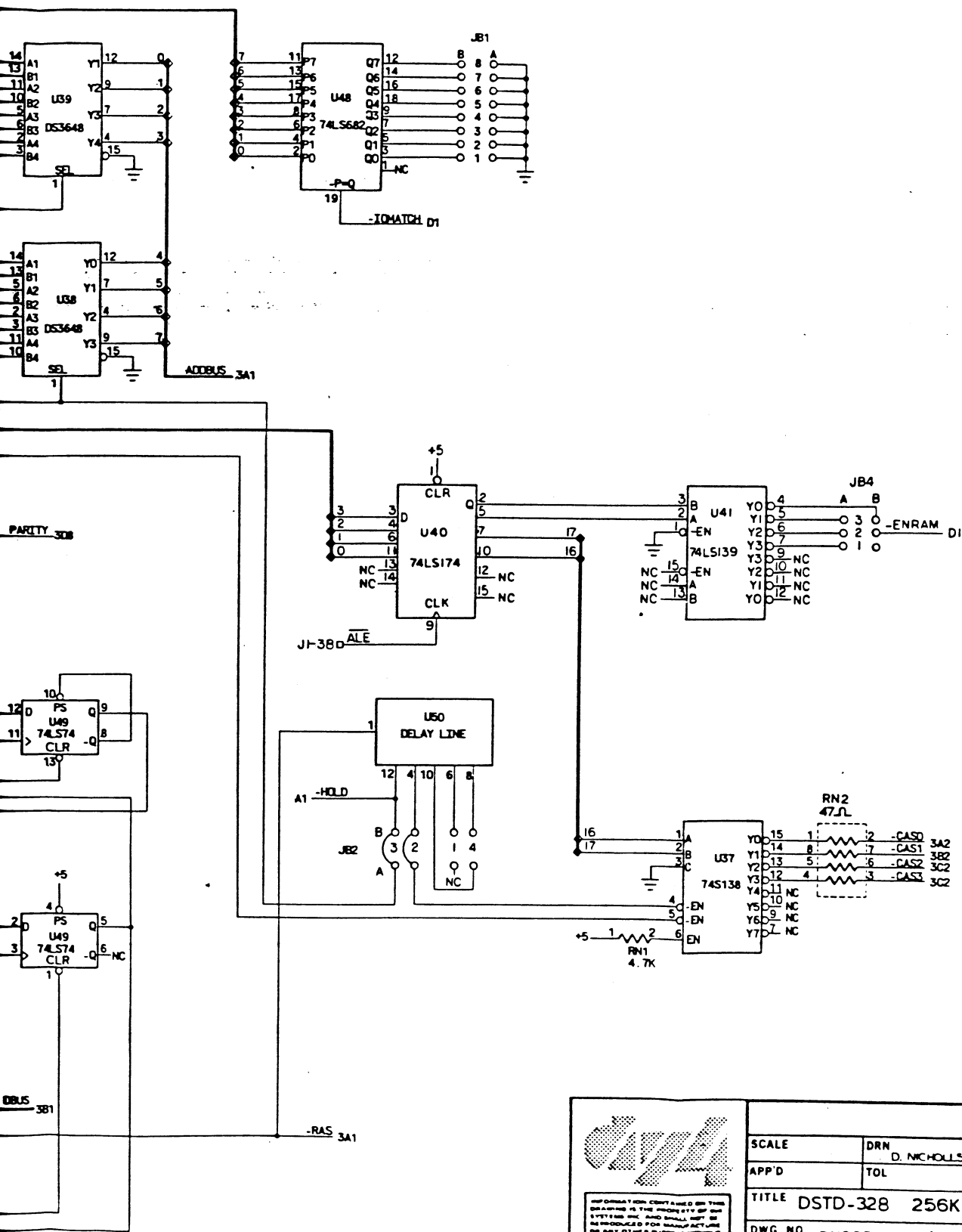
APPENDIX D  
DSTD-328 SCHEMATIC

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35				
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30				
29	36		SOCKET, IC., 16 PIN D.I.P.	AT U1-36
28	1		SOCKET, IC., 20 PIN D.I.P.	AT U51
27				
26	1		RES., NETWORK, 47K $\Omega$ , 6PIN SLP, (EPITEK 605)	RN1
25	1		RES., NETWORK, 47 $\Omega$ , 8PIN SLP,	RN2
24	2		RESISTOR, FIXED COMP., 1/4W, 5% 47 $\Omega$	RI, 2
23				
22	1		HEADER, STRAIGHT (2x8)	JB1
21	1		↑ (2x4)	JB2
20	1		↓ (2x3)	JB4
19	1		HEADER, STRAIGHT (1x2)	JB3
18				
17	5		CAPACITOR, TANTALUM, 10 $\mu$ F	C2, 20, 22, 40, 42
16	44		CAPACITOR, CERAMIC, .1 $\mu$ F 50V	C13-19, 21, 23-39, 41, 43-49
15				
14	1		INTEGRATED CIRCUIT, DELAY LINE	U50
13	1		↑ PAL16L8	U51
12	2		DS3648	U38, 39
11	36		4164	U1-36
10	1		74LS682	U48
9	2		74LS373	U44, 45
8	1		74S280	U42
7	3		74LS245	U43, 46, 47
6	1		74LS174	U40
5	1		74LS139	U41
4	1		↓ 74S138	U37
3	1		INTEGRATED CIRCUIT 74LS74	U49
2				
1	1		PRINTED CIRCUIT BOARD	
ITEM	QTY	PART NUMBER	DESCRIPTION	DESIGNATION

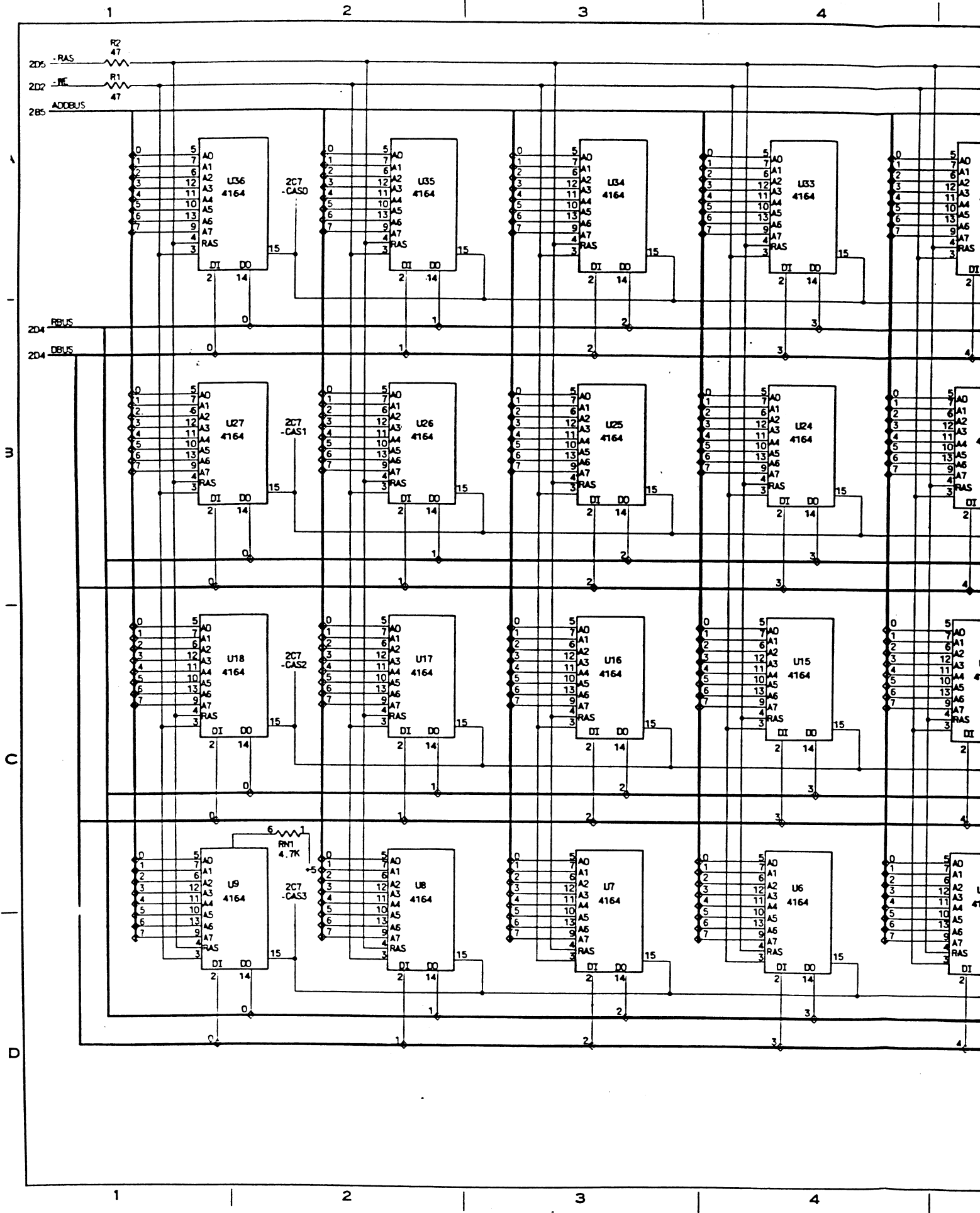




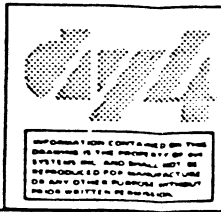
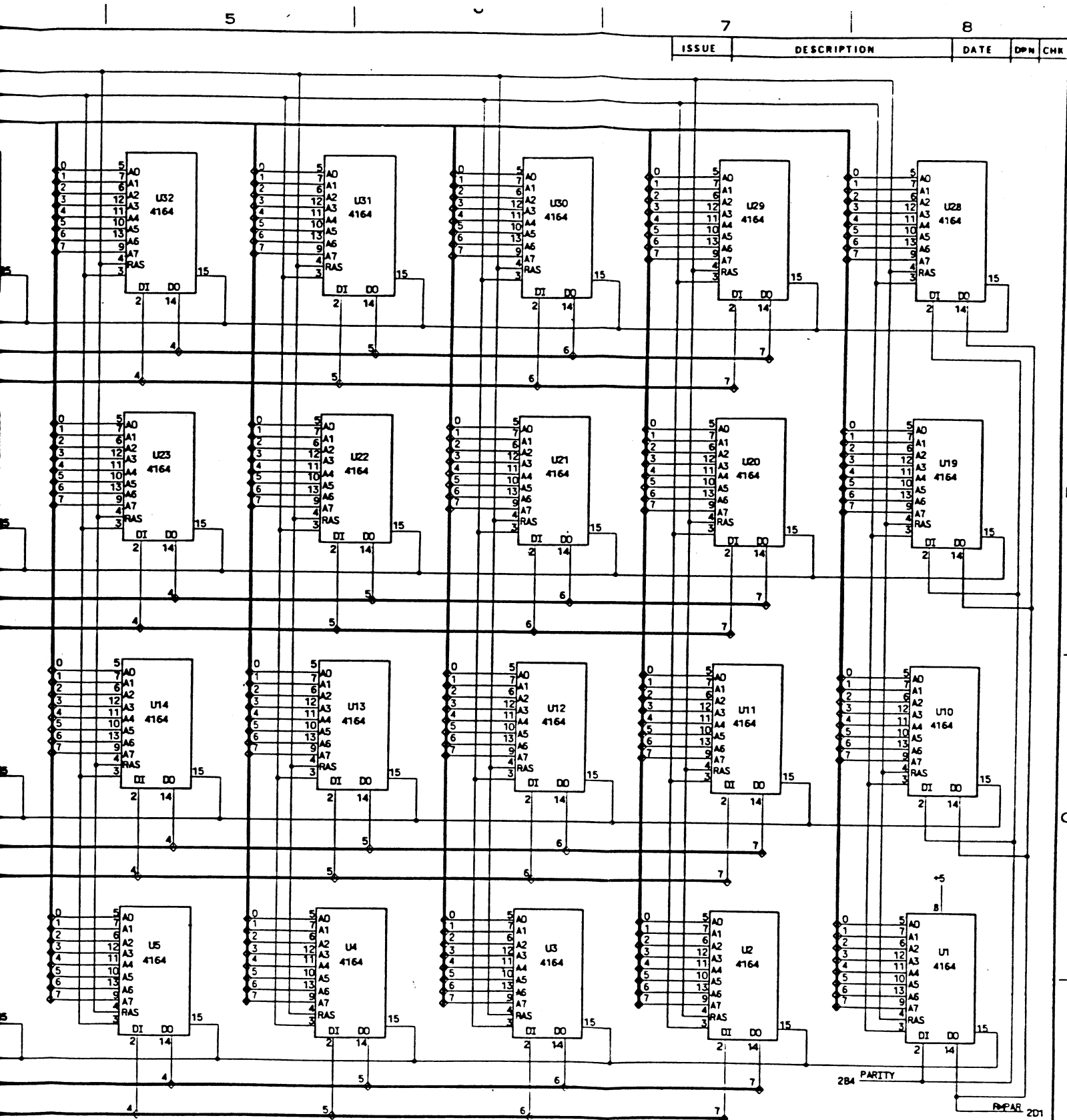
ISSUE	DESCRIPTION	DATE	DRN	CHK
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SCALE	DRN	CHK	DATE
APP'D	TOL	MAT'L	FINISH
TITLE DSTD-328 256K RAM CARD			
DWG NO DY00513-I-A2-1		ISS 1	SH 2 OF 3







SCALE	DRN D. NICHOLLS	CHK	DATE APRIL 13 1983
APP'D	TOL	MAT'L	FINISH
TITLE DSTD-328 256K RAM CARD			
DWG NO DY00513 -I-A3-1		ISS 1	SH 3 OF 3