

DOCUMENT NO. DSTD-401-M  
REVISION C

DSTD-401  
RS-422 SERIAL INTERFACE  
with DMA  
OPERATIONS MANUAL  
DY00460

covering part numbers:  
DSTD-401-2.5  
DSTD-401-4.0  
DSTD-401A-2.5  
DSTD-401A-4.0

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# REVISION NOTICE

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A	Original Release	
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#### Acknowledgements

Z80 is a Trademark of Zilog, Inc.

## SECTION 1

### 1.0 GENERAL INFORMATION

#### 1.1 DSTD Series General Description

The DY-4 DSTD Series of Z80/STD-BUS compatible products was designed to satisfy the need for high performance microcomputer modules that could be quickly and inexpensively integrated into a variety of end-user applications. The popular STD-BUS motherboard interconnect system concept provides expandability as needs change. Support by numerous manufacturers provides the user with a choice from scores of compatible products.

The modules for the Z80/STD-BUS are a compact 4.5 x 6.5 inches (11.45 x 16.50 cm) which provides for system partitioning by function, i.e. CPU, Memory, I/O, etc. DY-4 SYSTEMS has been able to combine most popular functions on single cards to reduce system card count and cost.

#### 1.2 DSTD-401 Features

The DSTD-401 is a dual channel general purpose RS-422 Serial Interface Module (using the powerful Z80-SIO controller) for applications requiring high speed, long distance serial communications. The SIO provides both asynchronous and synchronous message packaging protocols including SDLC, HDLC and IBM Bisync, and can automatically calculate and check message CRC's for increased reliability.

The DSTD-401 incorporates one Z80 DMA for each channel in order to achieve data throughput up to 800 Kbits/second. It supports the powerful Mode 2 Z80 vectored interrupt technique with built in daisy-chain priority. In most synchronous applications, half duplex operation is recommended due to the way the RS-422 receiver/drivers are used.

The RS-422 receiver/driver circuitry uses a differential signal detection technique which results in common mode induced voltage noise rejection up to 7 volts. Input protection circuitry is provided to minimize damage from line transients. The RS-422 drivers, which can drive up to 4000ft of twisted pair cable, are not in themselves short circuit protected. It is possible to install series resistors to provide some protection when appropriate.

Provision has been made to install shunt resistors across the inputs of the RS-422 receivers to minimize transmission line effects.

It is possible to cross-connect the transmit and receive lines. This is typically used in synchronous half duplex systems and because the transmitters can be disabled under software control, allows bidirectional data transfers over the same twisted pair.

### **1.3 DSTD-401 Description By Part Number**

Two Versions of the DSTD-401 are available, each capable of either 2.5 or 4.0 Mhz operation. Part numbers incorporating a trailing 'A' are single channel devices with only one DMA and components stuffed for operation of only the 'A' channel of the SIO. The '-2.5' and '-4.0' suffixes indicate modules intended for use in 2.5 and 4.0 Mhz systems respectively.



FIGURE 1 - 1 DSTD-401 MODULE

## SECTION 2

## 2.0 FUNCTIONAL DESCRIPTION

## 2.1 Application

The DSTD-401 may be used where high speed, noise immune serial communication is required over long distances. Typical applications include remote data acquisition devices, remote terminals, and as a networking communications controller. The block diagram shown in Figure 2-1 illustrates the major components of the module.

## 2.2 SIO Capabilities

The Z80 SIO is responsible for converting eight bit parallel data provided by the host CPU on the data bus into packaged serial data conforming to a variety of established protocols. For a complete description and programming details of features available with the SIO, please refer to the Zilog/Mostek Technical Manual.

Asynchronous protocols may be configured for 5, 6, 7 or 8 data bits per character; 1, 1-1/2, and 2 start/stop bits; even and odd parity generation and checking; and overrun/framing error detection.

Synchronous protocols available include bit and byte oriented messages conforming to establish standards such as SDLC, HDLC and IBM Bisync, or user defined protocols.

Each channel has a very flexible baud rate generator consisting of a programmable four bit counter and a nine bit binary divider driven from a 19.6608Mhz base clock. Table 2-1 shows the possible clock rates when the SIO is used in 'x1' mode. Table 2-2 shows the clock rates possible when using the SIO in 'x16' mode, the most common asynchronous mode.

The SIO may be programmed to interrupt on any of several possible conditions, utilizing the powerful Mode 2 interrupt response mechanism of the Z80 to vector program control to the appropriate user defined routine.



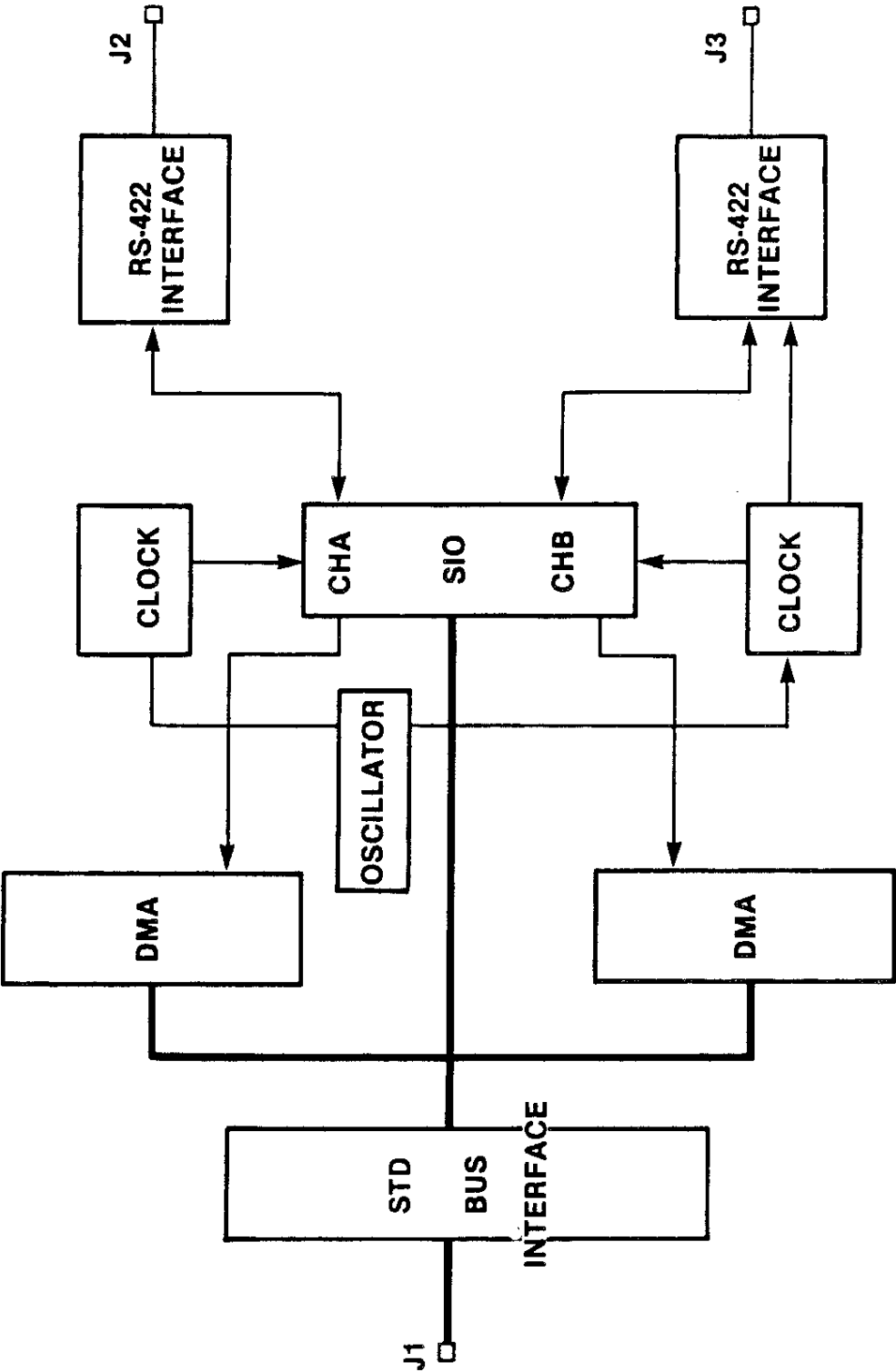


FIGURE 2 - 1 DSTD-401 BLOCK DIAGRAM

TABLE 2-1

## Synchronous Baud Rates

DIVIDER	2	4	8	16	32	64	128	256	512
1	*	*	*	*	(614400)	307200	153600	76800	38400
2	*	*	*	(614400)	307200	153600	76800	38400	19200
3	*	*		409600	204800	102400	51200	25600	12800
4	*	*	(614400)	307200	153600	76800	38400	19200	9600
5	*	*	491520	245760	122880	61440	30720	15360	7680
6	*		409600	204800	102400	51200	25600	12800	6400
7	*	(702171)	351086	175543	87771	43886	21943	10971	5486
8	*	(614400)	307200	153600	76800	38400	19200	9600	4800
9	*	(546133)	273067	136533	68267	34133	17067	8533	4267
10	*	491520	245760	122880	61440	30720	15360	7630	3815
11	*	446836	223418	111709	55855	27927	13964	6982	3491
12	*	409600	204800	102400	51200	25600	12800	6400	3200
13	(756185)	378092	189046	94523	47262	23631	11815	5908	2954
14	(702171)	351086	175543	87771	43886	21943	10971	5486	2743
15	(655360)	327680	163840	81920	40960	20480	10240	5120	1280
16	(614400)	307200	153600	76800	38400	19200	9600	4800	2400

NOTE: An '\*' indicates an illegal combination. The maximum input clock rate is one-fifth of the CPU clock. The entries enclosed in parentheses are legal for 4.0MHZ version boards.

TABLE 2-2

## Asynchronous Baud Rates

DIVIDER	2	4	8	16	32	64	128	256	512
1	*	*	76800	38400	19200	9600	4800	2400	1200
2	*	76800	34800	19200	9600	4800	2400	1200	600
3	102400	51200	25600	12800	6400	3200	1600	800	400
4	76800	34800	19200	9600	4800	2400	1200	600	300
5	61440	30720	15360	7680	3840	1920	960	480	240
6	51200	25600	12800	6400	3200	1600	800	400	200
7	43886	21943	10971	5486	2743	1371	686	343	171
8	38400	19200	9600	4800	2400	1200	600	300	150
9	34133	17067	8533	4267	2133	1067	533	267	133
10	30720	15360	7680	3840	1920	960	480	240	120
11	27927	13964	6982	3491	1745	873	436	218	109
12	25600	12800	6400	3200	1600	800	400	200	100
13	23631	11815	5908	2954	1477	738	369	185	92
14	21943	10971	5486	2743	1371	686	343	171	86
15	20480	10240	5120	2560	1280	640	320	160	80
16	19200	9600	480	2400	1200	600	300	150	75

NOTE: An '\*' indicates an illegal combination.

### 2.3 RS-422 Interface

The RS-422 interface provides differential voltage level type line drivers which can be used over long distances (up to 4000'). The circuitry provided allows user configuration of line shunting to minimize reflections. Refer to the RS-422 Electrical Specifications for the relationship between distance and maximum transmission rates.

### 2.4 DMA Operation

The two DMA Controllers designed into the DSTD-401 provide the ability to transfer data between the SIO and memory at maximum speed

As with most DSTD Series products, the DSTD-401 can be configured for standard backplanes for single DMA device systems or for the DY-4 SYSTEMS backplane for multiple DMA device systems.

## SECTION 3

## 3.0 User Selectable Options

## 3.1 Introduction

The following sections discuss the user selectable or user programmable options. The manual concentrates on the hardware selectable options with only a brief discussion of the system and software options. The user is referred to the operation manuals for the serial controller and the direct memory access chips published by the chip manufacturers (Zilog/Mostek)

## 3.2 Address Selections

The DSTD-401 occupies eight ports in the processor's I/O address space. The ports may be located anywhere in the address space on an eight port boundary. Only six of the eight ports are actually used. Table 3-1 show the ports assignments.

TABLE 3-1

INPUT/OUTPUT PORT ADDRESS ASSIGNMENTS

Port Address	Function
00	SIO Channel A Data
01	SIO Channel A Control
02	SIO Channel B Data
03	SIO Channel B Control
04	DMA Channel A
05	DMA Channel B
06	not used
07	not used

NOTE: Accessing port 6 will select DMA channel A and accessing port 7 will select DMA channel B. As a general practice this should be avoided.

Figure 3-1 illustrates how the base address is set up.

Figure 3-1

## BASE ADDRESS SELECTION (JB15)

	A	B	
1	o	o	Bit 7
2	o	o	Bit 6
3	o---	o	Bit 5
4	o---	o	Bit 4
5	o---	o	Bit 3

A short between adjacent pins, (e.g. 1A-1B), produces a binary '0'. Leaving an open produces a '1'. For the strapping shown, the binary value would equal 0COH (the remaining three bits are decoded internally on the DSTD-401.) The Factory Setting is as shown: 0COH.

### 3.3 RS-422 Cable Interface Blocks (JB1,2,3,4,5,6)

Each channel has five differential signal pairs.

1)	Transmit Data	pins 1(+) and 2(-)
2)	Transmit Clock	pins 7(+) and 8(-)
3)	Receive Data	pins 4(+) and 5(-)
4)	Receive Clock	pins 10(+) and 11(-)
5)	Clear to Send	pins 13(+) and 14(-)

Provision is made to allow for the termination of the receiver lines i.e. Receive Data, Receive Clock and Clear to Send. By installing the appropriate jumper a 100 ohm shunt resistor can be connected across the differential lines (refer to the schematic Appendix D).

Provision is also made to cross-connect the transmit drivers and the receivers for both the data lines and the clock lines. This is used in systems requiring bidirectional data paths (e.g. multi-drop network systems). Table 3-2 shows which jumper blocks serve which lines

TABLE 3-2

## CABLE INTERFACE BLOCKS

JB1	Channel A Transmit and Receive Data
JB2	Channel A Transmit and Receive Clock
JB3	Channel A Clear to Send
JB4	Channel B Transmit and Receive Data
JB5	Channel B Transmit and Receive Clock
JB6	Channel B Clear to Send

Jumper blocks JB1,2,4 and 5 consist of two rows of three pins and are arranged as show in figures 3-2 and 3-3. JB3 and 6 are each simply two pins as shown in figure 3-4.

Figure 3-2

## RS-422 CABLE DATA INTERFACE JUMPER BLOCK (JB1,JB4)

	A	B	
Rx(-)	1	o---o	through 100 ohm resistor to Rx+
Rx(-)	2	o---o	to Tx-
Rx(+)	3	o---o	to Tx+

Where: Rx +/- are the receive data differential input signals  
Tx +/- are the transmit data differential output signals

Factory Setting: as shown, fully shunted

Figure 3-3

## RS-422 CABLE CLOCK INTERFACE JUMPER BLOCKS (JB2,JB5)

	A	B	
Rclk(-)	1	o---o 1	through 100 ohm resistor to Rclk+
Rclk(-)	2	o---o 2	to Tclk(-)
Rclk(+)	3	o---o 3	to Tclk(+)

Where: Rclk +/- are the externally supplied differential input clock signals  
Tclk +/- are the differential output Tclk signals

Factory Setting: as shown, fully shunted

Figure 3-4

## CLEAR TO SEND SIGNAL CONDITIONING (JB3,JB6)

	A	B	
CTS(-)	o	o	through 100 ohm resistor to CTS(+)

Where: CTS +/- are the externally supplied differential input CTS signals

Factory Setting: as shown, open

### 3.4 Baud Rate Selection (JB 7, 8, 9, 12)

If the DSTD-401 module is to supply the clock for the system, then the Baud Rate Options at Jumper Blocks JB 7, 8, 9 and 12 must be configured for the appropriate Baud Rate. The baud rate generator has two sections - a programmable 4 bit counter driven by a 19.6608 Mhz clock oscillator, followed by a nine bit binary divider chain. Use Tables 2-1, 2-2 and 3-3 to select the desired rates. Figures 3-5 and 3-6 illustrate jumper blocks JB 7/8 and 9/12 for Channels A and B respectively.

TABLE 3 - 3

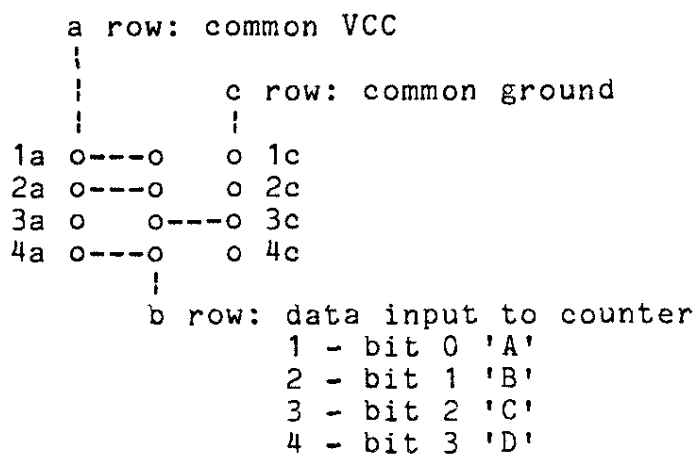
## PROGRAMMABLE DIVIDER SETTINGS

DIVIDER	D	C	B	A
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0

Figure 3-5 shows the jumper blocks for the programmable divider.

Figure 3-5

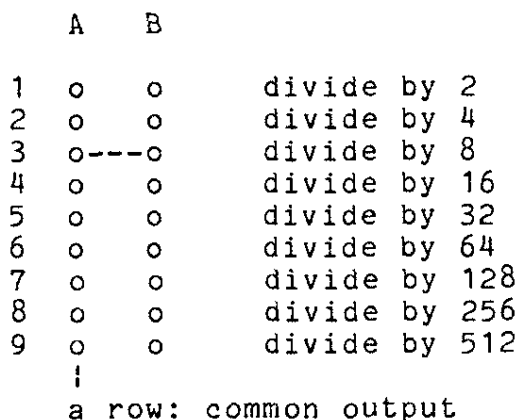
## PROGRAMMABLE DIVIDER - BAUD RATE GENERATOR (JB7,JB12)



Where: Connections between the A row and B row produce a high '1' logic level.  
Connections between the C row and B row produce a low '0' logic level.

Figure 3-6

BINARY DIVIDER - BAUD RATE GENERATOR (JB9,JB12)



Where: Only one pair of pins may be shorted.

Factory setting: 3a - 3b, divide by 8, as shown

## BAUD RATE PROGRAMMING EXAMPLE

Using the figures above and the Tables 2-1 and 2-2, the following baud rates may be configured for synchronous and asynchronous operation when the DSTD-401 is supplying the baud rate timing.



Example 1: Asynchronous - 9600 baud

JB7 (or JB8): 1A - 1B, 2A - 2B, 3A - 3B, 4A - 4B

JB9 (or JB12): 6A - 6B

Example 2: Synchronous - 38.4K baud

JB7 (or JB8): 1B - 1C, 2B - 2C, 3A - 3B, 4A - 4B

JB9 (or JB12): 2A - 2B

Example 3: Synchronous - 756K baud

JB7 (or JB8): 1A - 1B, 2A - 2B, 3B - 3C, 4B - 4C

JB9 (or JB12): 1A - 1B

### 3.5 Clock Source Selection (JB10, 11)

The DSTD-401 may be configured to generate the clock for use by other modules or may receive a clock input as one of the signals exchanged received. Figure 3-7 describes how this selection is made at Jumper Block JB 10 and 11 for Channels A and B respectively.

Figure 3-7

#### CLOCK SOURCE SELECTION

JB 10 and 11

		A	B	
SIO Tclk	1	o---o		to RS-422 Tclk driver
SIO Tclk	2	o	o	from RS-422 Rclk receiver
Baud Rate	3	o	o	Baud rate generator
Generator				
from RS-422	4	o---o		SIO Rclk
Rclk receiver				

Where: SIO Tclk/Rclk refer to the SIO input connections for separate clock frequencies for transmit and receive baud rates

Baud Rate Generator refers the output of the counter/divider chains.

Factory Setting: As shown, the module is supplying the transmit clock as determined by the baud rate generator. The receive clock is taken from the network i.e. the RS-422 receivers.

### 3.6 DMA BUS-Request Buffering (JB13)

The /BUSRQ signal is generated by the DMA controllers. This signal may be buffered onto the backplane by installing JB13-1A to JB13-2A. Note, however there are circumstances when this signal cannot be buffered. This signal is also an input to the DMA chips. A DMA chip will not generate a BUSRQ (Bus request) if DMA cycle is already in progress under the a control of another DMA device. This is so that it will not upset the DMA priority chain. Therefore in a multiple DMA device system this signal cannot be buffered onto the backplane - install JB13-1B to JB13-2B instead.

Figure 3-8

#### BUS REQUEST ARBITRATION

	1	2	
to /BUSRQ at STD BUS	A	o o	from BUSRQ buffer
to /BUSRQ at STD BUS	B	o---o	from DMA Chips BUSRQ

Factory Setting: 1b - 2b as shown

### 3.7 DMA BUS-Acknowledge Priority Chain (JB14)

The DY-4 SYSTEMS implementation of the STD BUS allows for multiple interrupting devices to be used by virtue of DMA Bus-Acknowledge signal arbitration. This creates a DMA device priority scheme similar to the way PCI/PCO is used to prioritize interrupt requests. To do this the DY-4 SYSTEMS backplane implementation uses pins 40 and 41 to create a DMA priority chain. Pin 41 is the output and pin 40 is the DMA priority chain input. However to be compatible with STD bus backplanes from other manufactures the DSTD-401 can be configured to accept the BUSAK input signal from pin 41.

Jumper Block JB14 is used to select whether the module will be used in a DY-4 backplane or an alternate manufacturer. This feature is described in Figure 3-9.

Figure 3-9

#### DMA-/BUSAK PRIORITY CHAIN (JB14)

	A	B	
Pin 41-BAO	1	o---o	Pin 40-BAI
/BAO signal	2	o---o	BUSAK

Where: 1a - 2a allows module to pass through DMA priority chain  
 1b - 2b allows module to arbitrate DMA priority chain  
 Factory Setting: Both jumpers installed, as shown

## SECTION 4

## 4.0 SPECIFICATIONS

## 4.1 Functional Specifications

## 4.1.1 Word Size

Data	8 bits
I/O Addressing	8 bits

## 4.1.2 Cycle Time

	MIN.	MAX.
DSTD-401-2.5	250 KHz	2.5 MHz
DSTD-401-4.0	250 KHz	4.0 MHz

## 4.1.3 I/O Addressing

On-board user-programmable, refer to paragraph 3.2 for programming details.

## 4.1.4 Serial Communication Ports

Each serial channel has its own baud rate generator which may be user programmed for the desired baud rate via hardware jumpers. For programming details refer to paragraph 3.4.

## 4.1.5 Interrupts

The DSTD-401 supports vectored interrupt generation via both the SIO and DMA controller chips. Each device is interrupt vector programmable upon initialization. Also, the DSTD-401 supports full daisy-chain interrupt priority.

## 4.1.5.1 System Interrupt Units

SIU - 3

## 4.2 Electrical Specifications

### 4.2.1 STD Bus Interface

Bus Inputs            One 74LS Load max.  
Bus Outputs         $I_{OL}$  - 24 mA min. @  $V_{OL}$  = 0.5VDC  
                      $I_{OH}$  - 15 mA min. @  $V_{OH}$  = 2.4VDC

### 4.2.2 Power Supply Requirements

+5VDC  $\pm$  5% @ 1.1 Amps Max

## 4.3 Mechanical Specifications

### 4.3.1 Card Dimensions

4.5 Inches (11.43 cm.) wide by 6.50 Inches (16.51 cm.) long

0.48 Inches (1.22 cm.) maximum height

0.062 Inches (0.16 cm.) printed circuit board thickness

### 4.3.2 STD BUS EDGE Connector

56 Pin dual readout; 0.125 inch centers

#### 4.3.2.1 Mating Bus Connector

VIKING 3VH28/1CE5 (PCB)  
VIKING 3VH28/1CND5 (Wirewrap)  
VIKING 3VH28/1CN5 (Solder Lug)

### 4.3.3 Serial Channel Connectors

2 - 26 Pin Dual 0.100 inch grid 1-87230-3 AMP

Mating Connector AMP 88378-3 or equivalent

### 4.3.4 Operating temperature

0 to 60 degrees celsius.

## SECTION 5

### 5.0 FACTORY NOTICES

#### 5.1 FACTORY REPAIR SERVICE

In the event that difficulty is encountered with this unit, it may be returned directly to DY-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. **THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL.** Enclose a letter containing the following information with the returned circuit board:

Name, address and phone number of purchaser  
Date and place of purchase  
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

SERVICE DEPARTMENT  
DY-4 SYSTEMS INC.  
888 Lady Ellen Place, -or-  
Ottawa, Ontario  
K1Z 5M1, Canada

SERVICE DEPARTMENT  
DY-4 SYSTEMS INC.  
3582 Dubarry Rd.  
Indianapolis, IN 46226

Securely package and mail the circuit board, prepaid and insured, to the same address.

#### 5.2 LIMITED WARRANTY

DY-4 warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

### NOTICE

The antistatic bag is provided for shipment of the DY-4 PC boards to prevent damage to the components due to electrostatic discharge.

Failure to use this bag in shipment will VOID the warranty.

**APPENDIX A**  
**JUMPER OPTION SUMMARY**

## APPENDIX A

## JUMPER OPTION SUMMARY

A - 1 The following is a list of the DSTD-401 jumper option blocks.

JB1	Channel A Transmit and Receive Data
JB2	Channel A Transmit and Receive Clock
JB3	Channel A Clear to Send
JB4	Channel B Transmit and Receive Data
JB5	Channel B Transmit and Receive Clock
JB6	Channel B Clear to Send
JB7	Channel A Programmable Divider
JB8	Channel B Programmable Divider
JB9	Channel A Binary Divider
JB10	Channel A Clock Source Selection
JB11	Channel B Clock Source Selection
JB12	Channel B Binary Divider
JB13	DMA BUSRQ
JB14	DMA Priority Chain
JB15	Module I/O Address Selection

A - 2 Transmit and Receive Data/Clock Blocks (JB1,2,4,5)

	1	2	3
B	o	o	o
A	o	o	o

1A,2A	RX/RCLK (-)
3A	RX/RCLK (+)
1B	Thru 100 ohms to RX/RCLK (+)
2B	TX/TCLK (-)
3B	TX/TCLK (+)

A - 3 Clear to Send Blocks (JB3,6)

	A	B
CTS (-)	1	o--o thru 100 ohms to CTS (+)

## A - 4 Programmable Divider (JB7,8)

	1	2	3	4
C	o	o	o	o
B	o	o	o	o
A	o	o	o	o

Set to divide by 5

1A - 4A VCC logic '1'

1C - 4C Ground logic '0'

1B	Counter Bit 0	'A'
2B	Counter Bit 1	'B'
3B	Counter Bit 2	'C'
4B	Counter Bit 3	'D'

## A - 5 Binary Divider (JB9,12)

	1	2	3	4	5	6	7	8	9
B	o	o	o	o	o	o	o	o	o
A	o	o	o	o	o	o	o	o	o

1A - 9A Common Output

1B	divide by 2
2B	divide by 4
3B	divide by 8
4B	divide by 16
5B	divide by 32
6B	divide by 64
7B	divide by 128
8B	divide by 256
9B	divide by 512



## A - 6 Clock Source Selection

	1	2	3	4
B	o	o	o	o
A	o	o--o		o

1A,2A TCLK - SIO input  
 3A,3B Baud Rate Generator  
 4A,2B RCLK - from RS-422 receivers  
 1B TCLK - to RS-422 drivers  
 4B RCLK - SIO input

## A - 7 DMA BUSRQ (JB13)

	A	B	
-BUSRQ (pin 41)	1	o o	-BUSRQ (pin 41)
BUSRQ buffered	2	o o	BUSRQ unbuffered

## A - 8 DMA Priority Chain (JB14)

	2	1	
BUSAK	o o	B	from BUSRQ buffer
-BAI (pin 40)	o o	A	-BAO (pin 41)

## A - 9 Module Address Selection (JB15)

	1	2	3	4	5
B	o	o	o	o	o
A	o	o	o	o	o

1A,5A Ground  
 1B Address Bit 7  
 2B Address Bit 6  
 3B Address Bit 5  
 4B Address Bit 4  
 5B Address Bit 3

**APPENDIX B**

**Z80 - STD BUS PIN OUT AND DESCRIPTION**

## APPENDIX B

### STD-Z80 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	Ground - System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	Address Bus (Tri-state, output, active high).
13	D0	
14	D4	
15	A7	Address Bus (Tri-state, output, active high).
16	A15	
17	A6	
18	A14	

# STD-Z80 BUS PIN OUT

19	A5	A0-A15 make up a 16-bit address bus. The address bus provides the address for memory (up to 65k bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Memory Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Memory Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-State output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 Systems DSTD.

# STD-Z80 BUS PIN OUT

36	/MEMEX	Memory expansion, not used on dy-4 Systems DSTD cards.
37	/REFRESH	/REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic zero and the upper 8 bits of the address bus contains the I register.
38	/DEBUG	/DEBUG (Input) used in conjunction with DDT-80 operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the /DEBUG line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
39	/M1	Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the opcode fetch cycle of an instruction. Note that during the execution of a 2-byte opcodes, /M1 will be generated as each opcode is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
40	STATUS 0	DMA priority chain input.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

## STD-Z80 BUS PIN OUT

- 42        /BUSRQ        Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.
- 43        /INTAK        Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.
- 44        /INTRQ        Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.
- 45        /WAITRQ        WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

## STD-Z80 BUS PIN OUT

46	/NMIRQ	Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will over-ride a /NMIRQ.
47	/SYSRESET	System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H and set Interrupt Mode 0.
48	/PBRESET	Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset.
49	/CLOCK	Processor Clock (Output, active low). Single phase system clock.
50	CNTRL	Auxiliary Timing
51	PCO	Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

## STD-Z80 BUS PIN OUT

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

### NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.



APPENDIX C  
DSTD-401 PARTS LIST

## DSTD-401 PARTS LIST

## APPENDIX C

QTY	DSTD401 PARTS LIST DESCRIPTION	PART NUMBER
INTEGRATED CIRCUITS		
2	U10,15	74S04
1	U17	74LS00
1	U14	74LS08
1	U9	74LS112
2	U5,U6	74LS163
5	U18,19,20,22,23	74LS245
2	U7,8	74LS393
1	U21	74LS682
2	U2,4	26LS33
2	U1,3	75159
1	U16	PAL16L8
2	U11,12	Z80[A]-DMA
1	U13	Z80[A]-SIO/2
DISCRETE COMPONENTS		
2	RN1,2	410A472
2	R18,R19	470 ohm 1/4 watt
1	R17	4.7K 1/4 watt
1	R16	10k 1/4 watt
6	R5,6,7,12,13,14	100 ohm 1/4 watt
8	R1-4,8-11	27 ohm 1/4 watt
1	R17	22 ohms 1/4 watt
1	R15	1.2K 1/4 watt
1	R16	220 ohms 1/4 watt
1	C14	TAG10M25
19	C1-12,15-20	8121-050-Z5U-104M
1	C21	CK05BX330K
1	Q1	2N3906
1	Y1	LOCO II 19.6608MHz
	JB1-15	CH6900W1S Headers
2	J2,3	(Unshrouded CHO 6926 26 Pin RA Header

DSTD-401 PARTS LIST

1	Printed Circuit Board	DY00460-H-A1-3
3	U16	20 Pin Socket
1	U11,12,13	40 Pin Socket
		Card Ejector



**APPENDIX D**  
**DSTD-401 SCHEMATIC**

TYPE		IC POWER PINS									
		+12	+12	+5	+5	GND					
PAL16L8		20	20	10	10	10					
220-DMA-3003		30	30	11	11	11					
220-DMA-3007		9	9	31	31	31					
26L353		16	16	8	8	8					
74LS08		14	14	7	7	7					
74LS112		16	16	8	8	8					
74LS163		16	16	8	8	8					
74LS245		20	20	10	10	10					
74LS293		14	14	7	7	7					
74LS3682		20	20	10	10	10					
74LS04		14	14	7	7	7					
75157		14	14	7	7	7					
74LS00		14	14	7	7	7					

ITEM	QTY	PART NUMBER	DESCRIPTION	DESIGNATION
60	1		PRINTED CIRCUIT BOARD	
59	1			
58	1			
57	1			
56	1			
55	1			
54	1			
53	2	CHS6302-WIS	CONNECTOR, 1+2 STRAIGHT HEADER	JB6, 3
52	2	CHS6304-WIS	1+4	JB6, 7
51	2	CHS6302-WIS	2+2	JB14, 13
50	4	CHS6303-WIS	2+3	JB5, 4, 2, 1
49	4	CHS6304-WIS	2+4	JB11, 10, 8, 7
48	1	CHS6306-WIS	2+6	JB15
47	2	CHS6303-WIS	CONNECTOR, 2+3 STRAIGHT HEADER	JB12, 9
46	2			
45	1		DIP SOCKET 20-PIN	AT U16
44	1		DIP SOCKET 40-PIN	AT U11, 12, 13
43	3			
42	1	100K II	CRYSTAL OSC. 19.4408 MHE	Y1
41	1	FOX1966	CRYSTAL 19.4408 MHE	Y1
40	1	2N3906	TRANSISTOR (70-18)	Q1
39	1		INTEGRATED CIRCUIT	U21
38	1	74LS3682		U16
37	1	74LS245		U15
36	1	74LS163		U14
35	1	220-DM-3007		U13
34	2	74LS04		U12
33	2	74LS00		U11
32	2	74LS112		U9
31	2	74LS293		U7
30	2	74LS3682		U5
29	2	75157		U4
28	2	74LS00		U3
27	2		INTEGRATED CIRCUIT	U2
26	2			
25	2			
24	2			
23	2			
22	2			
21	2	40K472	RESISTOR NETWORK 47K 10-SIP	RN1, 2
20	2		RESISTOR, FIXED COMP 22 1/4W	R21
19	1			
18	1			
17	1			
16	2			
15	1			
14	1			
13	1			
12	6			
11	8			
10	10			
9	2		CONNECTOR (2+13 R/A HEADER)	J2, 3
8	2			
7	1	5-208	CARD EJECTOR w/ SPRING PIN	
6	1			
5	1			
4	1	R314G3304	CAPACITOR, CERAMIC, 33PF 50V C21	
3	1	TAG10M25	CAPACITOR, TANTALUM, 10UF 25V C14	
2	1	BU100-100-100M	CAPACITOR, CERAMIC, 1000PF 50V C13	
1	1	BU100-100-100M	CAPACITOR, CERAMIC, 100PF 50V C12, 15-20	

SERIAL NETWORK CONTROLLER

SCALE: 1"=10"

APP'D: [Signature]

DWN: [Signature]

CHK: [Signature]

TOL: [Signature]

DATE: 12/10/15

FINISH: [Signature]

TITLE: DSTD401

DWG NO: DY00460-J-A1-A

ISS: 4

SH: 4

OF: 1

2

