

OPERATIONS MANUAL

**DSTD
402**

PARALLEL
INTERFACE
ADAPTER

(WINCHESTER INTERFACE)

DY00461

Covering part numbers:

DSTD-402-2.5 DSTD-402A-2.5

DSTD-402-4.0 DSTD-402A-4.0



dy-4 SYSTEMS INC.

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Revision A

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Acknowledgements

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SECTION 1

1.0 GENERAL INFORMATION

1.1 DSTD SERIES GENERAL DESCRIPTION

The dy-4 DSTD Series of Z80/STD-BUS compatible products was designed to satisfy the need for high performance microcomputer modules that could be quickly and inexpensively integrated into a variety of end-user applications. The popular STD-BUS motherboard interconnect system concept provides expandability as needs change. Support by numerous manufacturers provides the user with a choice from scores of compatible products.

The modules for the Z80/STD-BUS are a compact 4.5 x 6.5 inches (11.45 x 16.50 cm) which provides for system partitioning by function, i.e. CPU, Memory, I/O, etc. dy-4 SYSTEMS has been able to combine most popular functions on single cards to reduce system card count and cost.

1.2 DSTD-402 FEATURES

The DSTD-402 is a high-speed parallel interface for transfer of eight bit data between two intelligent systems.

One application is as a host adapter used between the STD-BUS and Winchester disk drive controllers operating with the Shugart Associates Standard Interface (SASI) protocol. Additional facilities available when used in this mode provide for auto acknowledge, DMA/non-DMA operation and parity generation/checking.

Another more general application is for data exchange between two processors. Used in this mode, the DSTD-402 may be configured to support a daisy-chain priority scheme to arbitrate among 8 such boards in a system; each able to receive and send parallel data at DMA speeds acting as either bus master or slave. One typical use is in multiprocessor local area networks.

Also included is an integrated delay network for non-standard I/O systems requiring hardware defined 'pauses' between control/data transfers. The parallel port design allows local/remote devices to latch data and control information or pass it asynchronously.



Figure 1 - 1 DSTD-402 MODULE

1.3 CARD CONFIGURATION BY PART NUMBER

The DSTD-402 may be purchased configured as a SASI interface. Part numbers for these configurations have a trailing 'A' after the DSTD-402 designation. The DSTD-402 may also be purchased with or without the DMA controller. Part numbers for these configurations have a trailing 'D' after the DSTD-402 designation. 2.5 or 4.0 Mhz operation is specified by the '-2.5' or '-4.0' suffix respectively.

Cards capable of more general parallel I/O operations are identified simply by DSTD-402, with the same suffix indicating rated clock frequency and DMA capability.

SECTION 2

2.0 FUNCTIONAL DESCRIPTION

2.1 INTRODUCTION

The DSTD-402 High Speed Parallel Interface is a multi-function card which can be adapted to many parallel I/O applications. It has an eight bit data bus with a ninth bit for parity. There is logic for automatic handshake and eight additional input/output lines for status and data flow control. The parallel drivers are terminated open collector drivers. The receivers are schmitt trigger buffers.

2.2 BLOCK DIAGRAM

The main elements of the DSTD-402 are shown in figure 2-1. The DSTD-402 has basically six sections - a DMA controller (280-DMA,3883), automatic handshake logic, an eight bit bi-directional data port, an eighth bit bi-directional control register, an eight bit write-only configuration register and a four bit status buffer.

2.2.1 DMA OPERATION

The DMA controller is an LSI device which allows memory to I/O, I/O to memory and memory to memory data transfers. It is configured under software control and is used to improve system throughput by allowing data transfers at the speed of the memory or the peripheral device instead of being limited by the processor program loops. It also allows the processor to do other tasks during data transfers such as checking for status or error conditions. DMA transfers may be done in one of three modes - continuous, burst or byte-at-a-time. (When using the DSTD-402 as a SASI interface use 'byte-at-a-time' for writing and burst mode for reading.) In all three modes the actual data transfer is controlled by the READY line.

The DMA receives its ready signal from one of two sources depending on whether the DSTD-402 is used as a host adapter for Winchester Disk Drives, (in which case /RDY is taken from the Winchester controller /REQUEST signal input,) or as a general purpose parallel I/O controller (from pin 32 at the J1 connector.)

The DMA Controller on the DSTD-402 may be the only DMA device in the system or it may be one of several. To determine which DMA has control of the bus, dy-4 SYSTEMS has implemented a Daisy-chain Priority scheme which allows bus location to determine priority among multiple DMA Controllers. If you are not using an STD-BUS Motherboard incorporating this design feature, (e.g. the DSTD-806 series,) then only one DMA device can operate in your system.

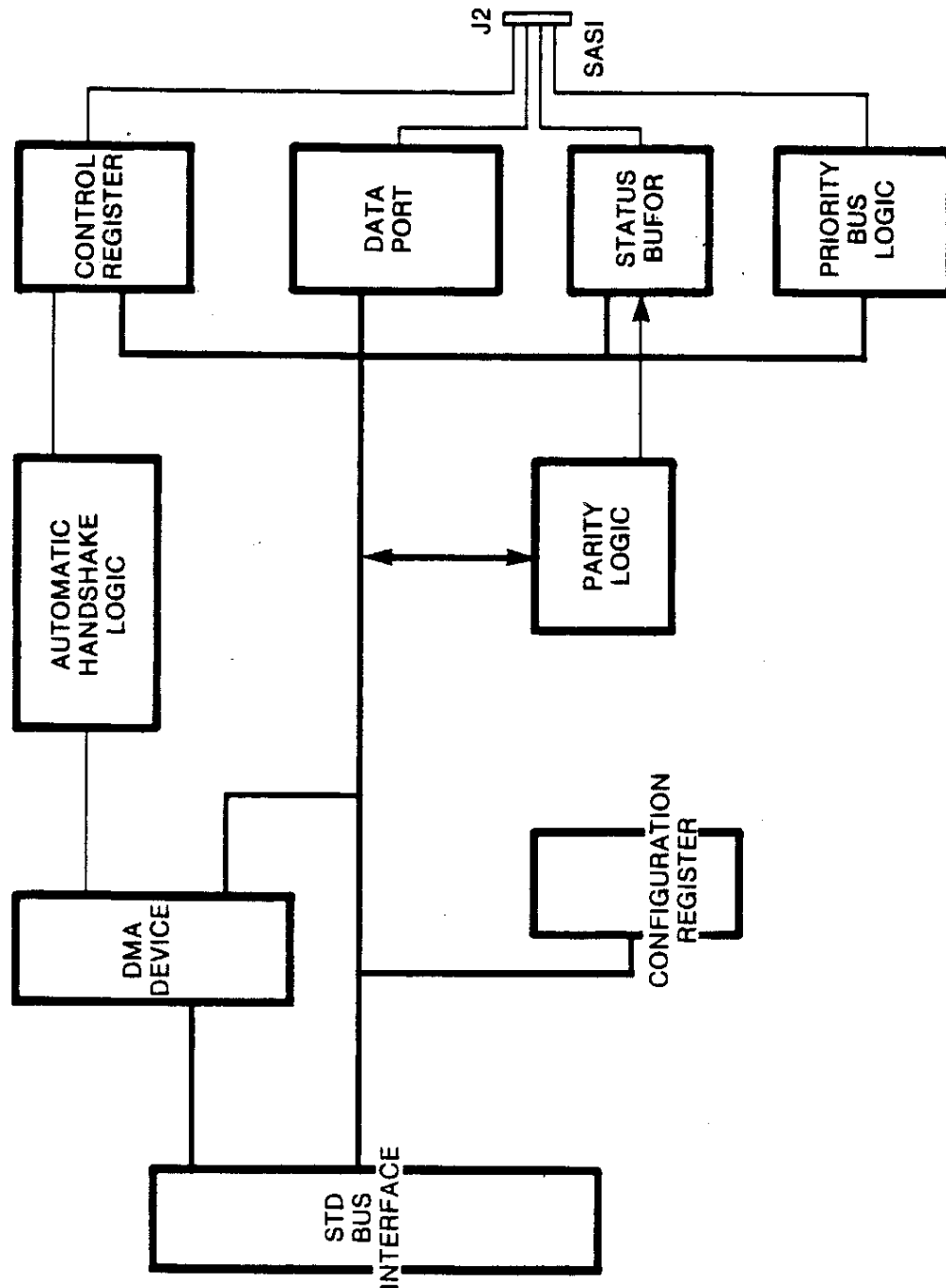


Figure 2 - 1 DSTD-402 BLOCK DIAGRAM

2.2.2 AUTO HANDSHAKE LOGIC

For most parallel applications including SASI controller applications, data exchanged between the DSTD-402 and Winchester Disk Controller is accompanied by a handshaking protocol for each byte transferred. This could consume a significant amount of processing time for a trivial function. The SASI interface uses signals called /REQUEST and /ACKNOWLEDGE.

The DSTD-402 incorporates auto-handshake circuitry which handles the /REQ-/ACK signals and the DMA's READY signal automatically.

As an example, the SASI interface data flow proceeds as follows. When the controller is ready to transfer data (either direction) it asserts the /REQ line. The interface generates a READY signal to the DMA controller which in turn executes a DMA cycle, transferring data to or from the DATA port. Each read or write of the DATA port (Base Address+1) is followed automatically by an assertion of the /ACK signal. The SASI Controller recognises /ACK and de-asserts it's /REQ line until the next transfer. Refer to the programming examples in Section 3.)

2.2.3 DATA PORT

The DSTD-402 has an eight bit bi-directional data port accessed through an I/O port located at the base address + 1. The direction of the data port can be determined by one of two methods. It can be set under software control using bit 0 of the Configuration Port (base address + 3) or, as is required by a SASI interface, it is controlled by one SASI interface control lines as determined by the SASI controller. JB6 is used to set the method of direction control.

Data writes are always latched however for data reads the data buffer may set to be transparent or latched. When set for latched mode the /REQ signal is used to control the latching. Latched mode is used when there is no control on how long the data will remain valid on the data bus during a read after the handshake signal.

The DSTD-402 also generates parity with each data output and checks parity on each data input. If a parity error occurs during a data input transfer a flag is set. This flag can be read using the status buffer (bit 0, base address + 3). The sense of parity (i.e. odd or even) is set using JBx. The parity flag is reset by writing to the data port.

2.2.4 CONTROL REGISTER

The DSTD-402 has an eight bit bi-directional control register accessed through the I/O port at the base address + 2. The bits of the register are divided into 3 groups and their direction is

controlled by bits in the configuration latch.

TABLE 2 - 1
CONTROL BIT GROUPING

BITS	CONFIGURATION BITS
0,1,2,3	2
4,5	3
6,7	4

When configured for a SASI interface the control lines are as follows. Bits 0,1,2,3 are /Busy, /Command-Data, /Message, /Input-Output; Bits 4 and 5 are /Reset and /Select; Bits 6 and 7 are uncommitted signals.

2.2.5 CONFIGURATION REGISTER

The configuration register allows some of the basic board functions such as driver direction control and handshake signal control to be software programmable. Table 2-2 shows the allocation of the bits. Bit 0 determines whether the card is in control of the transfer process or not. i.e. it is a master or a slave. Bits 1,2,3 and 4 control the direction of some of the drivers (refer to section 2.2.5). Bit 5 is used in multiple interface bus systems as a 'priority bus request signal'. Bits 6 and 7 are used to control the source of the DMA ready signal and the /REQ signal (refer to schematic).

For the SASI interface this register is simply initialized by loading it with 08H.

FIGURE 2 - 2
CONFIGURATION REGISTER

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
S1	S0	PREQ	DIR3	DIR2	DIR1	DIRO	M/S

S1,S0	-	Handshake signal source
	S1,S0	
	0 0	SASI type slave
	0 1	SASI type master
	1 0	high speed A
	1 1	high speed B

PREQ	-	Priority Bus Request 1 = active
DIR3	-	controls bits 6 & 7 of CONTROL register - 1 = output.
DIR2	-	controls bits 4 & 5 of CONTROL register
DIR1	-	controls bits 0,1,2 & 3 of CONTROL register
DIR0	-	controls direction of the DATA port if JB6 1A-1B installed 1 = input / 0 = output
M/S	-	Master/Slave - 1 = master

2.2.6 STATUS BUFFER

The DSTD-402 has a four bit status buffer. This buffer gives the processor access to four status bits, namely the state of the two handshake signals /REQ and ACK; the parity error flag and the bus priority grant bit.

Figure 2 - 3 STATUS BUFFER

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
n/u	n/u	PGNT	n/u	REQ	ACK	n/u	PERR

PGNT	-	Priority Bus Grant 1 = ready 0 = not ready
REQ	-	Request 1 = data transfer in process 0 = no transfer
ACK	-	Acknowledge 1 = data transfer being acknowledged.
PERR	-	Parity error 1 = error

The parity logic generates parity on writes and checks parity on reads. If during a read operation a parity error is detected, the parity error flag is set. The flag will remain set until the processor resets it by writing to the data port. The typical mode of operation is one in which data is transferred in blocks. The parity error flag is checked after each block transfer. If a

parity error has occurred the block may be retransferred.

2.2.7 PRIORITY BUS LOGIC

The most common applications for the parallel interface involve a straight connection between two devices. Typically one is a master and the other is a slave. However, there are applications where there are more than two devices and these other devices may be masters. e.g. multi-processor network systems. To accomodate multiple devices some kind of arbitration scheme is required. The DSTD-402 provides a bus arbitration scheme which allows for up to eight bus masters. One bus master is strapped to provide an arbitration clock to all the bus masters. Each master is assigned a priority using hardware jumpers. When a master wants access to the bus, it sets it's priority request flag. (bit 6 of the configuration register - base address + 3). If there are no other transfers in progress and it is the highest priority device requesting the bus, a priority bus grant flag will be set. (bit 5 of the status buffer - base address + 3). The master proceeds with the block transfer. When it has finished it releases the bus by clearing it's priority bus request flag. The parallel interface is an open collector bus.

2.3 WINCHESTER INTERFACE

The pin-out at connector J2 is designed to interface directly to most SASI compatible Winchester Drive Controllers. The organization is given below in Table 2-2. Signals designated with an asterisk are used for other parallel protocols.

TABLE 2 - 2

SASI INTERFACE CABLE CONNECTOR J2

Pin #	Signal Name	PIN #	Signal Name
2	/Data 0	26*	Priority Request
4	/Data 1	28*	parallel I/O Clock
6	/Data 2	30*	no connect
8	/Data 3	32*	unassigned
10	/Data 4	34*	unassigned
12	/Data 5	36	/busy
14	/Data 6	38	/Acknowledge
16	/Data 7	40	/Reset
18	/Parity	42	/Message
20*	Priority Bus 0	44	/Select
22*	Priority Bus 1	46	/command-Data
24*	Priority Bus 2	48	/Request
		50	/Input-Output

NOTE: For a description of the Signals, refer to the SASI literature. A '/' preceding the signal name indicates that it is

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active (asserted) when at a low logic level and inactive (de-asserted) at a high logic level. All SASI signals are terminated with a 220/330 ohm network and are bi-directional with schmitt trigger type inputs and open-collector outputs.

SECTION 3

3.0 OPTION PROGRAMMING

3.1 INTRODUCTION

The DSTD-402 may be user configured to meet a variety of needs for different applications. The following paragraphs describe the options available and the correct set-up for your use.

3.2 MODULE BASE ADDRESS SELECTION (JB8)

The Base Address of the DSTD-402 can be selected on any four byte boundary by strapping the binary match value desired at JB8 as described in Figure 3-1.

FIGURE 3-1

Base Address Selection JB8

	A	B	
1	o	o	= Bit 7
2	o	o	= Bit 6
3	o	o	= Bit 5
4	o	o	= Bit 4
5	o	o	= Bit 3
6	o	o	= Bit 2

A short between adjacent pins, (e.g. 1A-1B), produces a binary '0'. Leaving an Open produces a '1'. For the strapping shown, the binary value would equal FCh (the remaining two bits are decoded internally on the DSTD-402.) The Factory setting is all positions open as shown.

3.3 DATA BUS DIRECTION CONTROL (JB6)

For SASI Operation this option allows the INPUT/OUTPUT signal from the Winchester Controller to determine the direction of the data bus buffers (at Base Address+1) automatically. For non-SASI operation, the direction of the buffer is controlled directly by bit 1 value loaded into the CONFIGURATION register at Base Address + 3. Figure 3-2 shows how to make this set-up.

FIGURE 3-2

DATA BUS DIRECTION CONTROL JB6

	A	B
1	o	o
2	o	----o

1A-1B Shorted = Direction control from CONFIGURATION register.
 2A-2B Shorted = Direction control from Winchester controller
 Factory setting = 2A-2B, (Should be this way for SASI operation)

3.4 PARITY SENSE SELECTION (JB10)

Either Even or Odd parity is selectable using the option at JB10. Figure 3-3 shows how to select one or the other.

FIGURE 3-3

PARITY SENSE SELECTION JB10

1A	o	----	o	1B
2A	o		o	2B

1A-1B Shorted = Even Parity generated/Checked
 2A-2B Shorted = Odd Parity Generated/Checked
 Factory setting = 1A-1B as shown

3.5 BUS REQUEST/BUS ACKNOWLEDGE CHAIN (JB9)

The DSTD-402 makes use of the dy-4 Bus Request/Bus Acknowledge chain which allows more than one DMA device to exist on an STD-BUS. The option at JB9 allows the DSTD-402 to either pass through the Bus Request/Bus Acknowledge chain or sense it. Figure 3-4 describes how to set-up this option depending on your application.

FIGURE 3 - 4

BUS REQUEST/BUS ACKNOWLEDGE CHAIN JB9

	A	B
1	o	o
2	o	o

2A-1B = DMA device is not being used.
 1B-1A = DMA device being used in a single DMA system.
 1B-2B = DMA device being used in a multiple DMA system.
 1A-2A = DMA device being used in a multiple DMA system.

3.6 INPUT DATA/CONTROL LATCHING (JB3 and JB7)

Under some circumstances it is necessary to latch the data and control information being read from the external device. The REQ signal is used to latch data and control information. This feature is not required for the SASI interface. Figure 3-5 describes how to select either option.

FIGURE 3-5

DATA AND CONTROL LATCHING JB3 AND JB7

	A	B
1	o	o
2	o	o

1A-1B Shorted = Latched
 2A-2B Shorted = Unlatched
 Factory setting = 2A-2B. (Must be this way for SASI use)

3.7 DMA READY SOURCE (JB5)

When operating in the SASI mode under DMA the ready line to the DMA controller must be controlled by the /REQuest signal generated by the Winchester Controller. If a non-SASI parallel data exchange is to be controlled by the DMA, this signal can be brought in directly from pin 32 (bit 7) of the Control Port at Base Address+2. Figure 3-6 shows how this selection is made.

FIGURE 3-6

DMA READY SOURCE CONFIGURATION

JB5

```

1A  o---o  1B
2A  o    o  2B

```

1A-1B Shorted = Ready signal from Wichester controller
 2A-2B Shorted = Ready Signal from Control Port pin 32 (bit 7)
 Factory setting = 1A-1B. (Must be this way for SASI operation)

3.8 DELAY LINE TAPPING SELECTION (JB4)

When the DSTD-402 is used as a bus master, there are some situations when a time delay has to be inserted into the automatic handshake sequence. In a typical sequence the master will generate a /REQ when it is ready for a data transfer. The slave will respond by placing its data on the bus and asserting the /ACK line. Without the delay element this would cause the master to immediately de-assert the /REQ line which would in turn cause the slave to remove the data and de-assert the /ACK. The delay line is used to ensure there is sufficient set-up time and propagation time for the data paths.

The delay line is not required for the SASI interface nor is it required for most applications. It is not installed in standard versions of the DSTD-402. The board is layed out for common integrated delay line devices available for several manufacturers. Typical delay lines have several 'tappings'. The board is also layed out to take advantage of these tappings using a jumper block. Figure 3-7 describes this jumper block (JB4).

FIGURE 3-7

DELAY LINE TAPPING SELECTION JB4

	A	B	
1	o---o		= no delay
2	o	o	= tapping 1
3	o	o	= tapping 2
4	o	o	= tapping 3
5	o	o	= tapping 4
6	o	o	= tapping 5

Note: Only one strap should be installed. The factory setting is 1A-1B, (Must be this way for SASI operation)

3.9 PRIORITY ARBITRATION CLOCK (JB8)

The clock used to sequence all data exchanges between multiple DSTD-402's must be supplied from only one card. Figure 3-8 describes the configuration of JB1 to either source or sense the clock available on the data highway.

FIGURE 3-8

PRIORITY ARBITRATION CLOCK SOURCE

	A	B
1	o	o

1A-1B Open = This card receives clock from Data Highway
 1A-1B Shorted = This card supplies clock to data highway
 Factory setting = Open, (should be open for SASI operation)

3.10 PRIORITY LEVEL SELECTION (JB2)

The priority of any DSTD-402 on the data highway is determined by the strapping at JB2. Figure 3-9 describes the binary select value created here. The highest priority would be a value of 111B, the lowest value: 000.

FIGURE 3-9

PRIORITY SELECT CONFIGURATION

1A	o	o	1B	=	Bit 0	
2A	o	---	o	2B	=	Bit 1
3A	o	o	3B	=	Bit 2	

A short between adjacent pins, (e.g. 1A-1B), produces a binary '0'. Leaving an Open produces a '1'. For the strapping shown, the binary value would equal 5. The Factory setting is all positions open.

SECTION 4

4.0 SOFTWARE PROGRAMMING

4.1 INTRODUCTION

The DSTD-402 can be used as an interface between most SASI type Winchester Disk Controllers and the STD-BUS. Four Assembly language routines follow which should serve as a guide to the user in the construction of appropriate drivers for your application. We have used the INTEL/8080 opcodes here. The target Winchester Controller in these examples is the DTC 1403D.

We assume you have some familiarity with the DTC control syntax and with assembly language techniques in general.

The following equates are used to make the code easier to read.

HDDMA	equ	module base address
HDDATA	equ	module base address + 1
HDCNTRL	equ	module base address + 2
HDCONFG	equ	module base address + 3 (write)
HDSTAT	equ	module base address + 3 (read)
RST	equ	SASI reset command
SEL	equ	SASI select command
C%D	equ	SASI control/data flag
REQ	equ	SASI request flag
ACK	equ	SASI acknowledge flag
BSY	equ	SASI busy flag

4.2 DSTD-402 INITIALIZATION FOR SASI ADAPTER

The following routine will initialize the DSTD-402 Configuration Register at Base Address + 3 for use as a Winchester host adapter.

```

DSTD402.init:
    MVI    A,08H                ;SET UP CONFIGURATION REGISTER
    OUT    HDCONFG              ;on Host adapter
    MVI    A,RST                ;send a reset command to the
    OUT    HDCNTRL              ;dte controller
;
    PUSH   x                    ;90 t state delay
    POP    x                    ;the reset command must be held
    PUSH   x                    ;for at least 25 micro-seconds.
    POP    x
    PUSH   x
    POP    x

```

```

;
      XRA      A           ;clear the command port
      OUT      HDCNTRL     ;at Base Address + 2
      RET

```

4.3 DRIVE SELECT ROUTINE

The drive select routine gains the attention of the DTC 1403D and returns.

```

SELECT:
      IN       HDCNTRL     ;this is the control register
      ANI      BSY         ;bit 0 of the control register
      JNZ      SELECT      ;loop until busy is deasserted
;
      MVI      A,1         ;assert data bus bit 0 - part
      OUT      HDDATA      ; of the DTC select sequence
;
      MVI      A,SEL       ;assert select line, bit 5
      OUT      HDCNTRL
;
??loop:
      IN       HDCNTRL     ;wait until busy line gets set
      ANI      BSY         ;check bit 0
      JZ       ??loop      ;until it goes high
;
      XRA      A           ;now de-assert the SELECT line
      OUT      HDCNTRL
      RET

```

4.4 COMMAND OUTPUT ROUTINE

The Command Output routine transfers a six byte data field to the DTC controller to set up the read and write operations. The command field starts at address 'COMND'.

```

SENCOM:
      LXI      H,COMND     ;point to command string. The
                           ; first byte is the 'Read' or
                           ; 'WRITE' command and is later
                           ; used to determine which
                           ; subroutine to execute
      MVI      B,6         ;number of bytes to transfer
??lup1:
      IN       HDSTAT      ;wait for the controller to become
      ANI      REQ         ; ready to accept a byte. asserts
      JNZ      ??lup1      ; /REQ. (wait for bit 0 to go low)
;
      IN       HDCNTRL     ;ensure that the DTC controller is
      ANI      C%D ! I%O   ; in 'input' and 'command' mode
      CPI      2           ;
      RNZ

```

```

;
MOV      A,M                ;fetch the data from memory
OUT      HDDATA              ;transfer to the data port
INX      H                  ;increment command buffer pointer
DEC      B                  ;decrement the byte counter
JNZ      ??1up1              ;
RET

```

4.5 DATA READ/WRITE ROUTINE

After successfully selecting the drive and sending the command, the I/O operation can be performed. Both DMA and NON-DMA data transfers are supported by the DSTD-402. Both are illustrated.

```

READ/WRITE:                ;without DMA
MVI      B,0                ;sets up for 256 byte transfer
LXI      H,HSTBUF           ;DMA address, non-DMA xfer involved
LDA      COMND
CPI      HDRD               ;compares with a read function
JZ        %READ

%WRITE:                    ;else it must be write
;
??1up1:
IN        HDSTAT            ;wait for the controller to
ANI       REQ               ; assert the /REQ line.
JNR       ??1up1

;
??1up2:
IN        HDCNTRL           ;ensure that the controller is
ANI       C%D               ; in 'data' mode and ensure that
JNZ       ??exit            ; it stays in that mode.
;
MOV       A,M               ;get the next byte from buffer.
OUT       HDDATA            ;output to the data port.
INC       HL                ;increment the data buffer pointer
DEC       B                 ;decrement the data count.
JNZ       ??1up1

??exit  RET

;
%READ:
;
??1up1:
IN        HDSTAT            ;wait for the controller to
ANI       REQ               ; assert the /REQ line.
JNR       ??1up1

```

```

??lup2:      IN      HDCNTRL      ;ensure that the controller is
              ANI      C%D        ;in 'data' mode and ensure that
              JZ       ??exit     ;it stays in that mode.
;
              IN      HDDATA      ;input data from the data port.
              MOV      M,A        ;put the byte in the data buffer
              INC      HL         ;increment the data buffer pointer
              DEC      B          ;decrement the data count.
              JNZ      ??lup1
??exit:      RET

```

The following routines show the use of the DMA device to transfer data. Note that the Command bytes are still transferred to the controller using programmed I/O. It's not worth setting up the DMA chip to transfer six bytes. In fact DSTD-402 will not support command byte transfers under DMA control because it has special logic which inhibits a DMA transfer if the controller changes from data mode to command mode. This may happen unexpectedly if the controller detects an error. The adapter must be able to recognise this change so it can recover the status bytes returned by the controller indicating the cause the error.

The programmer sets up a table of information to initialize the DMA device. This table includes information on chip mode, byte count, source type and address and destination type and address. The user is encouraged to read the detailed data sheets from the DMA chip manufacturers (Mostek/Zilog), with particular reference to difference between memory-to-I/O transfers and I/O-to-memory transfers.

Note: Use Byte-at-a-time mode for transfers to the controller and either byte-at-a-time or burst mode when transferring from the controller. Burst mode is faster.

```

READ/WRITE:
              MVI      C,HDDMA    ;set up for control byte
                                   ;transfer to dma
              LXI      H,dmadat   ;point to dma data table
              LDA      COMND      ;check on transfer direction
              CPI      HDRD       ;i.e. read or write
              JZ       %READ
;
%WRITE:      MVI      A,B.TIME    ;BYTE-AT-A-TIME MODE
              STA      HDMODE     ;put into DMA set-up table
              MVI      B,dend-dmadat ;calculate number of bytes to
              JMPR     OUTIT      ;send to the DMA chip

```

```

;
%READ:  MVI      A,BURST      ;BURST MODE
        STA      HDMODE      ;put into DMA set-up table
        MVI      B,dend-dmadat-2;send two less bytes when
OUTIT:  OUTIR      ;setting up for reads.
        ;send data to DMA device

        MVI      A,87H      ;ENABLE DMA
        OUT      HDDMA
        RET      ;all done

```

4.6 STATUS ROUTINE

The status routine must be executed after read and write routines to be sure the command was completed successfully. Parity checking is an option on the both the DSTD-402 and most controllers which the user may enable to allow detect data/command transfer errors not associated with disk access problems.

```

STATUS:
        LXI      H,%STTUS      ;point to where two byte status
        MVI      B,2          ;returned will be placed
;
??1up1:
        IN       HDSTAT
        ANI      REQ          ;wait for /REQ to be asserted
        JNZ      ??1up1
;
??1up2:
        IN       HDCNTRL      ;ensure the controller is in
        ANI      C%D          ;command mode - if it's not
        JNZ      ??error      ;then we have an error.
;
;
        IN       HDDATA      ;stuff status
        MOV      M,A
;
        INX      H           ;to next location
        DJNZ     ??1up1
;
        DXC      H           ;point back at status byte
        DXC      H
        MOV      A,M
        ANI      00011111b    ;check relevant bits
        JNZ      ??error      ;else check message

        IN       HDSTAT      ;get parity status - makes
        RRC      ;sense for reads only.
        RNC      ;if bit 0 is not set, an error
        ;occured, return with carry
        ;cleared
;

```



```

    INX      H                ;point to completion message
    MOV      A,M
    ORA      A                ;message byte should be zeros
    CMC      ;compliment carry to set it
    RET      ;with A=0 if OKandz-flag set

```

4.7 DMA INITIALISATION ROUTINE

The DMA, if used, should be set up prior to each data transfer by transferring bytes from the following table to the DMA command port at Base Address+0. Refer to the chip manufacturers detailed data sheets for a complete explanation of the data required to set up the DMA device (Mostek/Zilog).

```

dmadat:
    .byte    0c3H            ;reset DMA
    .byte    79H
    .word    HSTBUR          ;always send to hstbuf
    .word    255             ;xfer length (assumes 256 byte
    .byte    14H             ;sector length)
    .byte    28H
hdmode:
    .byte    0               ;filled in at read/write
    .byte    HDDATA          ;the DSTD-402 data port
    .byte    9AH
    .byte    0CFH
    .byte    5               ;if writing, send the last
    .byte    0cfh            ;two bytes
dend      ==

```

SPECIFICATIONS

5.1 Functional Specifications

5.1.1 Word Size

Instructions: 8, 16, 24, or 32 bits

Data: 8 bits

5.1.2 Cycle Time

Clock period (T state): 400 ns for DSTD-402-2.5
250 ns for DSTD-402-4.0Instruction Cycle: Min. 4 T states
Max. 23 T states

5.1.3 I/O Addressing

There are four I/O addresses used on the DSTD-402. The base address is programmed using a jumper block.

PORT	ADDRESS
DMA DEVICE	base address + 0
PARALLEL DATA PORT	base address + 1
CONTROL PORT	base address + 2
CONFIGURATION PORT	base address + 3

5.1.4 System Clock

DSTD-402-2.5 2.5MHz Max

DSTD-402-4.0 4.0MHz Max

5.2 ELECTRICAL SPECIFICATIONS

5.2.1 STD Bus Interface

Bus Inputs: One 74LS load max.

Bus Outputs: $I_{OL} = 24 \text{ mA min. @ } V_{OL} = 0.5 \text{ Volts}$
 $I_{OH} = 15 \text{ mA min. @ } V_{OH} = 2.4 \text{ Volts}$

5.2.2 Operating Temperature

0 Degrees C to 50 Degrees C
95% humidity non-condensing

5.2.3 Power Supply Requirements

+5V +/- 5% @ 1.2A

5.3 MECHANICAL SPECIFICATIONS

5.3.1 Card Dimensions

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm)
long

0.48 in. (1.22 cm.) maximum height

0.062 in. (0.16 cm.) printed circuit board
thickness

5.3.2 STD Bus Edge Connector

56 pin Dual Readout; 0.125 in. centers

Mating Connector

Viking 3VH28/1CE5	(printed circuit)
Viking 3VH28/1CND5	(wire wrap)
Viking 3VH28/1CN5	(solder lug)

SECTION 6

6.1 FACTORY REPAIR SERVICE

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL. Enclose a letter containing the following information:

Name, address and phone number of purchaser
Date and place of purchase
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to the closest office:

Service Department
dy-4 SYSTEMS INC.
888 Lady Ellen Place
Ottawa, Ontario
K1Z 5M1, Canada

-or-

Service Department
dy-4 SYSTEMS INC.
3582 Dubarry Rd.
Indianapolis, IN 46226

Securely package and mail the circuit board, prepaid and insured, to the same address.

6.2 LIMITED WARRANTY

dy-4 warrants this product against defective materials and workmanship for a period of one year from date of purchase. This warranty does not apply to any product that has been subjected to misuse, accident, or improper installation, application, or operation, nor does it apply to any product that has been repaired or altered by other than our authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

NOTICE

The antistatic bag is provided for shipment of dy-4 products to prevent damage to the components due to electrostatic discharge.

Failure to use this bag in shipment will VOID the warranty.

APPENDIX A
OPTION JUMPER SUMMARY
DSTD-402

APPENDIX A

OPTION JUMPER SUMMARY

A - 1 JUMPER BLOCKS

The DSTD-402 has the following jumper blocks for user selectable option.

JB1	Priority Arbitration Clock
JB2	Priority Level Selection
JB3	Input Data Latching
JB4	Delay Line Tappings
JB5	DMA Ready Source
JB6	Data Bus Direction Control
JB7	Control Data Latching
JB8	Module Base Address Selection
JB9	Bus Request/Bus Acknowledge Priority Chain
JB10	Parity Sense Selection

A - 2 PRIORITY ARBITRATION CLOCK JB1

In a multi-master configuration one of the masters must supply the arbitration clock. Install the jumper on the master chosen to supply the clock. Not required for SASI interfaces.

		A	B	
Clock Source	1	o	o	PCLK (pin 28 of J2)

A - 3 PRIORITY LEVEL SELECTION JB2

In a multi-master configuration each master should be given a unique priority level. The levels are labelled 0 to 7, 7 being the highest. The level is set using JB2 which consisted of three pairs pins. Installing a jumper programs in a '0'. Not required for SASI interface.

	1	2	3
B	o	o	o
A	o	o	o

A1-A3	Ground
B1	bit '0'
B2	bit '1'
B3	bit '2'

A - 4 INPUT DATA/CONTROL LATCHING JB3/JB7

The data and control input buffers can be set up to be transparent or latching. When using latching mode /REQ is used to hold the data. Use transparent mode for SASI interfaces.

		1	2	
request	B	o	o	pullup
buffer latch input	A	o	o	buffer latch input

A - 5 DELAY LINE TAPPINGS JB4

In some configurations when the DSTD-402 is used as a master it is necessary to provide some delay elements in the automatic handshake logic. This feature is not used in SASI interfaces.

	1	2	3	4	5	6
B	o	o	o	o	o	o
A	o	o	o	o	o	o

A1	No Delay
A2	Delay Tapping 1
A3	Delay Tapping 2
A4	Delay Tapping 3
A5	Delay Tapping 4
A6	Delay Tapping 5
B1 - B6	Common

A - 6 DMA READY SOURCE JB5

DMA data transfers occur under the control of the READY input to the DMA device. This READY signal can be driven by the automatic handshake logic or directly from the interface J2.

		1	2	
Handshake logic	B	o	o	direct input J2 - pin 32
DMA READY input	A	o	o	DMA READY input

A - 7 DATA BUS DIRECTION CONTROL JB6

The direction of the data bus can be under software control or under the control of the bus master. In the case of the SASI interface the data bus direction is determined by the SASI controller.

		1	2	
Configuration reg.	B	o	o	from interface J2 - pin 50
(bit 1)			1	
data bus drivers	A	o	o	data bus drivers

A - 8 MODULE BASE ADDRESS SELECTION JB8

The module base address is determined by JB8

		1	2	3	4	5	6
B	o	o	o	o	o	o	o
			1	1	1	1	
A	o	o	o	o	o	o	o

A1	Address Bus Bit '2'
A2	Address Bus Bit '3'
A3	Address Bus Bit '4'
A4	Address Bus Bit '5'
A5	Address Bus Bit '6'
A6	Address Bus Bit '7'
B1-B6	Ground

A - 9 BUS REQUEST/BUS ACKNOWLEDGE PRIORITY CHAIN JB9

The dy-4 SYSTEMS implementation of the Z80-STD bus allows for multiple DMA devices. To do this bus signals 40 and 41 are used to set up a DMA priority chain similar to the interrupt priority chain. The DSTD-402 is designed to take advantage of this chain as well as being compatible with backplanes from other manufacturers. It is normally shipped for single DMA device systems unless it is shipped in a dy-4 SYSTEMS computer product.

/BAO (pin 41)	B	1 o	2 o	buffered/BAO
			1	
/BAI input	A	o	o	/BAI (pin 40)

A - 10 PARITY SENSE SELECTION

The DSTD-402 may be set up to generate and check either ODD parity or EVEN parity. Odd parity is used for the SASI interface.

		1	2	
EVEN parity generator	B	o	o	ODD parity generator
parity output	A	o	o	parity output

APPENDIX B

STD-Z80 BUS PIN OUT

APPENDIX B

STD-Z80 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	Ground - System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	
15	A7	Address Bus (Tri-state, output, active high).
16	A15	
17	A6	
18	A14	

STD-Z80 BUS PIN OUT

19	A5	A0-A15 make up a 16-bit address bus. The address bus provides the address for memory (up to 65k bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Memory Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Memory Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-State output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 Systems DSTD.

STD-Z80 BUS PIN OUT

36	/MEMEX	Memory expansion, not used on dy-4 Systems DSTD cards.
37	/REFRESH	/REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic zero and the upper 8 bits of the address bus contains the I register.
38	/DEBUG	/DEBUG (Input) used in conjunction with DDT-80 operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the /DEBUG line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
39	/M1	Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the opcode fetch cycle of an instruction. Note that during the execution of a 2-byte opcodes, /M1 will be generated as each opcode is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
40	STATUS 0	DMA priority chain input.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

STD-Z80 BUS PIN OUT

- 42 /BUSRQ Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.
- 43 /INTAK Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.
- 44 /INTRQ Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.
- 45 /WAITRQ WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

- 46 /NMIRQ Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will over-ride a /NMIRQ.
- 47 /SYSRESET System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H and set Interrupt Mode 0.
- 48 /PBRESET Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset.
- 49 /CLOCK Processor Clock (Output, active low). Single phase system clock.
- 50 CNTRL Auxiliary Timing
- 51 PCO Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

STD-280 BUS PIN OUT

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.

APPENDIX C
DSTD-402 PARTS LIST

APPENDIX C

Parts LIST FOR DSTD-402[A]-2.5 (-4.0)

(* parts preceeded with an '*' are not populated in standard versions; parts preceeded with a # are not populated in the non-dma version.)

QTY	DESIGNATION	PART NUMBER
INTEGRATED CIRCUITS		
3	U1,7,12	74LS240
5	U2,3,5,6,20	7438
*1	U4	PAL16L8-402-20-1
3	U8,9,15	74LS373
1	U10	74LS280
*1	U11	Delay Line
2	U13,14	74LS273
1	U16	74LS32
#1	U17	Z80[A]-DMA
3	U18,19,21	74LS74
1	U22	PAL16L8-402-10-1
1	U23	74LS139
1	U24	74LS04
1	U25	74LS08
1	U26	74LS253
5	U27,28,29,31,32	74LS245
1	U30	74LS682

DISCRETE COMPONENTS

2	R1,4	4.7K 1/4W 5%
2	R2,5	10K 1/4W 5%
1	R3	270 1/4W 5%
3	RN1,3,4	330,220
1	RN2	4.7K
20	C1-16,18-21	.1 uf ceramic
1	C17	10 uf tantalum
1	J1	

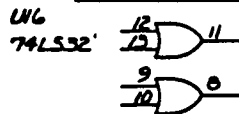


APPENDIX D
DSTD-402 SCHEMATIC

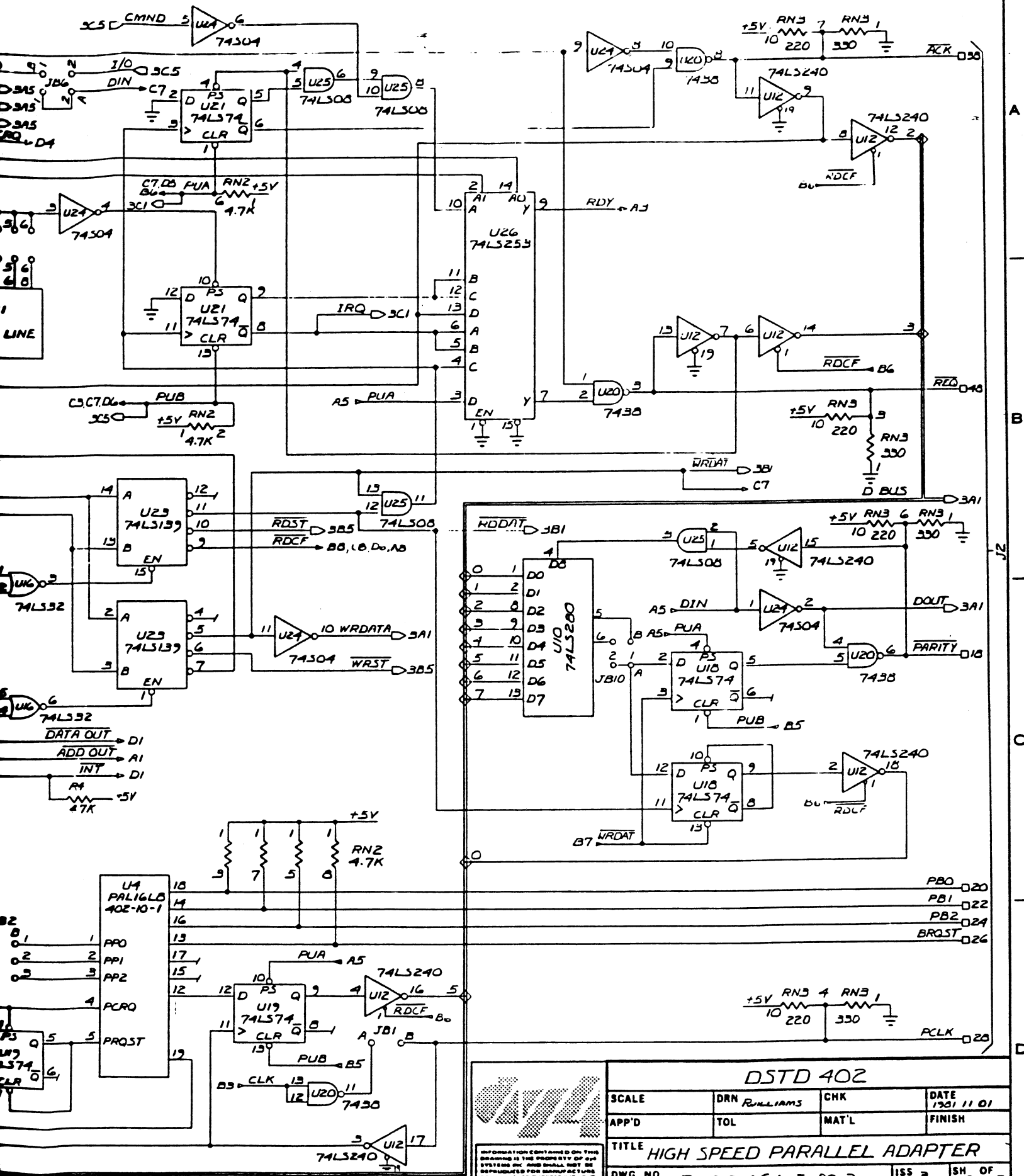
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59				
58				
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56				
55				
54				
53				
52				
51				
50				
49				
48				
47				
46				
45				
44				
43	1	5-208	CARD EJECTOR W/SPRING PIN/SCANNER	
42				
41	2		SOCKET (20-PIN DIP)	AT U4 & U22
40	1		SOCKET (40-PIN DIP)	AT U17
39				
38	1	74LS682	INTEGRATED CIRCUIT	U30
37	5	74LS245		U27,28,29,31 & 32
36	1	74LS253		U26
35	1	74LS08		U25
34	1	74S04		U24
33	1	74LS159		U23
32	3	74LS74		U18,19 & 21
31	1	280-DMA-3823		U17
30	1	74LS92		U16
29	2	74LS273		U13 & 14
28	1	DT2M1-100	(DELAY LINE)	U11
27	1	74LS280		U10
26	3	74LS373		U8,9 & 15
25	2	PAU6LB-402-10-1		U4 & 22
24	5	7438		U2,3,5,6 & 20
23	3	74LS240	INTEGRATED CIRCUIT	U1,7 & 12
22				
21				
20				
19				
18				
17	1		RESISTOR NETWORK, 4.7K	RN2
16	3		RESISTOR NETWORK, 330/220	RN1,3 & 4
15				
14				
13	1		RESISTOR, FIXED COMP, 270, 1/4W, 5%	R3
12	1		RESISTOR, FIXED COMP, 10K, 1/4W, 5%	R5
11	2		RESISTOR, FIXED COMP, 4.7K, 1/4W, 5%	R1 & 4
10	2		CONNECTOR (2x6 HEADER)	J8 & 6
9	1		CONNECTOR (2x3 HEADER)	J82
8	6		CONNECTOR (2x2 HEADER)	J83,5,6,7,9 & 10
7	1		CONNECTOR (1x2 HEADER)	J81
6	1	DM-50LP-3/16-T6	CONNECTOR (ROBINSON-MUGENT)	J2
5				
4	20		CAPACITOR, CERAMIC, .1μF, 50V	C1-16, 18-21
3	1		CAPACITOR, TANTALUM, 10μF, 25V	C17
2				
1	1		PRINTED CIRCUIT BOARD	
ITEM	QTY	PART NUMBER	DESCRIPTION	DESIGNATION

IC POWER PINS					
TYPE	+12	-12	+5	-5	GND
74LS168-102-10-1			20		10
200-DMM-3005			11		30
74LS08			14		7
74LS139			16		8
74LS240			20		10
74LS245			20		10
74LS255			16		8
74LS273			20		10
74LS280			14		7
74LS32			14		7
74LS373			20		10
74LS682			20		10
74LS74			14		7
74S04			14		7
74S8			14		7

UNUSED GATES



DSTD 402			
SCALE	DRN <i>R. WILLIAMS</i>	CHK	DATE <i>1/20/11/01</i>
APP'D	TOL	MAT'L	FINISH
TITLE <i>HIGH SPEED PARALLEL ADAPTER</i>			
DWG NO. <i>DY00461-1-A1-3</i>	ISS <i>3</i>	SH OF <i>1</i>	5

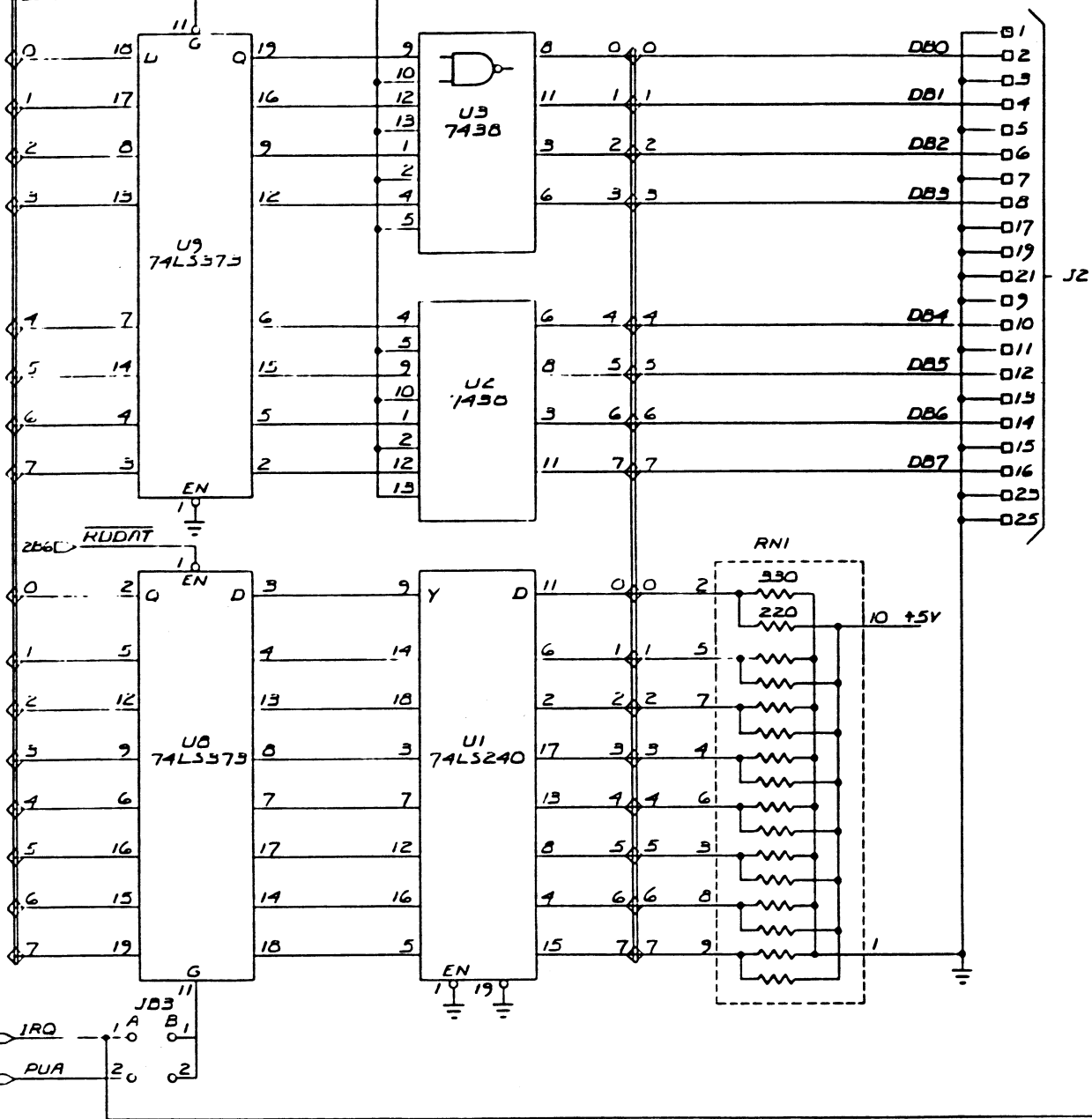


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APP'D	TOL	MAT'L	FINISH
TITLE <i>HIGH SPEED PARALLEL ADAPTER</i>			
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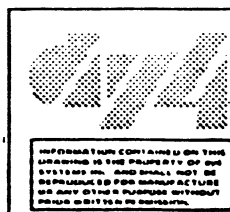
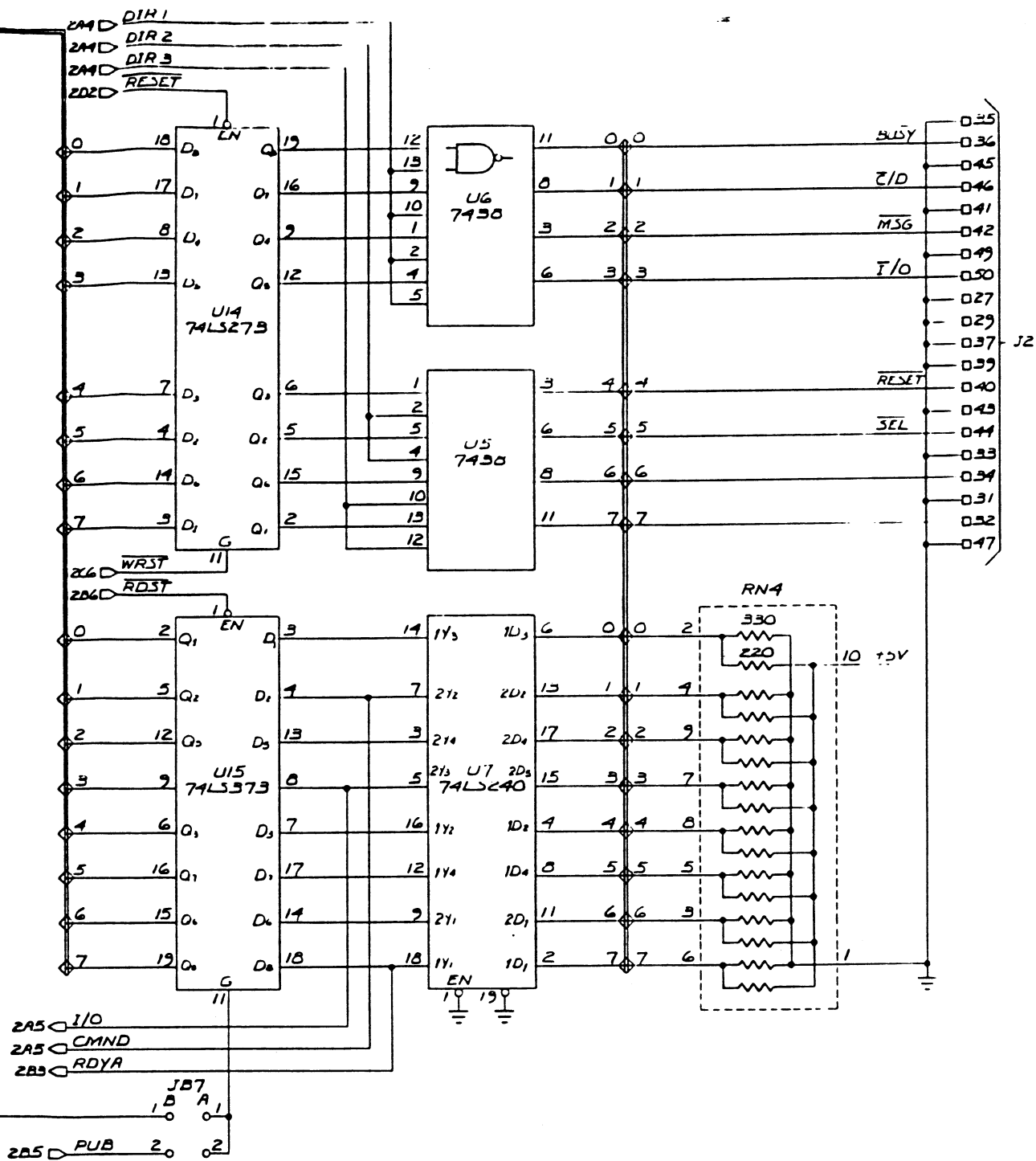
DBUS

286C 18X17
286C WHIATA



2A5
2A5
2B3

2A5



DSTD 402			
SCALE	DRN WILLIAMS	CHK	DATE 1981 11 01
APP'D	TOL	MAT'L	FINISH
TITLE HIGH SPEED PARALLEL ADAPTER			
DWG NO. DY00461-1-A3-3	ISS 3	SH OF 3	