

# OPERATIONS MANUAL

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**DSTD  
503** BYTEWIDE  
MEMORY  
CARD  
DY00489

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**dy-4 SYSTEMS INC.**

DOCUMENT NO. DSTD-503-M  
REVISION A

DSTD-503  
BYTEWIDE MEMORY CARD  
DY00489

DSTD-503 Bytewide Memory Card for STD-Z80 BUS

DSTD-503A Bytewide Memory Card for STD-2088 BUS

PREPARED BY: dy-4 SYSTEMS INC.

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## 1.0 GENERAL INFORMATION

### 1.1 Introduction

The dy-4 SYSTEMS INC. DSTD-503, Figure 1-1, is a general purpose byte-wide memory module. It has twelve 28 pin sockets which can individually be configured for any of the popular byte-wide memory devices. The DSTD-503 supports PROM, EPROM, RAM and EEPROM devices.

The software programmable memory mapping facility allows the sockets to be individually positioned in the processor's address space. This is particularly useful in systems requiring a large amount of memory and overlays.

The DSTD-503A is compatible with dy-4's DSTD-8088 series of modules. The module can be positioned anywhere in the 8088 processor's 1 megabyte address space on any 64K byte boundary.

### 1.2 DSTD Series General Description

The DSTD series was designed to satisfy the need for low cost OEM microcomputer modules. The DSTD-Z80 BUS uses a motherboard interconnect system concept. The modules for the STD-BUS are a compact 4.5 x 6.5 inches which provides for system partitioning by function, e.g. CPU, Memory, I/O, etc. This smaller module size makes system packaging easier, while increasing MOS-LSI densities provide high functionality per module.

### 1.3 DSTD-503 Features

- \* Compatible with STD-Z80 and STD-8088 bus
- \* Twelve 28 pin memory sockets
- \* Each socket individually configurable for the following devices and equivalents

EPROM		RAM	EEPROM
2716	(2Kx8)	4802 (2Kx8)	X2816A (2Kx8)
2732	(4Kx8)	2186 (8Kx8)	
2764	(8Kx8)		
27128	(16Kx8)		

- \* Each socket can be individually positioned in the processor's address space on a 4K/8K/16K address boundary. 2Kx8 devices are usually used in groups of two to maintain memory continuity.

- \* More than one DSTD-503 can be used in a system at a time. The DSTD-503 powers-up disabled and is enabled under software control on a per socket basis.
- \* The mapping RAM is accessed as an I/O port.





DSTD-503 MODULE

## 2.0 FUNCTIONAL HARDWARE DESCRIPTION

### 2.1 Introduction

The DSTD-503 consists basically of STD bus interface logic, memory mapping logic and twelve sockets each with its own 4x3 configuration jumper block. Logic is included to allow the DSTD-503A to be configured for the STD-8088 bus. The STD-8088 bus uses four data bits at the beginning of the memory cycle to extend the address space to 1 megabyte.

### 2.2 Block Diagram Description

Figure 2-1 is a block diagram illustrating the flow of address, data and control signals on the DSTD-503. The following paragraphs describe the function of each of the major blocks.

#### 2.2.1 STD Bus Interface

The STD Bus Interface consists of buffers and transceivers. Its function is simply to ensure that the bus loading specifications are met.

#### 2.2.2 Memory Mapping Logic

The main element of the memory mapping logic is a very high speed 16 x 6 bit memory array. It is a read/write memory array. There is also a latch to enable and disable the whole DSTD-503 card.

The array is accessed using a single I/O port as discussed in Section 3. A jumper block is used to position this I/O port in the processor's I/O address space. Each cell in the mapping array is arranged as follows.

B7	B6	B5	B4	B3	B2	B1	B0
CE	X	SE	DT	S3	S2	S1	S0

S0-S3 Specifies the socket number. Note that the socket labelled U1 is socket 0. U2 is socket 1 etc.

DT Device Type specifies 2K device or other

1 = 2K device

0 = All other size devices

SE            Socket enable

1 = enable  
0 = disable

X            Unused

CE           Card Enable. The card enable latch is common to all cells.

1 = enable  
0 = disable

To see how the mapping RAM is used we will first consider the STD-Z80 bus systems. The processor's 64K byte address space is divided into 16 four Kilobyte cells. Each of the 6 bit entries in the mapping RAM corresponds to one of the sixteen cells. Assigning a socket is done by writing the socket number (0 to 11) into the appropriate cell in the mapping RAM.

The DSTD-503 is designed primarily for 4Kx8 and larger devices. 2Kx8 devices they are usually used in groups of two for memory continuity. One of the 6 bits in the mapping RAM (DT) is used when a 2K device is being installed to re-configure the memory mapping logic. This is discussed in more detail in later sections.

For STD-8088 bus systems, the card is first positioned using hardwired jumpers on a 64 Kilobyte boundary within the processor's 1 Megabyte address space. The sockets are then assigned as in the STD-Z80 description above. Note however the STD-8088 configuration does not support 2kx8 devices without leaving holes in the address space. That is, the mapping logic assumes that each socket is at least a 4kx8 device. If a 2kx8 (or 1kx8) device is used it will be "repeated" in the second half of the 4K byte cell. This however, because of the mapping flexibility of the module, will not be of concern in most systems.

In 8088 systems the DSTD-503A uses the four most significant bits of the 16 bit I/O address bus as the cell address in the memory mapping array. (as does the DSTD-328 dynamic RAM module)

The memory mapping logic is disabled by a system reset. This also implies that it powers-up disabled. This allows multiple memory modules to be used in a system. The module can be enabled under software control. This is done writing to any cell with bit 7 of the data byte set. The module can be disabled by writing to any cell with bit 7 cleared.

Some 8kx8 RAM parts are pseudo static and generate a NOT READY signal when they are doing an internal refresh cycle. These devices are supported using the STD bus /WAITRQ line

### 2.2.3 Memory Sockets

Each of the memory sockets can be individually configured for any of the supported byte-wide memory devices. Each socket has a 4x3 jumper block which is used to configure the socket for its intended use. For example, some devices expect power to be applied to different pins than other devices. Some 2kx8 RAMs expect the write strobe to be pin 23 and 8kx8 RAM's expect the write strobe to be on pin 27. Table 2-1 shows some of the popular memory devices and how they expect certain pins to be connected.

Note that the pin numbers are given for a 28 pin socket. If a 24 pin device is used, it is inserted such that pin 1 of the device is in pin 3 of the socket. Thus pins 1 to 12 of the device corresponds to pins 3 to 14 of the socket and pins 13 to 24 of the device correspond to pins 15 to 26 of the socket.

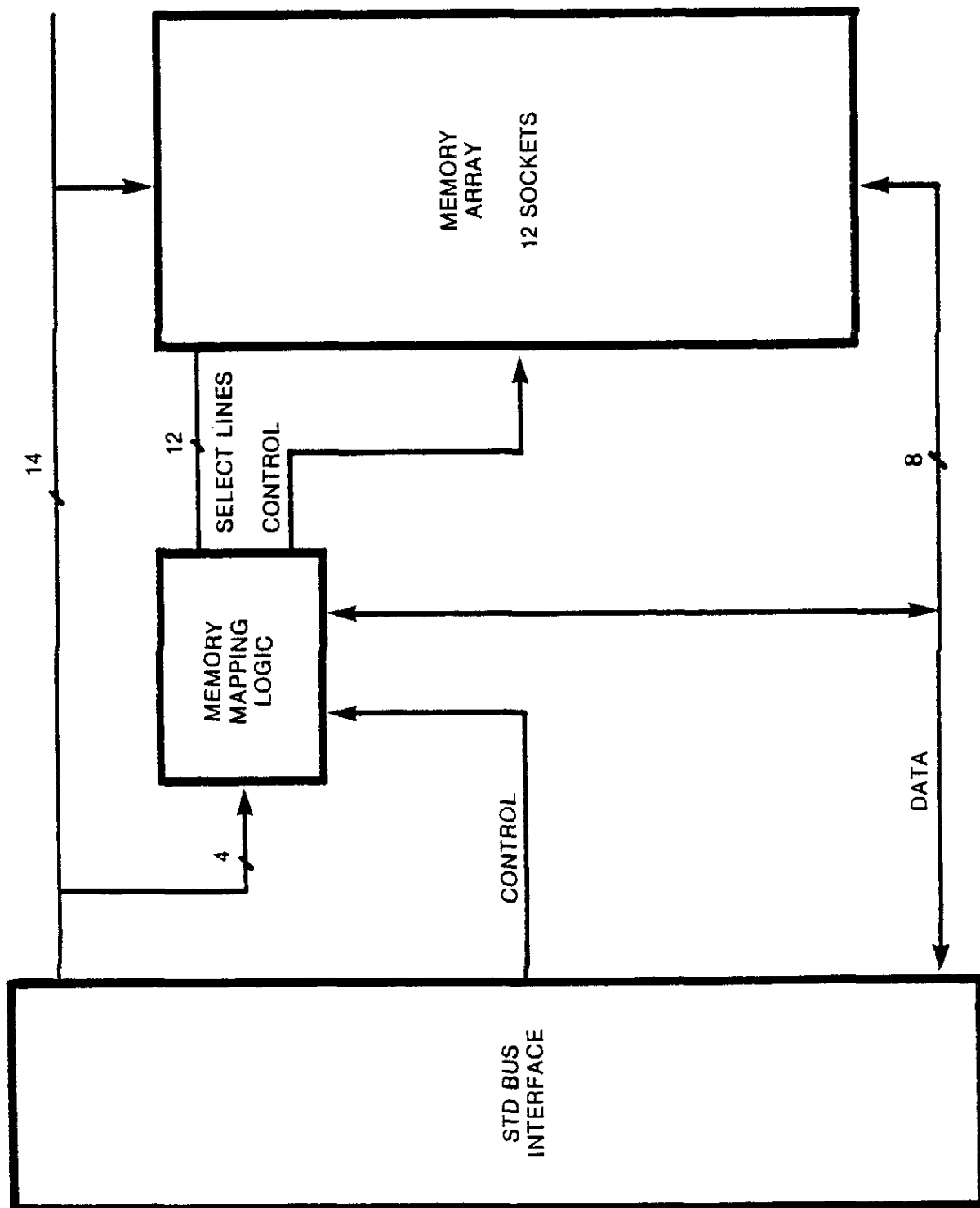


FIGURE 2-1 DSTD-503 BLOCK DIAGRAM

Type	Manufacturer	#	PINS					Jumper Setup
			27	26	23	21	1	
2 K x 8 CRAM	Toshiba	TC5517A/B	—	V <sub>CC</sub>	WE	A <sub>10</sub>	—	V <sub>CC</sub> : B3-C1 WE: B1-B2      A <sub>10</sub> : A1-C3
8 K x 8 CRAM	Toshiba	TC5564/5	WE	CE <sub>T</sub>	A <sub>11</sub>	A <sub>10</sub>	N/C	CE: B3-C1      A <sub>11</sub> : B1-C2 WE: A2-B2      A <sub>10</sub> : A1-C3
8 K x 8 DRAM	Intel	2186	WE	N/C	A <sub>11</sub>	A <sub>10</sub>	RPY	WE: B2-A2      A <sub>11</sub> : B1-C2 RPY: B4-C4      A <sub>10</sub> : A1-C3
4 K x 8 EPROM	Intel	2732A	—	V <sub>CC</sub>	A <sub>11</sub>	A <sub>10</sub>	—	V <sub>CC</sub> : B3-C1      A <sub>11</sub> : B1-C2 A <sub>10</sub> : A1-C3
8 K x 8 EPROM	Intel	2764	PGM	N/C	A <sub>11</sub>	A <sub>10</sub>	V <sub>PP</sub>	V <sub>PP</sub> : B4-C1      A <sub>11</sub> : B1-C2 PGM: A2-B2
16 K x 8 EPROM	Intel	27128	PGM	A <sub>13</sub>	A <sub>11</sub>	A <sub>10</sub>	V <sub>PP</sub>	PGM: A2-B2      A <sub>11</sub> : B1-C2 A <sub>13</sub> : B3-A3      V <sub>PP</sub> : B4-C1 A <sub>10</sub> : A1-C3
2 K x 8 E <sup>2</sup> PROM	XICOR	X2816A	—	V <sub>CC</sub>	WE	A <sub>10</sub>	—	Same as 2 K x 8 CRAM

TABLE 2-1  
 BYTEWIDE MEMORY BOARD JB1 TO JB12 MEMORY CONFIGURATION

### 3.0 USER SELECTABLE OPTIONS

#### 3.1 Introduction

The DSTD-503 incorporates many strapping options to provide the user with a high degree of flexibility in system configurations. This section describes the use of the available jumper options.

#### 3.2 STD Bus Selection (JB14)

The DSTD-503 is designed for use in both the STD-Z80 bus and the DSTD-8088 bus. The difference in operation is that when the DSTD-503 is configured for the STD-8088 bus it does not support 2K byte devices. The devices can still be used but the memory will not be contiguous.

Putting a jumper between pins 1 and 2 of jumper block JB14 selects STD-Z80 bus mode and putting it between pins 2 and 3 selects STD-8088 mode.

#### 3.3 I/O Port Address Selects (JB17)

The memory mapping RAM is accessed using an I/O port. During an I/O cycle the DSTD-503 compares the bottom eight address bits (A0-A7) to the settings of a user defined jumper block JB17. Four bits of the upper part of the address bus (A12-A15) are used to address the required cell in the mapping memory RAM.

The following shows how the jumper block is mapped to the address bus.

JB17	Address Bit
B8	0
B9	1
B6	2
B5	3
B4	4
B3	5
B2	6
B1	7

To program a '0' install a jumper between the corresponding A and B row pins. When no jumper is installed the bit is programmed as a '1'. For example, to assign an I/O port address of B5H to DSTD-503, install jumpers A JB17: A7 to B7, A4 to B4, A2 to B2.

### 3.4 Memory Bank Selection (JB13) [DSTD-8088 only]

In a DSTD-8088 system the DSTD-503A module can be positioned in any of the sixteen 64K byte banks within the 8088's 1 Megabyte address space. This positioning is hardwired using JB13. The settings of JB13 are compared with the most significant 4 bits of the address bus (A16 - A19) at the beginning of a memory cycle and then latched for the rest of the cycle. Installing a jumper between corresponding pins in rows A and B programs the bit pin to a '0'. Installing a jumper between corresponding in rows B and C programs the bit to a '1'.

JB13				Address Bit
A	B	C		
1	0	0	0	A16
2	0	0	0	A17
3	0	0	0	A18
4	0	0	0	A19

### 3.5 Memory Cell Size (JB15)

To maintain compatibility with existing dy-4 systems memory management arrangement JB15 allows the cell size to be set for 8K bytes. This mode however expects that the sockets will be occupied with 8 or 16K byte devices only. JB15 is normally set for 4K byte cells, i.e. pins 1 to 2 jumpered.

Jumpering pin 2 and 3 selects 8 Kilobyte cell size.

JB15		
1	0	4 Kilobyte cells
2	0	
3	0	8 Kilobyte cells



### 3.6 Memory Socket Configuration

Jumpers JB1 through JB12 are used to individually configure the memory sockets for the different byte-wide memory device. Table 2-1 indicates the differences between the various supported devices. The following shows how the signals are arranged in the jumper block and Table 2-1 shows the connections required for the more popular devices.

	A	B	C
1	Pin 21 A10/L	Pin 23 WE/A11	+5VOLTS
2	Pin 27 WE/11	STD WR STROBE	STD ADDRESS A11
3	STD ADDRESS A13	PIN 26 VCC/A13	STD ADDRESS A10
4	GND	PIN 1 +5/RDY	STD READ STROBE

### 3.7 DMA Priority Chain (JB16)

dy-4 SYSTEMS has implemented a DMA priority chain using pin 41 and unused a pin in the STD-Z80 bus definition - pin 40. When using the DSTD-503 in a dy-4 SYSTEMS backplane this jumper should be installed to ensure that the chain is not broken. In other systems, this jumper should not be installed.

## 4.0 PROGRAMMING THE DSTD-503

### 4.1 Introduction

The DSTD-503 has 12 byte-wide memory sockets capable of supporting 2K, 4K and 8K memory devices. The memory is arranged in 4K pages (If 2K devices are used they are grouped in twos. If 8K devices are used they are effectively divided into two 4K segments).

Any 4K device, group or segment can be positioned anywhere in the processor's address space with the exception that with 8K devices the lower 4K bytes are confined to even numbered segments and the upper 4K bytes are confined to the odd numbered segments. This is not a significant restriction.

### 4.2 Programming

Programming the DSTD-503 involves writing to an on-board mapping RAM which is accessed through a single I/O port. The DSTD-503 powers up disabled. It is also disabled by a system reset. The memory is managed using a 16 x 6 bit mapping RAM. It is arranged such that each of the 16 six bit registers corresponds to one of the sixteen 4K byte cells in the processor's address space. A socket is assigned to a processor cell (See note # 1) by writing its number into the associated 6 bit register in the mapping RAM.

Four of the six bits of the registers are used to specify the socket number. The fifth bit is used to enable the socket on the board. The sixth bit is used to handle 2K byte devices. If the socket contains a 2K byte device this bit must be set. If a 4K or 8K device is used the bit must be cleared.

On power-up or reset the memory-map RAM should be initialized. This is done by clearing the RAM to all zeros.

For STD-Z80 bus systems the RAM is accessed through a single I/O port using the special Z80 I/O instructions of the form IN r, (C) or OUT (C), r.

These instructions place the contents the B register on the upper half of the address bus during the transfer. The DSTD-503 uses the most significant 4 bits of the address bus as the address bus of the mapping RAM for both Memory cycles and I/O cycles. Thus the most significant 4 bits of the B register are loaded with the cell number, the C register is loaded with the I/O port address, the socket number is loaded into the A register and an output instruction executed.

**Note #1** A cell is defined as a 4K byte "piece" of the microprocessor's address space. A cell always starts on a 4K boundary. Cells are numbered from 0 to 15.

In STD-8088 system bits A12, A13, A14, A15 are used for addressing into the mapping RAM.

The following uses Z80 instructions to illustrate board setup. To initialize the mapping RAM write zeros to all locations.

```
LD  A,0           ;used for address calculation
LD  D,0           ;D will be output to MAP
LD  B,0           ;start at cell zero
LD  C,I/O PORT   ;DSTD-503 port address
LD  E,16          ;16 cells on each board
```

LOOP:

```
OUT  (C), D       ;output
ADD  A, 10H       ;move to next cell
LD   B, A         ;address is 4 MSB's of B
DEC  E           ;loop counter - 16 cells
JR   NZ, LOOP     ;loop
```

Having initialized the mapping RAM we can now start assigning sockets to the processor's address space. Thus for example to assign socket 9 (of 0 to 31) to the processors fourth cell (4000H to 4FFFH) write 9 or'ed with the enable bit (bit 5) into map register four.

```
LD  A, 9 + 00100000B ;socket 9 plus enable bit
LD  B, 01000000B     ;cell 4
LD  C, I/O PORT      ;board address
OUT (C), A           ;
```

Other cells are set up in this manner.

Up to this point the sockets have been enabled on the board but the board has not been enabled. To enable the board set bit 7 of any one of the map registers.

```
LD  C, I/O PORT      ;board address
IN  A, (C)           ;read any register
OR  10000000B        ;set bit 7
OUT (C), A           ;output again
```

To disable the board clear bit 7 of any one of the MAP registers.

```
LD  (C), I/O PORT      ;board address
IN  A, (C)              ;read any register
AND 01111111B           ;clear bit 7
OUT (C), A              ;output again
```

Cell assignments can be made "on the fly" without disabling the board. Multiple boards can be used in a system as long as there are no cell conflicts. i.e. sockets on two different boards are assigned and enabled for the same cell.

#### 4.2.1 Handling 2K Devices

When using 2K devices they must be used in groups of two or rather two adjacent sockets must be allocated to the same 4K byte group on a 4K byte boundary. This does not mean that both sockets have to be populated. When assigning 2K devices to processor cells bit 4 must be set.

#### 4.2.2 Handling 4K Devices

4K devices are handled easily. Any socket can be assigned to any processor cell. Bit 4 must be cleared.

#### 4.2.3 Handling 8K Devices

The DSTD-503 handles 8K devices by writing the same socket number into two cells. The cells are usually adjacent and located on an 8K boundary. This is not mandatory but very few applications would require other configurations. The only restriction is that the lower 4K bytes of an 8K device will respond to even numbered cells and the upper 4K bytes will respond to only odd numbered cells. Bit 4 must be cleared.

#### 4.2.4 Handling 16K Devices

The DSTD-503 handles 16K devices by writing the same socket number into four cells. The cells are usually adjacent and located on a 16K boundary. This is not mandatory but very few applications would require other configurations. The restriction is the same as for 8K devices and also the lower 8K bytes of a 16K device will respond to only even numbered 8K cells and the upper 8K bytes will respond to only odd numbered 8K cells. Bit 4 must be cleared.

## 5.0 SPECIFICATIONS

### 5.1 Electrical Specifications

#### 5.1.1 STD Bus Interface

Bus Inputs: One 74LS load max.

Bus outputs:  $I_{OL} = 24 \text{ mA min. @ } V_{OL} = 0.5 \text{ Volts}$   
 $I_{OH} = 15 \text{ mA min. @ } V^{OH} = 2.4 \text{ Volts}$

#### 5.1.2 Operating Temperature

0 Degrees C to 50 Degrees C  
95% humidity non-condensing

#### 5.1.3 Power Supply Requirements

+5V +/- 5% @ .5A without memory devices

### 5.2 Mechanical Specifications

#### 5.2.1 Card Dimensions

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm) long

0.48 in. (1.22 cm.) maximum height

0.062 in. (0.16 cm.) printed circuit board thickness

#### 5.2.2 STD Bus Edge Connector

56 pin Dual Readout; 0.125 in. centers

##### Mating Connector

Viking 3VH28/1CE5 (printed circuit)

Viking 3VH28/1CND5 (wire wrap)

Viking 3VH28/1CN5 (solder lug)

## SECTION 6

### 6.0

### FACTORY NOTICES

#### 6.1

#### Factory Repair Service

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. **THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL.** Enclose a letter containing the following information with the returned circuit board:

Name, address and phone number of purchaser  
Date and place of purchase  
Brief description of the difficulty

Mail a copy of this letter **SEPARATELY** to:

dy-4 SYSTEMS INC.,  
888 Lady Ellen Place,  
Ottawa, Ontario  
K1Z 5M1, Canada

Securely package and mail the circuit board, prepaid and insured, to the same address.

#### 6.2

#### Limited Warranty

Dy-4 warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

### NOTICE

The antistatic bag is provided for shipment of the dy-4 PC boards to prevent damage to the components due to electrostatic discharge.

Failure to use this bag in shipment will **VOID** the warranty.

**APPENDIX A**  
**OPTION JUMPER SUMMARY**

**APPENDIX A**  
**OPTION JUMPER SUMMARY**

**A.1 Jumper Blocks**

The DSTD-503 has the following jumpers:

JB1-JB12 Memory Socket Configuration Blocks.

JB13 8088 STD BUS Address Selection.

JB14 8088 vs Z80 STD BUS Address Selection.

JB15 Memory Mapper Cell Size.

JB16 DMA Chain.

JB17 Card Port Address Selection.

**A.2 Memory Socket Configuration Blocks (JB1 - JB12)**

One jumper block is associated with each byte-wide memory socket.

JB1 - JB12

	A	B	C
1	o	o	o
2	o	o	o
3	o	o	o
4	o	o	o

A1 Memory Socket Pin 21 - A10/L  
A2 Memory Socket Pin 27 - WE/H  
A3 STD Address A13  
A4 GND  
B1 Memory Socket Pin 23 - WE/A11  
B2 STD Write Line  
B3 Memory Socket Pin 26 -VCC/A13  
B4 Memory Socket Pin 1 - +5/RDY  
C1 +5 Volts  
C2 STD Address A11  
C3 STD Address A10  
C4 STD Read Line



### A.3 8088 STD BUS Address Selection (JB13)

This jumper block determines the card page address in 8088 STD BUS mode.

	1	2	3	4
C	o	o	o	o
B	o	o	o	o
A	o	o	o	o

A1 to A4 Logic '0'

C1 to C4 Logic '1'

B1	Address Bit 16
B2	Address Bit 17
B3	Address Bit 18
B4	Address Bit 19

### A.4 8088 vs Z80 STD BUS Address Selection (JB14)

This jumper block selects either the 8088 page address (via JB13) or memory mapper 2K/4K select bit in Z80 mode.

1	o	
		Z80
2	o	
		8088
3	o	

### A.5 Memory Mapper Cell Size (JB15)

This jumper block sets the cell size of the memory mapper to either 8K or 4K bytes.

JB15		
1	o	
		4K
2	o	
		8K
3	o	

#### A.6 DMA Chain (JB16)

This jumper should be installed only when the card is used in a dy-4 SYSTEMS backplane.

1 o BUSAK (pin 40)

2 o BAO (pin 41)

#### A.7 Card Port Address Selection (JB17)

This jumper block sets the card's I/O address port.

	1	2	3	4	5	6	7	8
A	o	o	o	o	o	o	o	o
B	o	o	o	o	o	o	o	o

A1 to A8 Ground

B1	Address Bit	7
B2	Address Bit	6
B3	Address Bit	5
B4	Address Bit	4
B5	Address Bit	3
B6	Address Bit	2
B7	Address Bit	1
B8	Address Bit	0

**APPENDIX B**

**STD-Z80 BUS PIN OUT**

## APPENDIX B

### STD-Z80 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	Ground - System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	Address Bus (Tri-state, output, active high).
15	A7	
16	A15	
17	A6	
18	A14	

# STD-Z80 BUS PIN OUT

19	A5	A0-A15 make up a 16-bit address bus. The address bus provides the address for memory (up to 65k bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Memory Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Memory Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-State output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 Systems DSTD.

# STD-Z80 BUS PIN OUT

36	/MEMEX	Memory expansion, not used on dy-4 Systems DSTD cards.
37	/REFRESH	/REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic zero and the upper 8 bits of the address bus contains the I register.
38	/DEBUG	/DEBUG (Input) used in conjunction with DDT-80 operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the /DEBUG line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
39	/M1	Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the opcode fetch cycle of an instruction. Note that during the execution of a 2-byte opcodes, /M1 will be generated as each opcode is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
40	STATUS 0	DMA priority chain input.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

## STD-Z80 BUS PIN OUT

- 42        /BUSRQ        Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.
- 43        /INTAK        Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.
- 44        /INTRQ        Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.
- 45        /WAITRQ        WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

46	/NMIRQ	Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will over-ride a /NMIRQ.
47	/SYSRESET	System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H and set Interrupt Mode 0.
48	/PBRESET	Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset.
49	/CLOCK	Processor Clock (Output, active low). Single phase system clock.
50	CNTRL	Auxiliary Timing
51	PCO	Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.



## STD-Z80 BUS PIN OUT

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

### NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.

APPENDIX C  
PARTS LIST

APPENDIX C  
DSTD-503 PARTS LIST

DY00489

QTY	DESIGNATION	PART NUMBER
INTEGRATED CIRCUITS		
1	U18	74LS74
1	U14	74LS85
1	U23	PAL16L8
4	U21,22,20,25	74LS245
1	U24	74LS682
1	U19	74LS240
2	U16,17	74S138
2	U13,15	74S189A
RESISTORS		
4	RN1,2,3,4	4608X-2-470
1	R1	CF25-511
2	R3,4	CF25-470
1	R2	CF25-472
CAPACITORS		
23	C1-16,18-24	8121-050-Z50-104M
1	C17	TAG10M25
SOCKETS		
12	at U1-12	640362-3
1	at U23	640464-3
JUMPER BLOCKS		
1	JB16	CHS6902-W1S
2	JB14,15	CHS6903-W1S
13	JB1-12,13	CHS6904-W1S
13	JB1-13	CHD6904-W1S
1	JB17	CHD6908-W1S

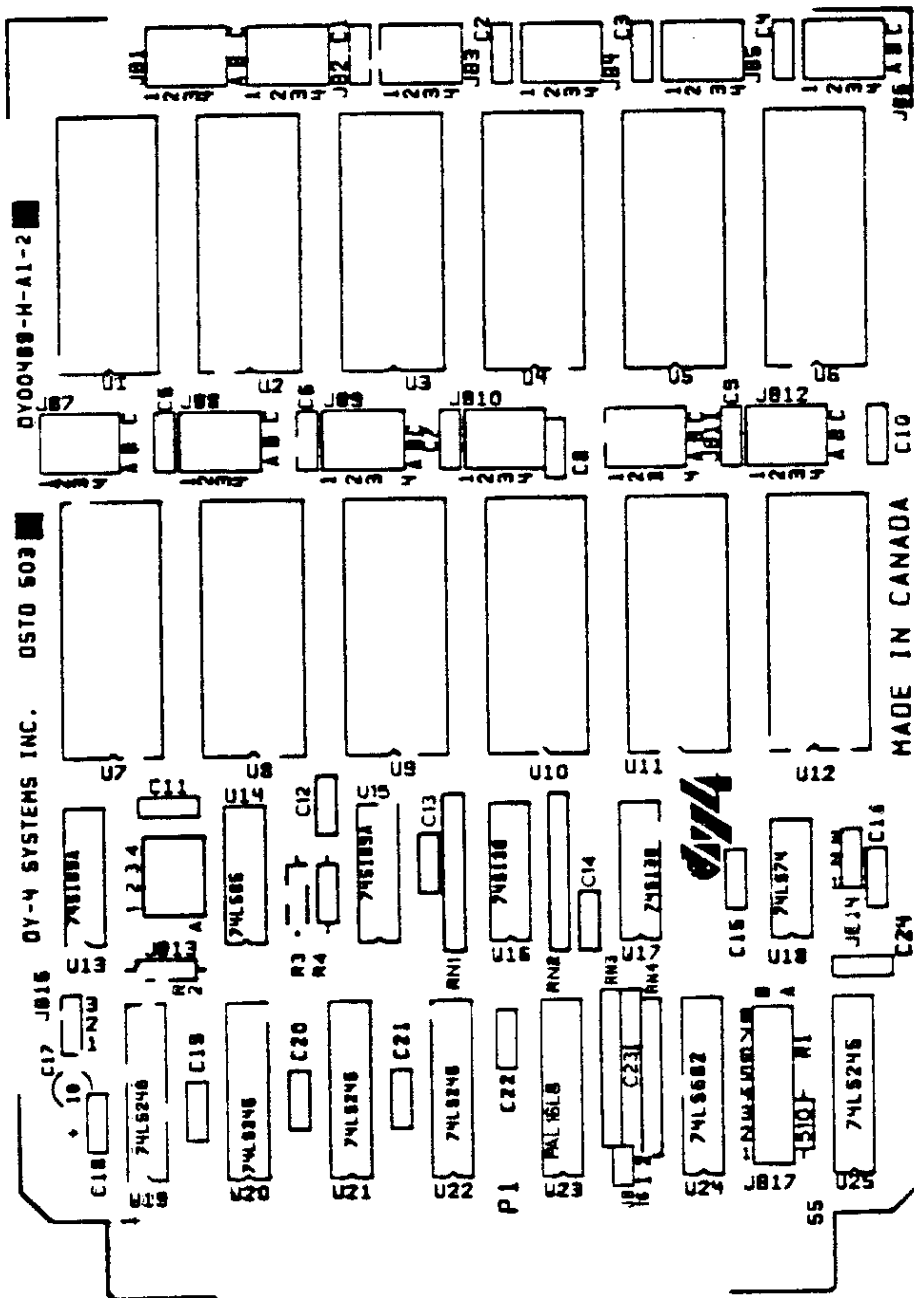


FIGURE C-1 DSTD-503 SILK SCREEN

**APPENDIX D**  
**SCHEMATIC**

A

B

C

D

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31	4	40000-0-000	RESISTOR NETWORK 8-PIN D.I.P. 47 ohm	RN1,2,3,4
30				
29	1	CF25-001	RESISTOR, FIXED COMP. 510 ohm 1/4W 5%	R1
28	2	CF25-070	" " " 47 ohm " " "	R3,4
27	1	CF25-072	RESISTOR, FIXED COMP. 4.7 K 1/4W 5%	R2
26				
25	1	CH00002-W10	CONNECTOR (1x2 STRAIGHT HEADER)	J016
24	2	CH00003-W10	1x3	J014,15
23	13	CH00004-W10	1x4	J01 - 12,13
22				
21	13	CH00004-W10	2x4	J01 - 13
20	1	CH00006-W10	CONNECTOR (2x8 STRAIGHT HEADER)	J017
19				
18	23	0K21-000-230-104M	CAPACITOR CERAMIC .1uF 50V (E96E)	C1 - 10,18-24
17	1	TAN000025	CAPACITOR TANTALUM 10uF 25V (LXX)	C17
16				
15	1	74LS74	INTEGRATED CIRCUIT	U10
14	1	74LS95		U14
13	1	74LS16LS		U23
12	4	74LS246		U21,22,20,25
11	1	74LS002		U24
10				
9	1	74LS246		U10
8	2	74LS130		U16,17
7	2	74LS009A		U13,15
6			INTEGRATED CIRCUIT	U1 - 12
5				
4	12	640062-3	SOCKET 28-PIN D.I.P.	@ U1 - 12
3	1	640064-3	SOCKET 20-PIN D.I.P.	@ U23
2				
1	1		PRINTED CIRCUIT BOARD	
ITEM	QTY	PART NUMBER	DESCRIPTION	DESIGNATION

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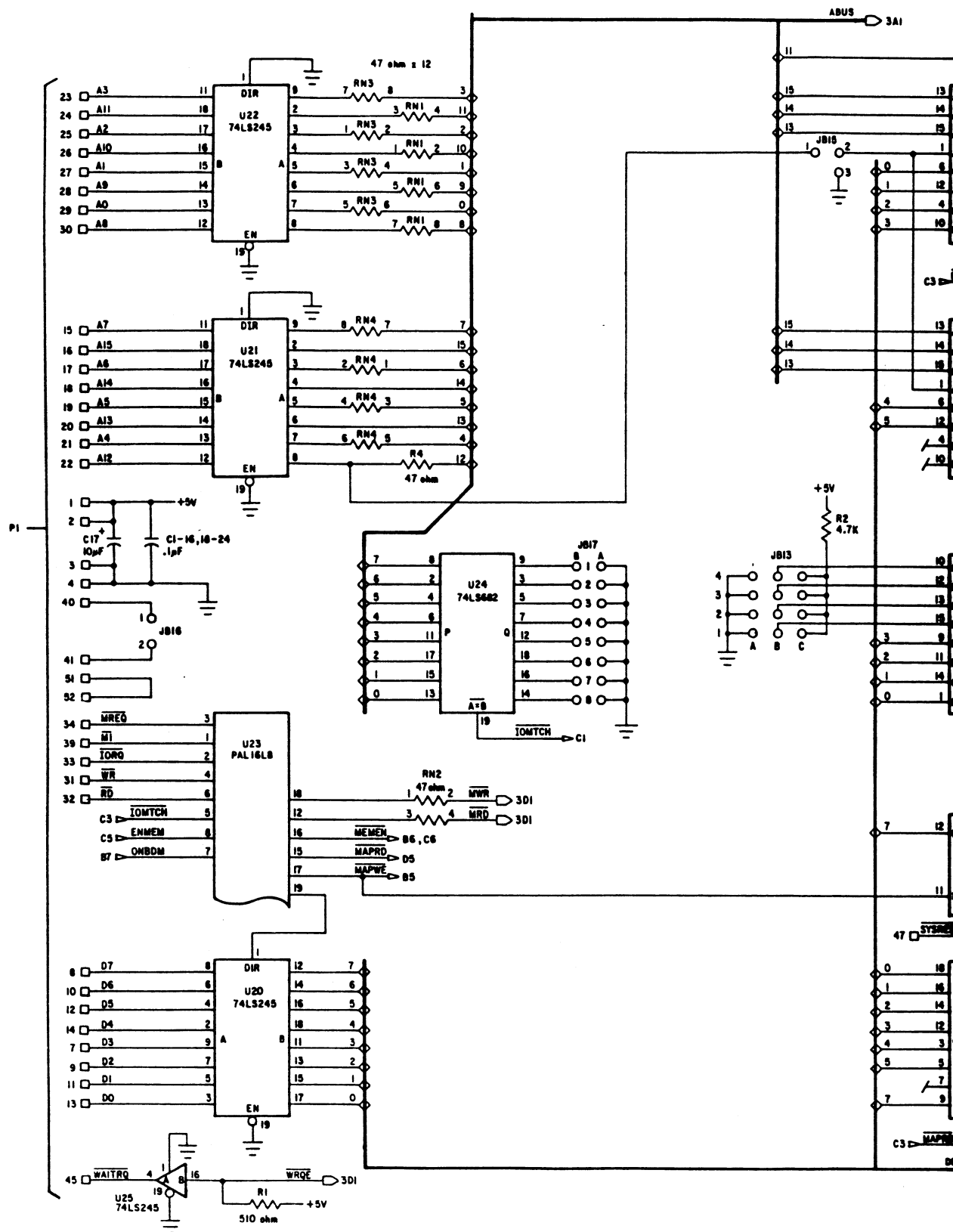


A

B

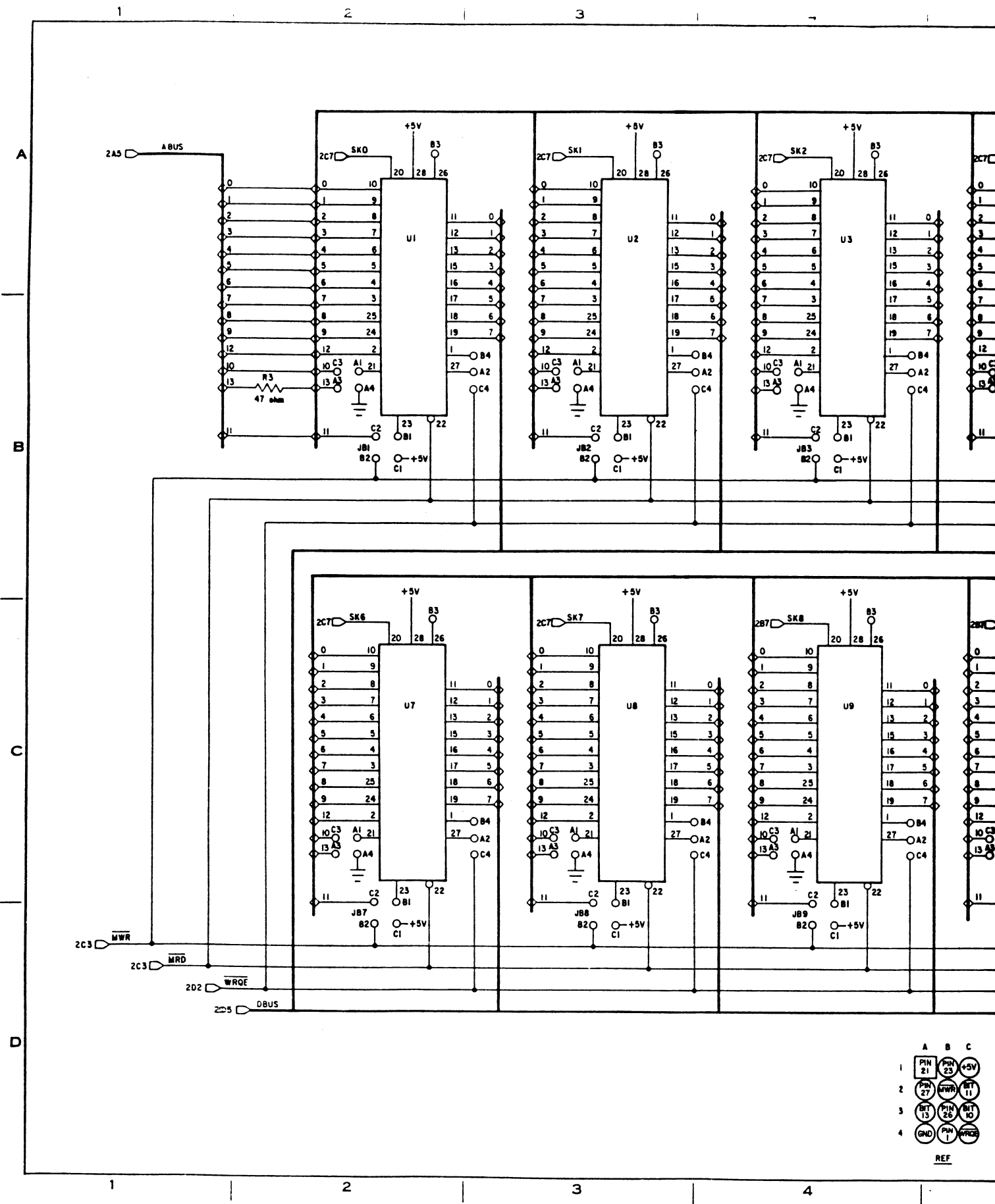
C

D





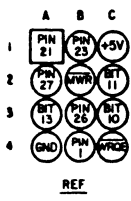
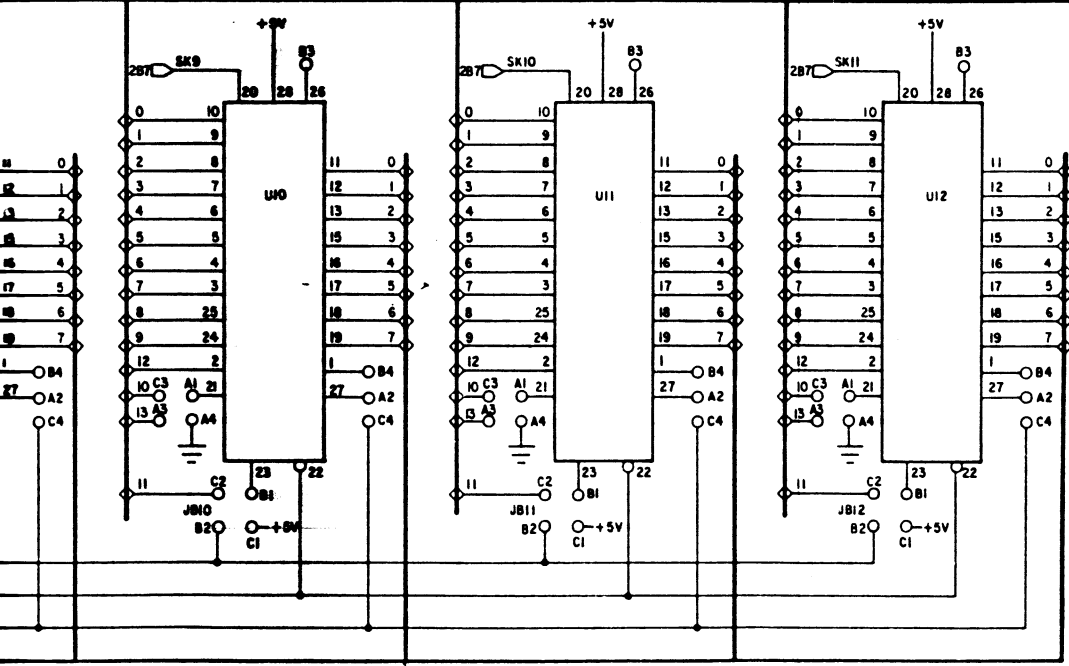
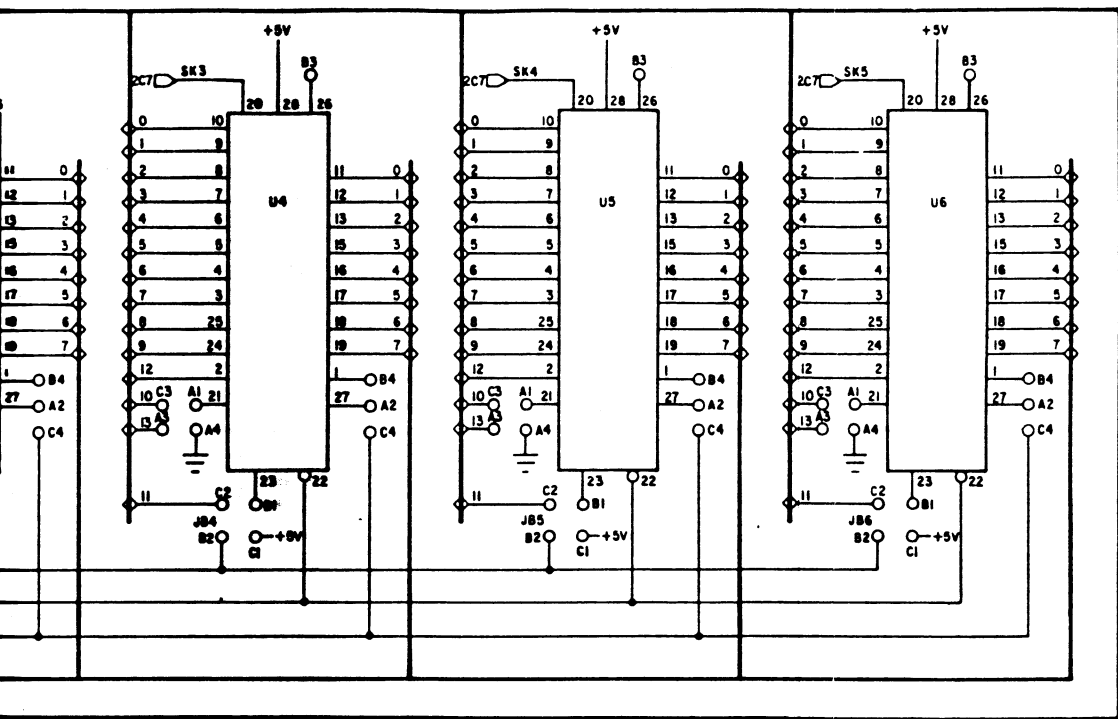




	A	B	C
1	PN 21	PN 23	+5V
2	PN 27	MRD	BT 11
3	BT 13	PN 26	BT 10
4	GND	PN 1	WRQE

REF

7		8		
ISSUE	DESCRIPTION	DATE	DRN	CHK



SCALE	DRN Kohler	CHK	DATE
APP'D	TOL	MAT'L	FINISH
TITLE DSTD-503 BYTE WIDE MEMORY CARD			
DWG NO. DY00489-1-A3-2	ISS 2	SH 3 OF	