

DSTD-703

MULTI FUNCTIONAL CALENDAR/CLOCK CARD

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SECTION 1

1.0 GENERAL INFORMATION**1.1 Introduction**

The DSTD-703 provides a Real Time Calendar Clock, two fully buffered 8 bit parallel ports and a 4 channel Counter/Timer.

These are also provisions for 4 byte-wide sockets which may be placed anywhere in the processor memory space Modulo 8K.

Full Z80 mode 2 interrupts are supported by the DSTD-703.

The Brown-out detector causes a "System Reset" when +5 volt rail dips below 4.7Volts. This ensures that the computer system does not latch up in an unknown state due to momentary power dips.

1.2 DSTD Series General Description

The DSTD was designed to satisfy the need for low cost OEM microcomputer modules. The DSTD-Z80 BUS uses a motherboard interconnect system concept. The modules for the STD-Z80 BUS are a compact 4.5 x 6.5 inches which provides for system partitioning by function, e.g. CPU, Memory, I/O, etc. This smaller module size makes system packaging easier, while increasing MOS-LSI densities provide high functionality per module.

1.3 DSTD-703 Features

- Calendar/Clock with MONTH, DAY of month, DAY of week, HR, MIN, SEC, 1/100 SEC, 1/10000 SEC,
- 56 bits of battery-back up RAM available on the clock chip
- Ni-Cad battery backup @ 200 mAHr configurable for external battery
- 4 independent programmable interval timers/counters
- Daisy-chain Interrupt capability
- Brown-out detector
- 4-28 pin sockets for byte-wide ROM/EPROM and RAM
- byte-wide memory may be enabled/disabled under software control
- 16 pin Bi-directional parallel port with interrupt capability. This can drive the DSTD-ACC-RDSM directly for a

GENERAL INFORMATION

DSTD-703

date/time display

- STD BUS compatible board

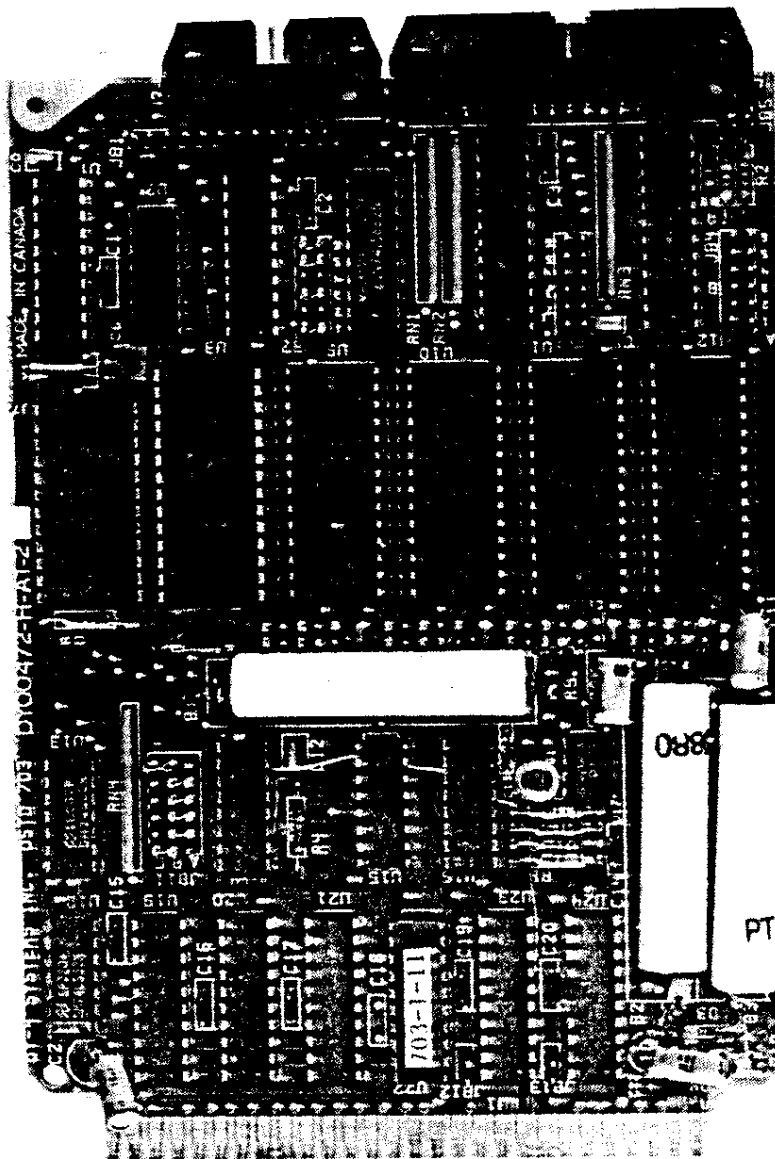


FIGURE 1-1 DSTD-703 MODULE

SECTION 2

2.0 FUNCTIONAL HARDWARE DESCRIPTION**2.1 Introduction**

The DSTD-703 contains a crystal controlled MM58167A Calendar/Clock chip to provide the date time function. With software support, this card can easily drive an external 7 segment LED display card (DSTD-ACC-RDSM) for a date and time display.

The fully charged Ni-Cad battery will run the Calendar/ Clock for over one year without need for recharge.

The programmable interrupt timer is implemented with a Z80-CTC. It may be connected to user devices via a 10 pin connector for Interrupt or counter capabilities.

The 16 bit parallel port is general purpose. A 26 pin connector is provided for interface purposes.

The Brown-out detector causes a "System Reset" when +5 volt rail dips below 4.7V. This ensures that the computer system does not latch up in an unknown state due to momentary power dips.

2.2 Block Diagram Description

The block diagram of the DSTD-703, Figure 2-1, illustrates the flow of system address, data and control signals. The following paragraphs describe the function of each of the major blocks.

2.2.1 STD BUS Interface

The STD BUS Interface consists of an assortment of circuitry which gates various bus control signals including interrupt requests, daisy-chained priority In/Out, Clock, system reset, M1, IORQ, read and interrupt acknowledge between the BUS and the on-board peripheral chips. The STD BUS Interface also includes address buffers, bi-directional data bus transceivers and I/O port address decoder with associated jumper block for I/O address programming by the user.

2.2.2 Memory Decode Logic

This section consists of a 74LS85 and PAL. The 74LS85 configures the base memory address and memory address range for the DSTD-703. The PAL decodes the 5 high order memory addresses and generates the appropriate chip selects when the DSTD-703 memory is accessed. The PAL provides for two types of memory decoding.

The first assumes 2K devices in the memory sockets. The second is user definable. (see Section 3 for further details)

2.2.3 Memory

The DSTD-703 has been designed to accomodate any combination of the byte-wide RAM, ROM, and EPROM devices. Four 28-pin sockets have been provided, each of which may be strapped for any of the allowable memory types. These user-selectable options are fully described in Section 3.

2.2.4 I/O Decode Logic

This section consists of a 74LS682, a 74LS139 and some SSI gates. It provides the chip select for the CTC and read and write strobes for the parallel port and (RTC) Real Time Clock.

2.2.5 Counter/Timer Controller

The Counter/Timer Controller (MK3882/Z80-CTC) provides four independent, programmable channels for either software or hardware controlled counting and timing functions. Each channel can be configured by the CPU for various modes of operation and the built-in daisy-chain priority interrupt logic provides for automatic, independent interrupt vectoring.

The Trigger inputs and Zero Count outputs are buffered and brought out to a connector for external hardware control. A strapping option has also been included to permit any or all of the four CTC channels to be cascaded for long count sequences.

Section 3 provides the necessary information for utilizing this option. For a complete description of CTC operation, refer to the Mostek MK3882 or Zilog Z80-CTC Technical Manual or Appendix A-11 of this manual.

2.2.6 Parallel Ports

The DSTD-703 has two parallel ports. These ports are implemented using octal transceiver chips. The jumper blocks associated with the ports are used to "program" the transceivers for appropriate operations. A data sheet for the 74LS646 is included in Appendix E of this manual.

2.2.7 Real Time Clock

The Real Time Clock is implemented using an MM58167A calendar/clock chip. It also provides 56 bits of battery backed up RAM. Addressses to the RTC chip are first latched by a 74LS174 before they are presented to the RTC. This method takes up only

two I/O addresses to communicate to the RTC, therefore freeing I/O addresses on the STD BUS.

2.2.8 Battery Back Up

Nickel-Cadmium batteries provide the battery back up function. The batteries will be charged continuously when power is applied to the DSTD-703.

2.2.9 Brown-Out Detector

This circuit detects when voltage drops below 4.7V, when this occurs a push button reset is generated. The software when reset, should check for a brown-out condition by reading bit 7 of I/O address base +1; the software then continues with the reset routine or goes into the brown-out routine.

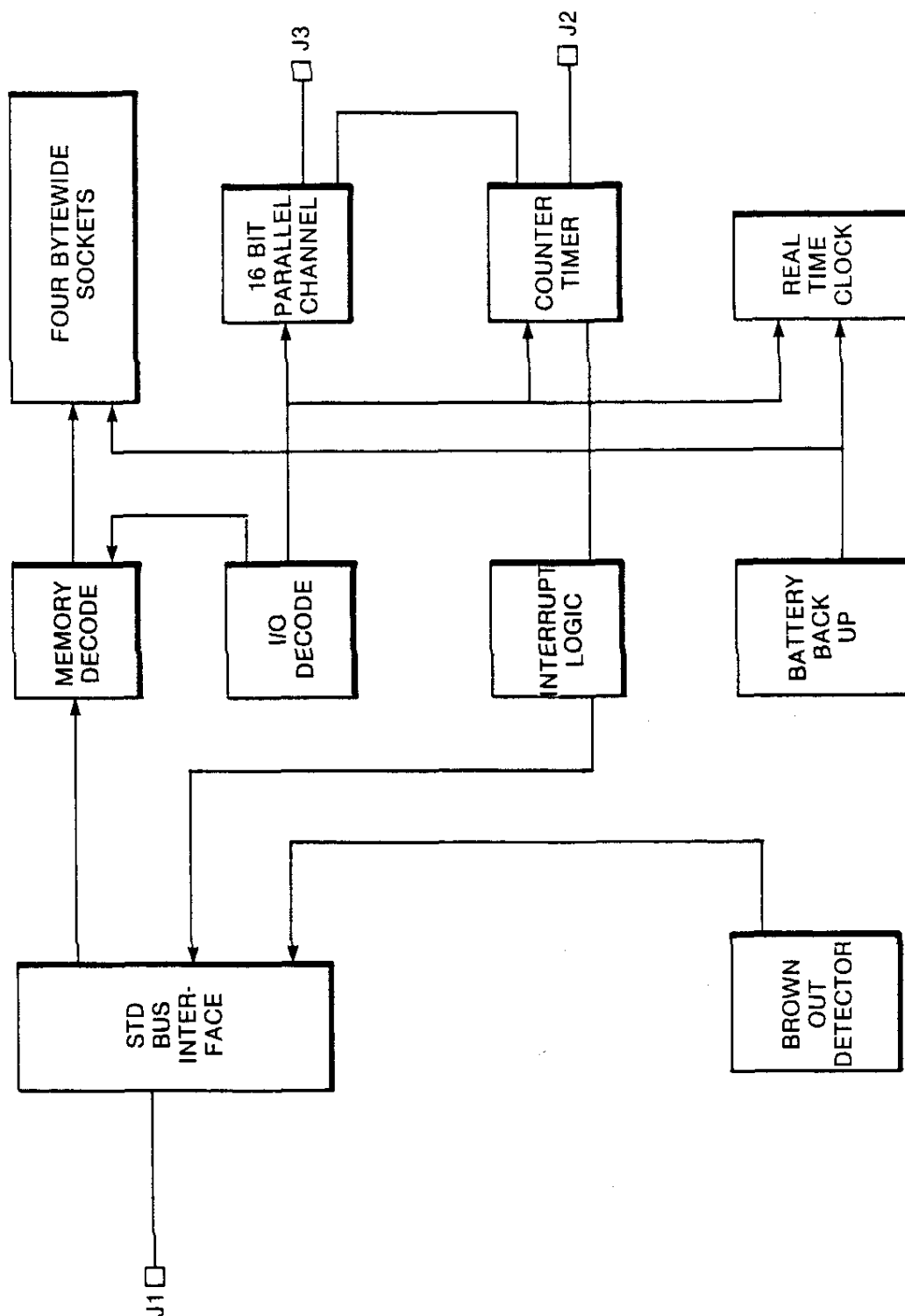
2.3 Z80 Interrupts

2.3.1 Interrupt Overview

Interrupt capability is provided to allow peripheral devices to suspend CPU operation in an orderly manner and force the Z80 processor to start executing a specific peripheral service routine. On completion of the service routine, the Z80 returns to the operation from which it was interrupted.

2.3.2 Priority Daisy-Chain

The CTC is a Z80 peripheral device and as such includes daisy-chained priority interrupt logic which automatically provides the programmed interrupt vector (from the highest priority interrupting device) to the processor during an interrupt acknowledge. Look-ahead priority logic has been designed to ensure that more than one peripheral card (from an interrupt speed standpoint) may be included in a larger interrupt priority loop. This is accomplished by providing both ends of the board daisy chain logic (PCI and PCO) at the edge card connector J1, so that the card priority within a several card priority daisy-chained system may be implemented. The "high" and "low" state of the PCI and PCO determines the card priority in the same fashion as for the individual peripheral chips.



DSTD-703 BLOCK DIAGRAM

2.4 I/O PORT DEFINITION SUMMARY

The I/O base address port is set at 50H by the factory. However this base address may be re-configured by the user.

The following table describes the port assignments and their use. The mnemonics used to represent the control functions of the individual bits are described at the end of the table.

TABLE 2 - 1
PORT ASSIGNMENTS AND DEFINITIONS

ADDR	ACCESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BASE									
+0	R/W								
									Real Time Clock Chip Data Port
+1	R/W			MEMEN	RTCA4	RTCA3	TRCA2	RTCA1	RTCA0
+1	R/O	BRNOT							
+2	R/W								Parallel Port 0 Data Port
+3	R/W								Parallel Port 1 Data Port
+4	R/W		CTC	CHNL 0					
+5	R/W		CTC	CHNL 1					
+6	R/W		CTC	CHNL 2					
+7	R/W		CTC	CHNL 3					

MEMEN: memory enable : is set High to enable on-board memory

RTCA4-0: RTC Address 4-0: is used to select the address for the Real Time Clock Chip.

BRNOT: Brown Out: is low when a brown out has occurred.

SECTION 3

3.0 USER SELECTABLE OPTIONS**3.1 Introduction**

The DSTD-703 incorporates many strapping options to provide the user with a high degree of flexibility in system configurations. This section describes the use of the switch jumper option.

3.2 Counter/Timer Configuration (JB1)

The four Counter/Timer channels may be cascaded for extended counting and timing functions. Table 3-1 shows the jumper pin numbers and the edge connector numbers for the CTC. Refer to the MK3882 Technical Manual or the Zilog Data Book for a complete description of CTC operation or Appendix A-11 of this manual.

TABLE 3 - 1**CTC CONNECTOR PIN ASSIGNMENT**

SIGNAL		JUMPER BLOCK EDGE CONNECTOR	
NAME		JB1	J2
C/T0	I	2	1
ZC0	0	3	2
C/T1	I	4	3
ZC1	0	5	4
C/T2	I	6	5
ZC2	0	7	6
C/T3	I	8	7
CLKP0		9	
CLKP1		10	
POINTR		11	
P1INTR		12	
RTCINTR		13	

The CTC may also be used to generate interrupts on status changes during parallel I/O transfers. This will be discussed in more detail in the following sections.

3.3 I/O Base Address Select (JB2)

The DSTD-703 occupies 8 contiguous I/O addresses. Its position in the I/O address space is determined by JB2 connections. Table 3-2 shows the jumper block pin numbers and the corresponding processor address bits used in the comparison. Installing a jumper implies a logic '0'. No jumper implies a logic '1'.

Examples:

- 1) Base address B8H requires jumpers between pins 2A & 2B and 6A & 6B
- 2) Base address 50H requires jumpers between pins 1A & 1B, 3A & 3B, 5A & 5B and 6A & 6B

The board is shipped from the factory wired for address 50H.

Table 3 - 3 illustrates the function of each of the 8 individual I/O Ports assigned to the DSTD-703.

TABLE 3 - 2
JB2 PORT ADDRESS PIN ASSIGNMENTS

PIN	ADDRESS BIT
1	A7
2	A6
3	A5
4	A4
5	A3
6	IORQ This jumper must always be installed

Logic '0' - Jumper installed

Logic '1' - No Jumper

TABLE 3 - 3
I/O PORT CONFIGURATION

Port Address								Port Function	
A7	A6	A5	A4	A3	A2	A1	A0		
X	X	X	X	X	0	0	0	RTC	- Data
X	X	X	X	X	0	0	0	RTC	- Control
X	X	X	X	X	0	1	0	Port 0	-
X	X	X	X	X	0	1	1	Port 1	-
X	X	X	X	X	1	0	0	CTC	- Chan 0
X	X	X	X	X	1	0	1	CTC	- Chan 1
X	X	X	X	X	1	1	0	CTC	- Chan 2
X	X	X	X	X	1	1	1	CTC	- Chan 3

Refer to Table 2-1 for the data bit definitions.

3.4 Parallel Ports (JB3, JB4)

The DSTD-703 has two independent 8-bit parallel ports. These ports are implemented using the 74LS646 to 74LS649 series of integrated circuits. They are octal transceivers with latches. Table 3 - 4 lists the basic functions of these chips. (Refer to Appendix E).

TABLE 3 - 4
I/O PORT DEVICE SELECTION OPTIONS

	DATA PATH	OUTPUT
74LS646	TRUE	3 - State
74LS647	TRUE	Open Collector
74LS648	INVERTING	3 State
74LS649	INVERTING	Open Collector

Note: When using open collector devices, Resister Network RN4 must be used.

Both parallel ports are accessed through one connector J3. Table 3 - 5 shows the pinouts for the connector.

TABLE 3 - 5
PORT CONNECTOR PIN ASSIGNMENT

PORT SIGNAL	PORT A	PORT B
Data 0	1	11
Data 1	2	12
Data 2	3	13
Data 3	4	14
Data 4	5	15
Data 5	6	16
Data 6	7	17
Data 7	8	18
CLKP	9	19
CONTROL	10	20
GND	24,25,26	
+5V	21,22,23	

3.4.1 Modes of Operation

Each parallel port has six basic modes of operation. Those modes represent the most common configurations.

- 1) Latch Input Mode
- 2) Transparent Input Mode
- 3) Latch Output Mode
- 4) Transparent Output Mode
- 5) Latched Bi-directional Mode
- 6) Transparent Bi-directional Mode

Note that latched bi-directional mode typically uses both ports. Table 3 - 7 summarizes some of the port configurations discussed in the following section.

3.4.2 Latch Input

In this mode data is clocked into the port register by an external device using the "CLKP" signal. Data is clocked on rising edge of "CLKP". In some applications it is necessary to inform the processor that valid or new data is available. This can be accomplished using the CTC.

Connect the "CLKP" signal to a channel on the counter/timer. The "CLKP" signal for port A is pin 9 and for port B is pin 10 on the CTC jumper block JB1. This pin can be connected to a free CTC channel (CH 0 / JB1-2; CH 1 / JB1 -4; CH 2 / JB1 -6; CH 3 / JB1-8). The CTC channel is then used in the counter mode to report positive transitions of the "CLKP" signal.

3.4.3 Transparent Input Mode

In this mode the data is read directly from the port. This mode is typically used for scanning switches or other relatively static information - or when there is no clock available. Again the control signal, with the CTC may be used to indicate "valid data" as discussed in Section 3.5.2.

3.4.4 Latched Output

In this mode the processor writes data into the port. The CONTROL signal may be used in one of several ways. First, it may be used by the external device to enable the port. The CONTROL signal is connected to the ENABLE input of the port register. (Connect pins A2 and B2 on the appropriate port jumper block). Second, the control signal can be used as a strobe in the external device to indicate valid data. (Note that in latched output mode it cannot be used to clock data into the external device-use transparent output mode if this function is required). To use the CONTROL signal as a strobe connect pins A2 and A1 on the port jumper block. Third, the CONTROL signal may be connected to a channel of the CTC and used by the external device to inform the processor that it is ready for new data. The strapping options allow many other handshake arrangements including combinations of the above.

3.4.5 Transparent Output

This mode is used when strobing data into an external device. The CONTROL signal is connected to the write port line (pins A2 and A1 of the port jumper block). In this mode the port acts simply as a buffer. Data is clocked on the rising edge of the CONTROL signal.

3.4.6 Latched Bi-directional Mode

This mode typically requires the use of both ports. Port A for the OUT direction and Port B for the IN direction. The ports are connected together in the edge connector (J3). The external device controls the direction of the data flow on the bi-directional bus. The external device clocks data in the B port using CLKP.

CLKPB can be connected in the CTC to provide an indication to the processor that new valid data is available from the external

device. The /RDPB signal is connected to the CONTROL B signal to inform the external device when the processor has read the data from the port. The processor outputs data to the external device by writing it to Port A. /WRPA is connected to CLKPA (JB3-B6 to JB3-A1). This is used to inform the external device that new data is available from the processor. The external device enables the data onto the bus using the CONTROLA line. The CONTROLA line can be connected to a CTC channel to let the processor know when the external device has taken the data.

3.4.7 Transparent Bi-directional Mode

This mode provides simple bi-directional capability. The port is enabled at all times and the direction is controlled by the RDPA signal; i.e., the direction is out unless the processor is "reading" the port. The /RDPA is also connected to the control signal to enable the drivers in the external device. The CLKPA line can be either connected to the CTC or to the /WRDA signal to provide handshake signals in the desired direction. Other configurations are possible. For example the out data can be latched instead of transparent.

Jumper blocks JB3 and JB4 are used to configure Port A and Port B respectively. Table 3 - 7 shows connector pinouts for both ports (J3).

Port A has the I/O address 52H and Port B has 53H.

Table 3 - 6 describes the Jumper Block pin functions.

TABLE 3 - 6

JUMPER BLOCK (JB3 AND JB4) PIN ASSSIGNMENT

PIN	NAME	FUNCTION
B1	RDP (A/B)	Read port signal from the processor- usually connected to the ENABLE or DIRECTION pins.
A1	WRP (A/B)	Write port signal from the processor- usually connected to the CONTROL signal for handshake purposes.
B2	ENABLE (A/B)	Port chip enable - when low, enables the port.
A2	CONTROL (A/B)	General purpose signal - for connecting- to external device to CTC or ENABLE.
B3	SEL AB	When low, the "out" direction is transparent. When high, the "out"

direction is latched - strobed by WRP (A/B).

A3,A4	GND	Used for option selection.
B4	SEL BA	When low, the "in" direction is transparent. When high, the "in" direction is latched - strobed by CLKP (A/B)>
B5	DIRECTION	Controls the direction of the port when enabled - low is in, high is out.
A5,A6	+5V	
B6	CLKP (A/B)	External strobe for clocking data into the port.

TABLE 3 - 7

SAMPLE PORT CONFIGURATION

MODE	JB6 AND/OR JB9 JUMPER CONNECTION		FUNCTION
Latched Input	A4-B5 B1-B2 B4-A5		Direction in port enable latched mode.
Transparent Input	A4-B5 B1-B2 B4-A4		Direction in Port enable Transparent.
Latched Output	B5-A5 B2-A3 or (B2-A2) or (A1-A2) B3-A5		Direction out Enable on When external device controls enable Strobe for external device Latched Mode
Transparent Output	B5-A5 B2-A3 A1-A2 B3-A3		Direction out enable on write strobe for external device transparent mode
Latched Bi-directional	Port A	Port B	
	B5-A5	A4-B5	Direction
	(JB3-B6/JB3-A1)	B1-A2	Handshake
	B2-A2		Out enable
	(JB1-11/JB1-8)		Handshake
		(JB1-10/JB1-6)	Handshake
		B1-A2	In enable
Transparent Bi-directional		B1-B5 B2-A3 B1-A2	Direction Port enable Handshake

3.5 5V Only Charge Option (JB5)

When 12 volts is not available to the DSTD-703, install JB5 for proper battery charging operation.

3.6 Byte-wide Memory Socket Configuration (JB6,JB7,JB8,JB9)

The DSTD-703 incorporates four 28-pin sockets which can be independently configured to accept a variety of pin compatible memory devices. Table 3 - 8 lists each socket, its corresponding jumper block, and its address space for the standard configuration. Table 3 - 9 illustrates the necessary jumper connections for configuring a socket to accept a particular memory device.

The DSTD-703 is shipped from the factory with a memory decoding PAL (U22) which supports 2K byte chips. The factory can supply memory decoding PAL's on request for other standard configurations using 4K byte and 8K byte chips. Consult the factory for PAL programming details for non-standard requirements.

The base address of memory is selected by the user. (see Section 3 - 7)

TABLE 3 - 8

MEMORY SOCKET/JUMPER BLOCK ASSIGNMENT

SOCKET	ADDRESS	JUMPER BLOCK
U9	base + 0000 to 07FF	JB6
U10	base + 0800 to 0FFF	JB7
U11	base + 1000 to 17FF	JB8
U12	base + 1800 to 1FFF	JB9

Table 3 - 9 shows the straps necessary to configure the sockets for the different memory types. All the sockets are wired independently, allowing any mix of chips within the addressing constraints.

TABLE 3 - 9
MEMORY SOCKET CONFIGURATION

MEMORY	JUMPER CONNECTIONS
2758	1 - 3 4 - 6 OPEN 2,7,5
2759	1 - 4 4 - 6 OPEN 2,7,3,5
2716	1A - 1B 3A - 4A 5B - 4A
2732	1A - 1B 3A - 2A 5B - 4A
2764	1A - 1B 3A - 2A 5B - 4A
4118 4801	1B - 2B 3A - 3B 5B - 4A
4802	1B - 1A 3A - 3B 5B - 4A

JUMPER BLOCK LAYOUT FOR J6, J7, J8, J9.

	A	B
1	o	o
2	o	o
3	o	o
4	o	o

3.7 On Board Battery Select (JB10)

The DSTD-703 allows the user to select between on-board battery or an external battery. The on-board battery is selected by installing a jumper at JB10. The external battery is selected by connecting the positive side of the battery to external connector J2 pin 8 and the negative side to J2 pin 10.

3.8 Memory Base Address Select (JB11)

The board's position in the processor's memory address space is selected by using hardwired jumpers. The board can be selected to occupy an 8K, 16K or 32K range of address by JB11. JB11 also configures the base address of the card to any 8K, 16K or 32K boundary.

TABLE 3 - 10**MEMORY RANGE SELECT**

32K	install	2B-2A;	4B-4C;	5B-5C;	3B-3C;	6B-6C
16K	install	2B-2A;	4B-4A;	5B-5C;	6B-6C	
8K	install	2B-2A;	4B-4A;	5B-5A		

TABLE 3 - 11**MEMORY BASE ADDRESS SELECT****32K Range**

Base at 0000H:	install	1B - 1A
8000H:	install	1B - 1C

16K Range

Base at 0000H:	install	1B - 1A;	3B - 3A
4000H:	install	1B - 1A;	3B - 3C
8000H:	install	1B - 1C;	3B - 3A
C000H:	install	1B - 1C;	3B - 3C

8K Range

Base at 0000H:	install	1B - 1A;	3B - 1A;	6B - 6A
2000H:	install	1B - 1A;	3B - 1A;	6B - 6C
4000H:	install	1B - 1A;	3B - 1C;	6B - 6A
6000H:	install	1B - 1A;	3B - 1C;	6B - 6C
8000H:	install	1B - 1C;	3B - 1A;	6B - 6A
A000H:	install	1B - 1C;	3B - 1A;	6B - 6C
C000H:	install	1B - 1C;	3B - 1C;	6B - 6A
E000H:	install	1B - 1C;	3B - 1C;	6B - 6C

3.9 Memory Option Configuration (JB12)

This Jumper Block is available as a user defined function. It is an input to the memory decoder and may be used to select a non-standard user defined memory map.

3.10 DMA Chain Enable (JB13)

This Jumper Block is used only when a dy-4 SYSTEMS INC. backplane is used. It provides a path through this card for the DMA chain.

SECTION 4

4.0 SPECIFICATIONS

4.1 Functional Specifications

4.1.1 Word Size

Data	8 bits
I/O Addressing	8 bits

4.1.2 Cycle Time

	Min	Max
DSTD-703 - 2.5	250kHz	2.5MHz
DSTD-703 - 4.0	250kHz	4.0MHz

4.1.3 I/O Port Addressing

The DSTD-703 occupies 8 contiguous I/O addresses. The base address is user selectable by JB2 (see Section 3.2). Two I/O addresses are used for the Real Time Clock (RTC) chip and memory enable port; two for the two 8 bit parallel port and four for the CTC.

4.1.4 Real Time Clock

The RTC occupies two I/O addresses on the DSTD-703.

At base + 0 is the data port
 base + 1 is the address latch that controls the address codes to the RTC chip.

The appendix contains a data sheet for the RTC chip.

Example for reading time. HH/MM/SS

```
LD    A,2 ;
OUT   (51H),A ; select counter-seconds
IN    A,(50H) ; read seconds from RTC chip
LD    (SEC),A ; store in location (SEC)
LD    A,3
OUT   (51H),A ; select counter-minutes
IN    A,(50H) ; read minutes
LD    (MIN),A ; store in location (MIN)
LD    A,4
OUT   (61H),A ; select counter-hours
IN    A,(50H) ; read hours
LD    (HRS),A ; store in location (HRS)
```

4.1.5 Memory Enable Bit

The memory enable bit is located at I/O address base +1 bit 5. Memory is enabled when this bit is set High, and disabled when it is set Low. This bit is set low by reset.

4.1.6 Eight Bit Parallel Ports

There are two general purpose 8 bit parallel ports on the DSTD-703. They may be configured to run in several modes (refer to Section 3.3). Port 0 is controlled via I/O address base +2 and Port 1 is controlled via I/O address base +3.

4.1.7 Counter/Timer

The counter/timer controller is located at I/O address base +4 through to base +7. Refer to Section 3.1 for configuration description.

4.1.8 Interrupts

The DSTD-703 supports vectored interrupt generation via the CTC chip. The interrupt vector is programmable upon initialization. Also the DSTD-703 supports full daisy chain interrupt priority.

4.2 Electrical Specifications

4.2.1 STD Bus Interface

Bus Inputs : one 74LS load max.
Bus Outputs: I_{OL} 24 mA min @ V_{OL} 0.5 Volts
 I_{OH} 15 mA min @ V_{OH} 2.4 Volts

4.2.2 Operating Temperature

0 degree Celsius to 60 degrees Celsius

4.2.3 Power Supply Requirements

+5VDC 5% @ 1.0 Amps Max
+12VDC 5% @ 0.02 Amps Max

4.3 Mechanical Specification

4.3.1 Card Dimensions

4.5 inches (11.43 cm.) wide by 6.50 inches (16.52 cm.) long
0.48 inches (1.22 cm.) maximum height
0.062 inches (0.16 cm.) printed circuit board thickness

4.3.2 STD Bus Edge Connector

56 Pin dual readout: 0.125 inch centers

4.3.2.1 Mating Bus Connector

Viking	3VH28/1CES	(PCB)
Viking	3VH28/1CND5	(Wire wrap)
Viking	3VH28/1CN5	(Solder lug)

4.3.3 Counter/Timer Connector

10 Pin Dual 0.100 inch grid

4.3.3.1 Mating Connector

Flat cable Ansley 609-100M or equivalent

4.3.4 Parallel Port Connector

1 - 26 Pin Dual 0.100 inch grid flat cable type male connector
(header)

4.3.4.1 Parallel Port Mating Connector

Ansley 609 - 2600M (flat cable) or equivalent

Winchester PGB26A - housing) For use with
Winchester 100-700COs - contacts) discrete wires

SECTION 5

5.0 FACTORY NOTICES**5.1 Factory Repair Service**

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. **THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL.** Enclose a letter containing the following information with the returned circuit board:

Name, address and phone number of purchaser
Date and place of purchase
Brief description of the difficulty

Mail a copy of this letter **SEPARATELY** to:

dy-4 SYSTEMS INC.,
888 Lady Ellen Place,
Ottawa, Ontario
K1Z 5M1, Canada

Securely package and mail the circuit board, prepaid and insured, to the same address.

5.2 Limited Warranty

dy-4 warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

NOTICE

The antistatic bag is provided for shipment of the dy-4 PC boards to prevent damage to the components due to electrostatic discharge.

Failure to use this bag in shipment will **VOID** the warranty.

APPENDIX A
OPTION JUMPER SUMMARY

APPENDIX A

OPTION JUMPER SUMMARY

A-1 The following is a summary of the DSTD-703 Option Jumper Blocks.

JB1	Counter/Timer Configuration Block.
JB2	I/O Base Address Select.
JB3,4	Parallel Ports.
JB5	5V Only Charge Option.
JB6,7,8,9	Memory Socket Configuration.
JB10	On Board Battery Select.
JB11	Memory Base Address Select.
JB12	Memory Option Configuration.
JB13	DMA Chain Enable.

A-2

Counter Timer Configuration (JB1)

JB1

- o RTC Interrupt
- o J2-1
- o J2-2
- o J2-3
- o J2-4
- o J2-5
- o J2-6
- o J2-7
- o J2-8
- o CLK P0
- o CLK P1
- o P1 Interrupt

A-3

I/O Base Address (JB2)

B	o	o	o	o	o	o
A	o	o	o	o	o	o
	1	2	3	4	5	6

B1 to B6		Ground
A1	Address Bit	7
A2	Address Bit	6
A3	Address Bit	5
A4	Address Bit	4
A5	Address Bit	3
A6	/IORQ	

A-4

Parallel Ports (JB3,4)

	1	2	3	4	5	6
B	o	o	o	o	o	o
A	o	o	o	o	o	o

A1	WRP 0/1	B1	RDP 0/1
A2	P(0/1) INTR	B2	G EN (74LS64X)
A3	GND	B3	SEL A/B (74LS64X)
A4	GND	B4	SEL B/A (74LS64X)
A5	+5V	B5	DIR (74LS64X)
A6	+5V	B6	CLP 0/1

A-5

+5V Battery Charge Option (JB5)

o Battery Feed

o +5V

A-6

Memory Socket Configuration (JB6,7,8,9)

		A	B	
Address Bit 10	1	o	o	Socket pin 21 (A10)
Address Bit 11	2	o	o	GND
Socket pin 23 (A11/WE/VPP)	3	o	o	Write Strobe
+5V	4	o	o	+5V
VBATT	5	o	o	Socket pin 26 (VCC)

A-7

On Board Battery Select (JB10)

JB10

Battery o o Battery Feed

A-8**Memory Base Address Select (JB11)**

	1	2	3	4	5	6	
JB11	C	o	o	o	o	o	o
	B	o	o	o	o	o	o
	A	o	o	o	o	o	o
	A1,3,6					GND	
	A2						Address Bit 15
	A4						Address Bit 14
	A5						Address Bit 13
	B1						Comparator Bit B3
	B2						Comparator Bit A3
	B3						Comparator Bit B2
	B4						Comparator Bit A2
	B5						Comparator Bit A1
	B6						Comparator Bit B1
	C1-C6						+5V logic '1'

A-9**Memory Option Configuration**

JB12

opt input o o GND

A-10**DMA Chain Enable (JB13)**

JB13

Pin 41 o o Pin 40

A-11**Programming The CTC****A-11.1****Channel Selection**

DSTD products using the Z80 CTC decode the CTC to occupy 4 contiguous port addresses. Writing to the appropriate port address will automatically select the correct register in the CTC.

A-11.2 Interrupt Vectors

If any one of the CTC channels is going to be used with its interrupt enabled, an Interrupt Vector must be written to the CTC. The use need only supply the 5 high bits of one vector as the CTC assumes the vector points to 4 contiguous byte pairs corresponding to the 4 channels. Note that D0 must equal 0 to indicate that the word being written to the CTC is an interrupt vector; this also requires vectored addresses to start at an even memory locations.

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	X	X	0
<USER SUPPLIED VECTOR>					<SUPPLIED BY CTC>		

A-11.3 Channel Control Register

The control register bit functions are as illustrated below.

D7	D6	D5	D4	D3	D2	D1	D0
INT					LOAD		
ENA	MODE	RANGE	SLOPE	TRIG	TC	RESET	1

D0 = 0 indicates the byte is an INTERRUPT VECTOR.

D0 = 1 indicates the byte is a CONTROL WORD.

D1 = 0 the channel continues current operation.

D1 = 1 the channel is immediately RESET to control word values.

D2 = 0 indicates NO TIME CONSTANT to follow.

D2 = 1 the next I/O byte will be a TIME CONSTANT. (1 to 256)

D3 = 0 timer will FREE-RUN starting on next processor cycle.

D3 = 1 indicates timer will start on EXTERNAL TRIGGER.

D4 = 0 indicates external trigger on NEGATIVE-GOING edge.

D4 = 1 indicates external trigger on POSITIVE-GOING edge.

D5 = 0 indicates prescaler factor of 16. (timer mode only)

D5 = 1 indicates prescaler factor of 256. (timer mode only)

D6 = 0 indicates TIMER mode. (prescaler is enabled)

D6 = 1 indicates COUNTER mode. (prescaler disabled)

D7 = 0 INTERRUPT DISABLED for that channel.

D7 = 1 INTERRUPT on zero count ENABLED for the channel.

APPENDIX B
STD-Z80 BUS SIGNALS

APPENDIX B

STD-Z80 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	Ground - System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	
15	A7	Address Bus (Tri-state, output, active high).
16	A15	
17	A6	
18	A14	

STD-Z80 BUS PIN OUT

19	A5	A0-A15 make up a 16-bit address bus. The address bus provides the address for memory (up to 65k bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Memory Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Memory Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-State output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 Systems DSTD.

STD-Z80 BUS PIN OUT

36	/MEMEX	Memory expansion, not used on dy-4 Systems DSTD cards.
37	/REFRESH	/REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic zero and the upper 8 bits of the address bus contains the I register.
38	/DEBUG	/DEBUG (Input) used in conjunction with DDT-80 operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the /DEBUG line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
39	/M1	Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the opcode fetch cycle of an instruction. Note that during the execution of a 2-byte opcodes, /M1 will be generated as each opcode is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
40	STATUS 0	DMA priority chain input.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

STD-Z80 BUS PIN OUT

- 42 /BUSRQ Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.
- 43 /INTAK Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.
- 44 /INTRQ Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.
- 45 /WAITRQ WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

STD-Z80 BUS PIN OUT

46	/NMIRQ	Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will over-ride a /NMIRQ.
47	/SYSRESET	System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H and set Interrupt Mode 0.
48	/PBRESET	Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset.
49	/CLOCK	Processor Clock (Output, active low). Single phase system clock.
50	CNTRL	Auxiliary Timing
51	PCO	Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

STD-Z80 BUS PIN OUT

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.


APPENDIX C
PARTS LIST

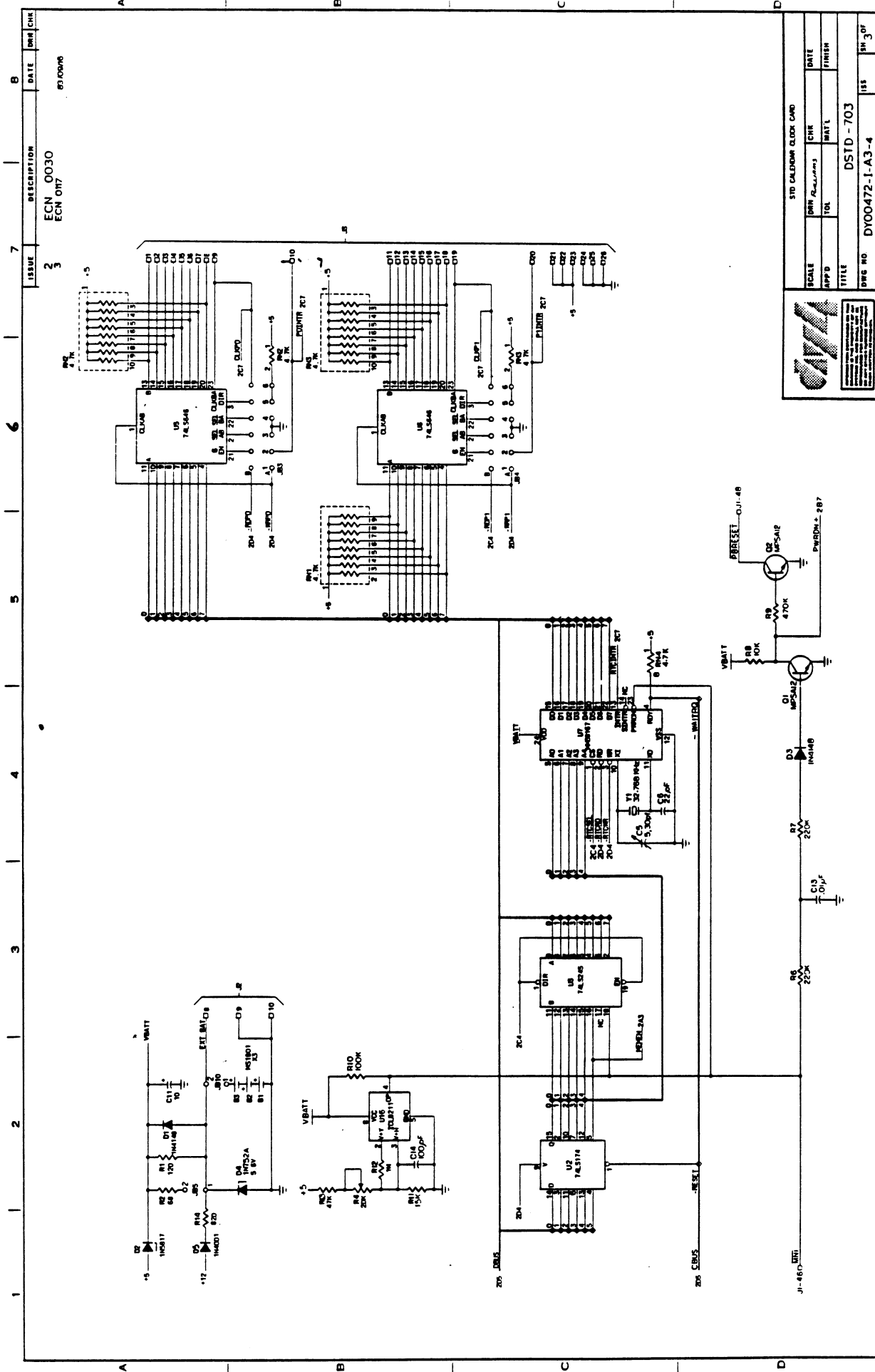
APPENDIX C

DSTD 703 PARTS LIST

DY4PART	QTY	DESCRIPTION	DESIGNATION
PT012032	1	74LS32 TTL-LS	U17
PT012085	1	74LS85 TTL-LS	U14
PT012139	1	74LS139 TTL-LS	U15
PT012174	1	74LS174 TTL-LS	U2
PT012245	6	74LS245 TTL-LS	U1,U3,U18,U19,U20,U23
PT012346	2	74LS646 TTL-LS (T.I. ONLY)	U5,U6
PT012682	1	74LS692 TTL-LS	U4
PT013005	1	74S05 TTL-S	U13
PT014001	1	MM58167AN CMOS	U7
PT014013	1	40H32 CMOS (TOSHIBA)	U22
PT015014	1	MK3882n-4 (280A-CTC) 4.00 MHZ CTC	U8
PT029001	1	ICL8211 CPA	U16
PT036001	1	PAL12L6	U21
PT041103	1	1/4 WATT, 10K OHM, 5% RESISTOR	R8
PT041104	1	1/4 WATT, 100K OHM, 5% RESISTOR	R10
PT041105	1	1/4 WATT, 1 MEG OHM, 5% RESISTOR	R12
PT041121	1	1/4 WATT, 120 OHM, 5% RESISTOR	R1
PT041153	1	1/4 WATT, 15K OHM, 5% RESISTOR	R11
PT041224	2	1/4 WATT, 220K OHM, 5% RESISTOR	R6,R7
PT041471	1	1/4 WATT, 470 OHM, 5% RESISTOR	R5
PT041472	1	1/4 WATT, 4.7K OHM, 5% RESISTOR	R3
PT041473	1	1/4 WATT, 47K OHM, 5% RESISTOR	R13
PT041474	1	1/4 WATT, 470K OHM, 5% RESISTOR	R9
PT041680	1	1/4 WATT, 68 OHM, 5% RESISTOR	R2
PT041821	1	1/4 WATT, 820 OHM, 5% RESISTOR	R14
PT042023	1	3299W-1-203 OR 64W203, 20K OHM POTENTIOMETER, TOP ADJUST	R4
PT043002	1	6 PIN, 5 RESISTOR, 4.7K OHM SIP RESISTOR NETWORK	RN5
PT043017	4	10 PIN, 9 RESISTOR, 4.7K OHM, SIP RESISTOR NETWORK	RN1,RN2,RN3,RN4
PT052000	1	CK05BX101K OR D645BZ101M, 100pf, 200V CERAMIC CAPACITOR	C14
PT052002	1	CK05BX220K, 22pf, 200V CERAMIC CAPACITOR	C6
PT052010	6	.1uf, 50V(.1 LD. SP.) 9121-050-Z5U-104M, CERAMIC CAPACITOR	C4,C7-C10,C12
PT053000	3	TAG10M25, 10uf, 25V TANTALUM CAPACITOR	C11,C21,C22
PT059000	9	.1uf 43V(.2 LD. SP.)1R47104M,POLYESTER FILM CAPACITOR	C1-C3,C15-C20
PT059001	1	1R47103M, .01uf, 43V POLYESTER FILM CAPACITOR (.2 LD. SP.)	C13
PT059003	1	5 - 30 pf, VARIABLE CAPACITOR	C5
PT061006	2	MPSA12 NPN DARLINGTON TRANSISTOR	Q1,Q2
PT071000	2	1N4148 SIGNAL DIODE	Q1,Q3
PT072001	1	1N752A ZENER DIODE	Q4
PT073001	1	1N4001 RECTIFIER	Q5
PT073002	1	1N5817 SHOTTKY RECTIFIER	Q2
PT102007	1	FOX 32.768 MHZ DISCRETE CRYSTAL	Y1
PT111073	1	S208-1 CARD EJECTOR WITH PINS	
PT112001	3	404016 NICAD BATTERY, 4AA, 190 SCL	B1,B2,B3
PT122003	2	CHD6960WIS 60 PIN DOUBLE ROW HEADER	J82-J84,J86-J89,J911
PT122004	1	CHS6936WIS 36 PIN SINGLE ROW HEADER	J81,J85,J910-J913
PT123001	1	102160-6 26 PIN RIGHT ANGLE CONNECTOR	J3
PT123002	1	102160-1 10 PIN RIGHT ANGLE CONNECTOR	J2
PT126020	1	640464-3 20 PIN I.C. SOCKET	U21
PT126024	1	640361-3 24 PIN I.C. SOCKET	U7
PT126028	5	640362-3 28 PIN I.C. SOCKET	U8-U12
PT347201	1	DSTD 703 DW00473-AA-01-3	
PT711016	1	703 MANUAL	

APPENDIX D
SCHEMATIC

 <p> <small> INFORMATION NOT CONTAINED ON THIS DOCUMENT IS THE PROPERTY OF THE SYSTEMS INC. AND SHALL NOT BE REPRODUCED FOR MANUFACTURE OR ANY OTHER BUSINESS WITHOUT WRITTEN PERMISSION. </small> </p>	STD CALENDAR CLOCK CARD			
	SCALE	DRN <i>WILLIAMS</i>	CHK	DATE <i>1982 01 02</i>
	APP'D	TOL	MAT'L	FINISH
	TITLE DSTD-703			
	DWG NO.	DI00472-I A1-4	ISS 2	SH 1 OF 3



APPENDIX E

DATA SHEETS MM58167A REAL TIME CLOCK

DATA SHEETS 74LS64X PARALLEL PORT DEVICES

MM58167A Microprocessor Real Time Clock

General Description

The MM58167A is a low threshold metal gate CMOS circuit that functions as a real time clock in bus oriented microprocessor systems. The device includes an addressable real time counter, 56 bits of RAM, and two interrupt outputs. A POWER DOWN input allows the chip to be disabled from the rest of the system for standby low power operation. The time base is a 32,768 Hz crystal oscillator.

Features

- Microprocessor compatible (8-bit data bus)
- 1/10,000 of a second through month counters
- 56 bits of RAM with comparator to compare the real time counter to the RAM data
- 2 INTERRUPT OUTPUTS with 8 possible interrupt signals
- POWER DOWN input that disables all inputs and outputs except for one of the interrupts
- Status bit to indicate rollover during a read
- 32,768 Hz crystal oscillator
- Four-year calendar (no leap year)
- 24-hour clock

Functional Description

Real Time Counter

The real time counter is divided into 4-bit digits with 2 digits being accessed during any read or write cycle. Each digit represents a BCD number and is defined in Table I. Any unused bits are held at a logical zero during a read and ignored during a write. An unused bit is any bit not necessary to provide a full BCD number. For example tens of hours cannot legally exceed the number 2, thus only 2 bits are necessary to define the tens of hours. The other 2 bits in the tens of hours digit are unused. The unused bits are designated in Table I as dashes.

The addressable portion of the counter is from 1/10,000 of a second to months. The counter itself is a ripple counter. The ripple delay is less than 60 μ s above 4.0V and 300 μ s at 2.0V.

RAM

56 bits of RAM are contained on-chip. These can be used for any necessary power down storage or as an alarm latch for comparison to the real time counter. The data in the RAM can be compared to the real time counter on a digit basis. The only digits that are not compared are the unit ten thousandths of seconds and tens of days of the week (these are unused in the real time counter). If the two most significant bits of any RAM digit are ones, then this RAM location will always compare.

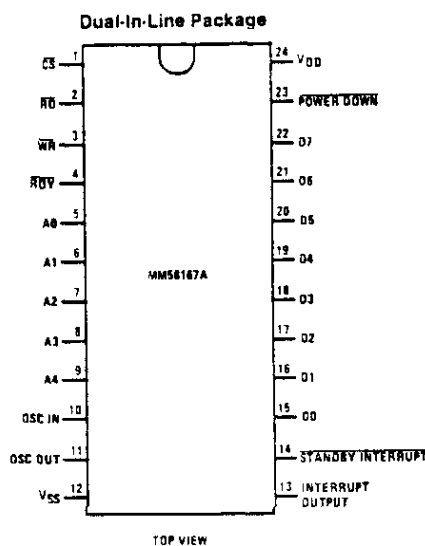
The RAM is formatted the same as the real time counter, 4 bits per digit, 14 digits, however there are no unused bits. The unused bits in the real time counter will compare only to zeros in the RAM.

Interrupts and Comparator

There are two interrupt outputs. The first and most flexible is the INTERRUPT OUTPUT (a true high signal). This output can be programmed to provide 8 different output signals. They are: 10 Hz, 1 Hz, once per minute, once per hour, once a day, once a week, once a month, and when a RAM/real time counter comparison occurs. To enable the output a one is written into the interrupt control register at the bit location corresponding to the desired output frequency (Figure 1). Once one or more bits have been set in the interrupt control register, the corresponding counter's rollover to its reset state will clock the interrupt status register and cause the interrupt output to go high. To reset the interrupt and to identify which frequency caused the interrupt, the interrupt status register is read. Reading this register places the contents of the status register on the data bus. The interrupting frequency will be identified by a one in the respective bit position. Removing the read will reset the interrupt.

The second interrupt is the STANDBY INTERRUPT (open drain output, active low). This interrupt occurs when enabled and when a RAM/real time counter comparison occurs. The STANDBY INTERRUPT is enabled by writing a one on the D0 line at address 16_H or disabled by writing a zero on the D0 line. This interrupt is not triggered by the edge of the compare signal, but rather by the level. Thus if the compare is enabled when the STANDBY INTERRUPT is enabled, the interrupt will turn on immediately.

Connection Diagram



Absolute Maximum Ratings

Voltage at All Pins	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature	$-40^{\circ}C$ to $85^{\circ}C$
Storage Temperature	$-65^{\circ}C$ to $150^{\circ}C$
$V_{DD} - V_{SS}$	6.0V
Lead Temperature (Soldering, 10 seconds)	$300^{\circ}C$

Electrical Characteristics $V_{SS} = 0V$, $-40^{\circ}C \leq T_A \leq 85^{\circ}C$

Parameter	Conditions	Min	Max	Units
Supply Voltage				
V_{DD}	Outputs Enabled	4.0	5.5	V
V_{DD}	POWER DOWN Mode	2.0	5.5	V
Supply Current				
I_{DD} , Static	Outputs TRI-STATE [*] $f_{IN} = DC$, $V_{DD} = 5.5V$		10	μA
I_{DD} , Dynamic	Outputs TRI-STATE $f_{IN} = 32\text{ kHz}$, $V_{DD} = 5.5V$ $V_{IH} \geq V_{DD} - 0.3V$ $V_{IL} \leq V_{SS} + 0.3V$		20	μA
I_{DD} , Dynamic	Outputs TRI-STATE $f_{IN} = 32\text{ kHz}$, $V_{DD} = 5.5V$ $V_{IH} = 2.0V$, $V_{IL} = 0.8V$		12	mA
Input Voltage				
Logical Low		0.0	0.8	V
Logical High		2.0	V_{DD}	V
Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-1	1	μA
Output Impedance	I/O and INTERRUPT OUT			
Logical Low	$V_{DD} = 4.5V$, $I_{OL} = 1.6\text{ mA}$		0.4	V
Logical High	$V_{DD} = 4.5V$, $I_{OH} = -400\text{ }\mu A$ $I_{OH} = -10\text{ }\mu A$	2.4 0.8 V_{DD}		V
TRI-STATE	$V_{SS} \leq V_{OUT} \leq V_{DD}$	-1	1	V
Output Impedance	RDY and STANDBY INTERRUPT			
Logical Low, Sink	$V_{DD} = 4.5V$, $I_{OL} = 1.6\text{ mA}$		0.4	V
Logical High, Leakage	$V_{OUT} \leq V_{DD}$		10	μA

Functional Description (Continued)

TABLE I. REAL TIME COUNTER FORMAT

Counter Addressed		Units				Max BCD Code	Tens				Max BCD Code
		D0	D1	D2	D3		D4	D5	D6	D7	
1/10,000 of Seconds	(00 _H)	-	-	-	-	0	D4	D5	D6	D7	9
Hundredths and Tenths Sec	(01 _H)	D0	D1	D2	D3	9	D4	D5	D6	D7	9
Seconds	(02 _H)	D0	D1	D2	D3	9	D4	D5	D6	-	5
Minutes	(03 _H)	D0	D1	D2	D3	9	D4	D5	D6	-	5
Hours	(04 _H)	D0	D1	D2	D3	9	D4	D5	-	-	2
Day of the Week	(05 _H)	D0	D1	D2	-	7	-	-	-	-	0
Day of the Month	(06 _H)	D0	D1	D2	D3	9	D4	D5	-	-	3
Month	(07 _H)	D0	D1	D2	D3	9	D4	-	-	-	1

(-) indicates unused bits

TRI-STATE^{*} is a registered trademark of National Semiconductor Corp.

Functional Description (Continued)

TABLE II. ADDRESS CODES AND FUNCTIONS

A4	A3	A2	A1	A0	Function
0	0	0	0	0	Counter—Ten Thousandths of Seconds
0	0	0	0	1	Counter—Hundredths and Tenths of Seconds
0	0	0	1	0	Counter—Seconds
0	0	0	1	1	Counter—Minutes
0	0	1	0	0	Counter—Hours
0	0	1	0	1	Counter—Day of Week
0	0	1	1	0	Counter—Day of Month
0	0	1	1	1	Counter—Month
0	1	0	0	0	RAM—Ten Thousandths of Seconds
0	1	0	0	1	RAM—Hundredths and Tenths of Seconds
0	1	0	1	0	RAM—Seconds
0	1	0	1	1	RAM—Minutes
0	1	1	0	0	RAM—Hours
0	1	1	0	1	RAM—Day of Week
0	1	1	1	0	RAM—Day of Month
0	1	1	1	1	RAM—Months
1	0	0	0	0	Interrupt Status Register
1	0	0	0	1	Interrupt Control Register
1	0	0	1	0	Counter Reset
1	0	0	1	1	RAM Reset
1	0	1	0	0	Status Bit
1	0	1	0	1	GO Command
1	0	1	1	0	STANDBY INTERRUPT
1	1	1	1	1	Test Mode

All others unused

TABLE III. COUNTER AND RAM RESET FORMAT

D0	D1	D2	D3	D4	D5	D6	D7	Counter or RAM Reset
1	0	0	0	0	0	0	0	Ten Thousandths of Seconds
0	1	0	0	0	0	0	0	Hundredths and Tenths of Seconds
0	0	1	0	0	0	0	0	Seconds
0	0	0	1	0	0	0	0	Minutes
0	0	0	0	1	0	0	0	Hours
0	0	0	0	0	1	0	0	Days of the Week
0	0	0	0	0	0	1	0	Days of the Month
0	0	0	0	0	0	0	1	Months

For counters reset address = 12H

For RAM reset address = 13H

Functional Description (Continued)

The comparator is a cascaded exclusive NOR. Its output is latched 61 μ s after the rising edge of the 1 kHz clock signal (input to the ten thousandths of seconds counter). This allows the counter to ripple through before looking at the comparator. For operation at less than 4.0V, the thousandths of seconds counter should not be included in a compare because of the possibility of having a ripple delay greater than 61 μ s. (For output timing see Interrupt Timing.)

Power Down Mode

The **POWER DOWN** input is essentially a second chip select. It disables all inputs and outputs except for the **STANDBY INTERRUPT**. When this input is at a logical zero, the device will not respond to any external signals. It will, however, maintain timekeeping and turn on the **STANDBY INTERRUPT** if programmed to do so. (The programming must be done before the **POWER DOWN** input goes to a logical zero.) When switching V_{DD} to the standby or power down mode, the **POWER DOWN** input should go to a logical zero at least 1 μ s before V_{DD} is switched. When switching V_{DD} all other inputs must remain between $V_{SS} - 0.3V$ and $V_{DD} + 0.3V$. When restoring V_{DD} to the normal operating mode, it is necessary to insure that all other inputs are at valid levels before switching the **POWER DOWN** input back to a logical one. These precautions are necessary to insure that no data is lost or altered when changing to or from the power down mode.

Counter and RAM Resets; GO Command

The counters and RAM can be reset by writing the proper data at address 12_H or address 13_H respectively. The resets are divided up the same way as the counters and RAM are divided up when accessing them. The data written into the part will determine which set of 2 digits (1 digit for ten thousandths of seconds and days of the week) will be reset. The address will determine whether the 2 digits are in the RAM or in the real time counter. Each logical one on the data bus will cause 2 digits to be reset. Resetting the most significant used bit of any counter will clock the following counter.

A write pulse at address 15_H will reset the thousandths, hundredths, tenths, units, and tens of seconds counters. This **GO** command is used for precise starting of the clock. The data on the data bus is ignored during the write. If the seconds counter is at a value greater than 40 when the **GO** is issued, the minute counter will increment; otherwise the minute counter is unaffected. This command is not necessary to start the clock, but merely a convenient way to start precisely at a given minute. (See Table III for reset format.)

Status Bit

The status bit is provided to inform the user that the clock is in the process of rolling over when a counter is read. The 1 kHz clock into the thousandths of seconds counter has a pulse width of 61 μ s. If a read of the real time counter (any digits) is done during this 61 μ s period the status bit will be set. This tells the user that the clock is rippling through the real time counter. Because the clock is rippling, invalid data may be read from the counter. If the status bit is set following a counter read, the counter should be reread.

The status bit appears on D0 when address 14_H is read. All the other data lines will be zero. The bit is set when a logical one appears. This bit should be read every time a counter read or series of counter reads are done. The trailing edge of the read at address 14_H will reset the status bit.

Oscillator

The oscillator used is the standard Pierce oscillator. Externally only 2 capacitors and the crystal are required. For micropower crystals a resistor in series with the oscillator output may be necessary to insure the crystal is not overdriven. This resistor should be approximately 200 k Ω . The capacitor values should be typically 20 pF–25 pF. The crystal frequency is 32,768 Hz.

The oscillator input can be externally driven, if desired. In this case the output should be left floating and the input levels should be within 0.3V of the supplies.

A ground line or ground plane between pins 9 and 10 may be necessary to prevent interference of the oscillator by the A4 address.

Control Lines

The **READ**, **WRITE**, and **CHIP SELECT** signals are active low inputs. The **READY** signal is an open drain output. At the start of each read or write cycle the **READY** line (open drain) will pull low and will remain low until valid data from a chip read appears on the bus or data on the bus is latched in during a write. **READ** and **WRITE** must be accompanied by a **CHIP SELECT** (see Figures 3 and 4 for read and write cycle timing).

Test Mode

The test mode is merely a mode for production testing. It allows the counters to count at a higher than normal rate. In this mode the 32 kHz oscillator input is connected directly to the ten thousandths of seconds counter. The chip select and write lines must be low and the address must be held at 1F_H.

Functional Description (Continued)

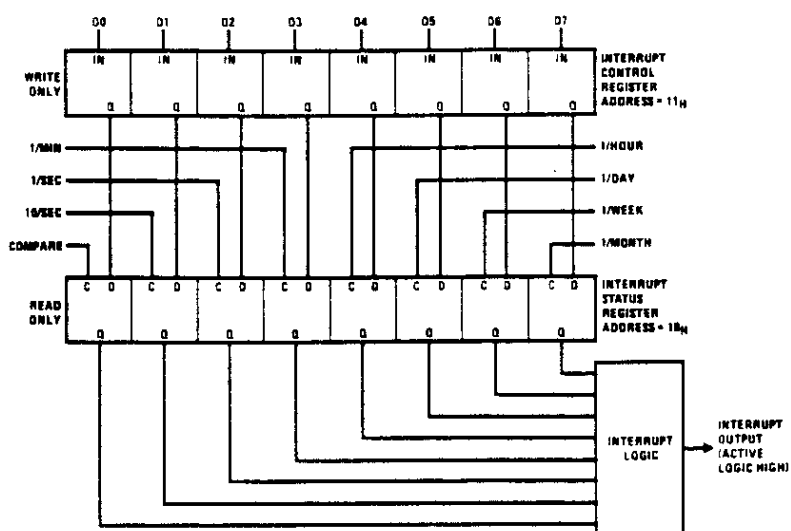


FIGURE 1. Interrupt Register Format

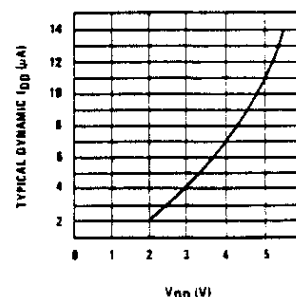


FIGURE 2. Typical Supply Current vs Supply Voltage

Interrupt Timing – $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$, $V_{SS} = 0\text{V}$

Parameter	Min	Max	Units
t_{INTON} Status Register Clock to INTERRUPT OUTPUT (Pin 13) High (Note 1)		5	μS
t_{SBYON} Compare Valid to STANDBY INTERRUPT (Pin 14) Low (Note 1)		5	μS
t_{INTOFF} Trailing Edge of Status Register Read to INTERRUPT OUTPUT Low		5	μS
t_{SBYOFF} Trailing Edge of Write Cycle (D0 = 0; Address = 16H) to STANDBY INTERRUPT Off (High Impedance State)		5	μS

Note 1: The status register clocks are: the corresponding counter's rollover to its reset state or the compare becoming valid. The compare becomes valid 81 μs after the 1/10,000 of a second counter is clocked, if the real time counter data matches the RAM data.

Read Cycle Timing – $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$, $V_{SS} = 0\text{V}$

Parameter	Min	Max	Units
t_{AR} Address Bus Valid to Read Strobe	100		ns
t_{CSR} Chip Select to Read Strobe	0		ns
t_{RRY} Read Strobe to Ready Strobe		150	ns
t_{RYD} Ready Strobe to Data Valid		800	ns
t_{AD} Address Bus Valid to Data Valid		1050	ns
t_{RH} Data Hold Time From Trailing Edge of Read Strobe	0		ns
t_{HZ} Trailing Edge of Read Strobe to TRI-STATE Mode		250	ns
t_{RYH} Read Hold Time after Ready Strobe	0		ns
t_{RA} Address Bus Hold Time from Trailing Edge of Read Strobe	50		ns

Write Cycle Timing – $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$, $V_{SS} = 0\text{V}$

Parameter	Min	Max	Units
t_{AW} Address Valid to Write Strobe	100		ns
t_{CSW} Chip Select to Write Strobe	0		ns
t_{DW} Data Valid before Write Strobe	100		ns
t_{WRY} Write Strobe to Ready Strobe		150	ns
t_{RY} Ready Strobe Width		800	ns
t_{RYH} Write Hold Time after Ready Strobe	0		ns
t_{WD} Data Hold Time after Write Strobe	110		ns
t_{WA} Address Hold Time after Write Strobe	50		ns

Data bus loading is 100 pF.

Ready output loading is 50 pF and 20 k Ω pull-up.

Input and output AC timing levels:

Logical one = 2.0V

Logical zero = 0.8V

Read and Write Cycle Timing Diagrams

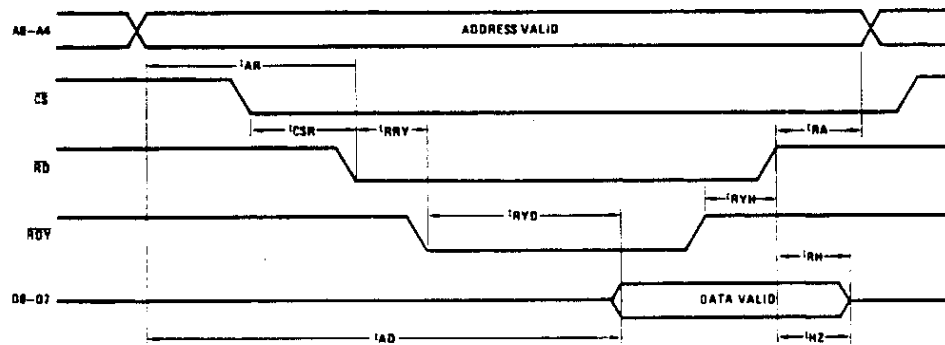


FIGURE 3. Read Cycle Timing

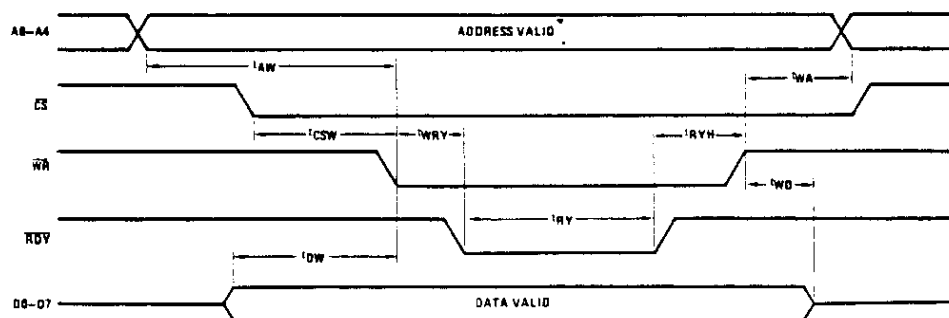
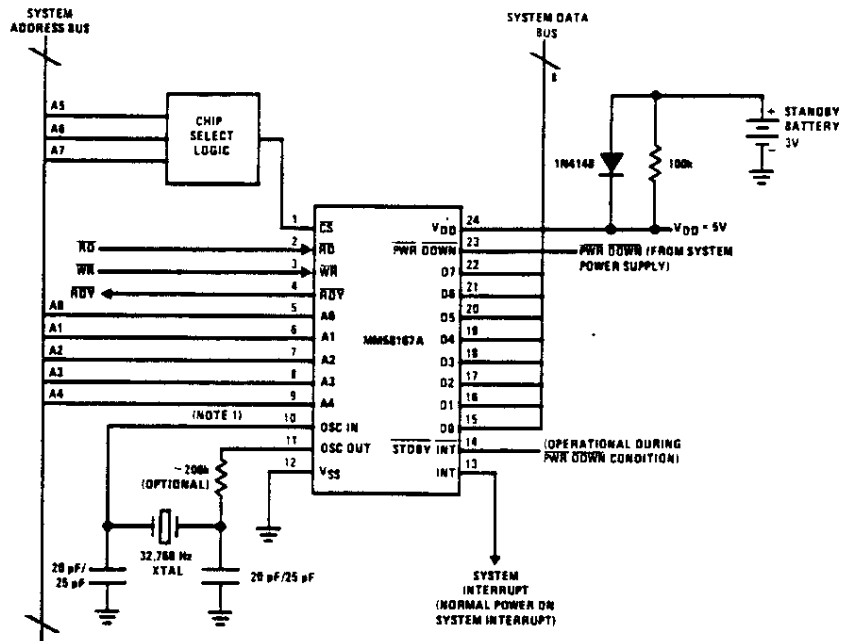


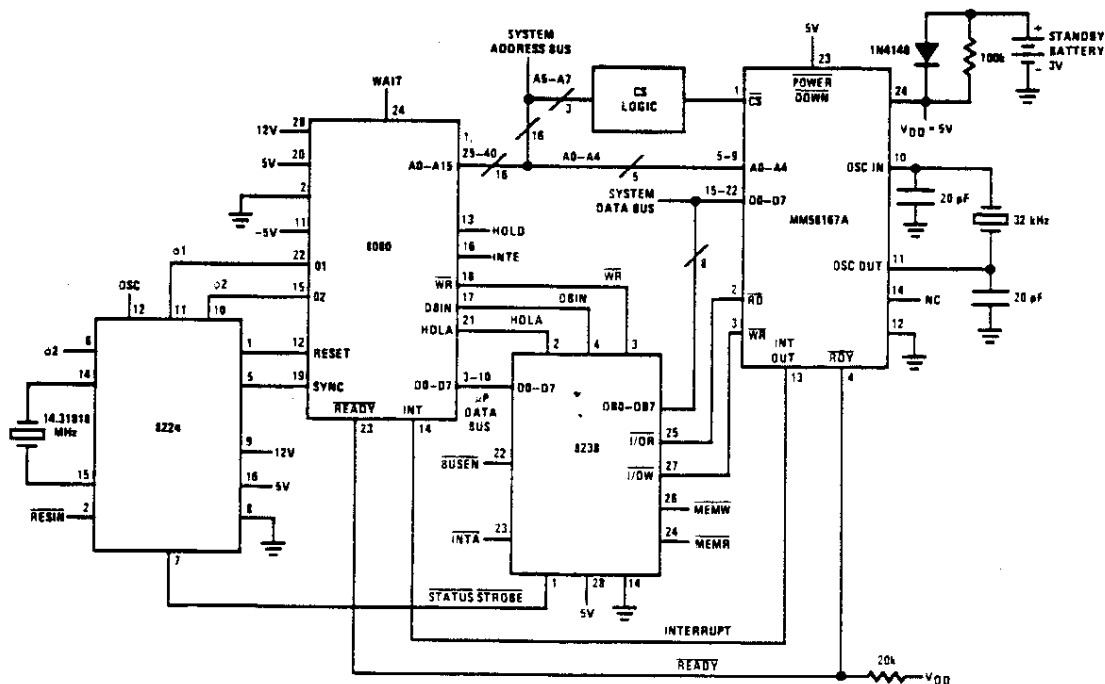
FIGURE 4. Write Cycle Timing

Typical Applications



Note 1: A ground line or ground plane guard trace should be included between pins 9 and 10 to insure the oscillator is not disturbed by the address line.

FIGURE 5. Typical Connection Diagram



Note 1: Must use 8238 or equivalent logic to insure advanced \overline{RDY} pulse; so that the ready output of the MM58167A is valid by the end of $\phi 2$ during the T2 microcycle.

Note 2: $t_{\phi 2} \geq t_{RS8080} + t_{DL8238} + t_{WR58167}$.

FIGURE 6. 8080 System Interface with Battery Backup

TTL
LSI

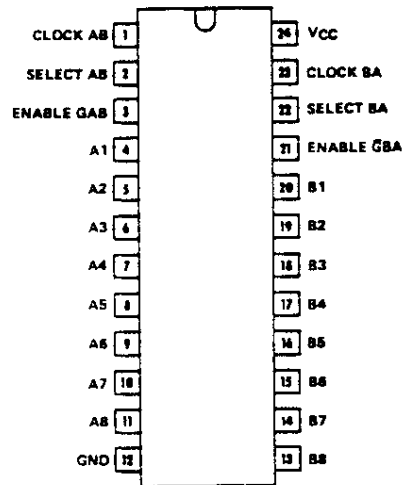
TYPES SN54LS646 THRU SN54LS649 SN74LS646 THRU SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

D2581, JANUARY 1981

- Bidirectional Bus Transceivers/Registers in the New JT and NT 24-pin 300-mil Packages
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs

DEVICE	OUTPUT	LOGIC
'LS646	3-State	True
'LS647	Open-Collector	True
'LS648	3-State	Inverting
'LS649	Open-Collector	Inverting

SN54LS*...JT PACKAGE
SN74LS*...JT OR NT PACKAGE
(TOP VIEW)

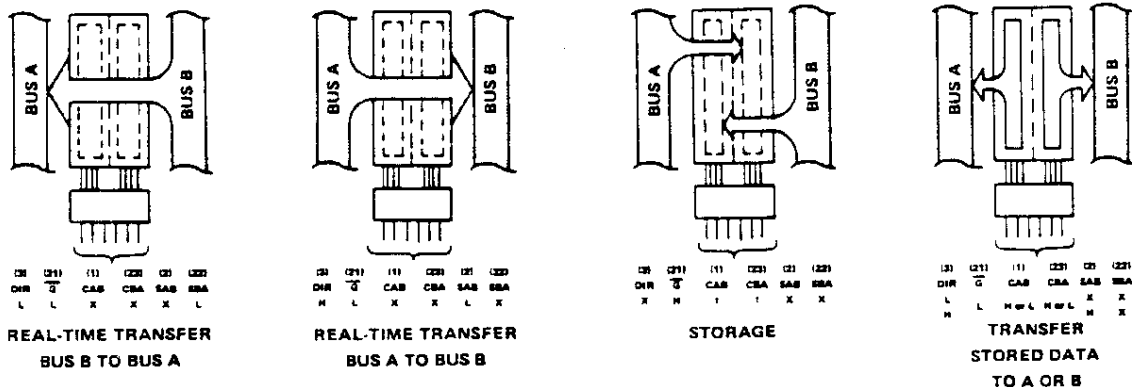


description

These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control \bar{G} and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control \bar{G} is active (low). In the isolation mode (control \bar{G} high), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled, and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'LS646, 'LS647, 'LS648, or 'LS649.



TYPES SN54LS646 THRU SN54LS649, SN74LS646 THRU SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

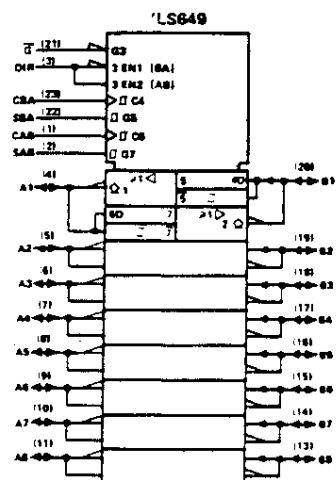
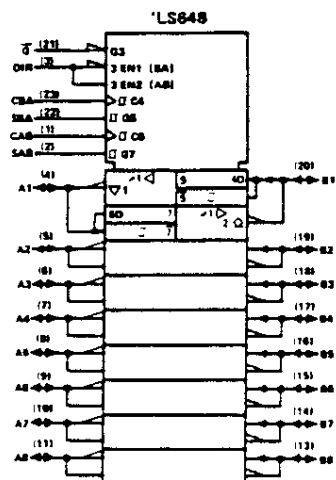
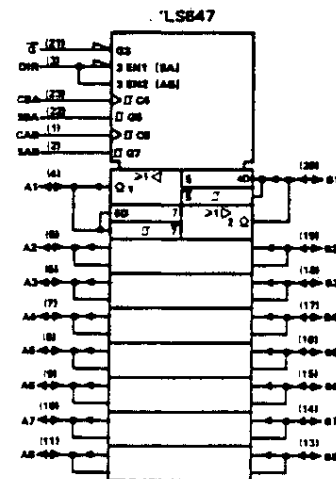
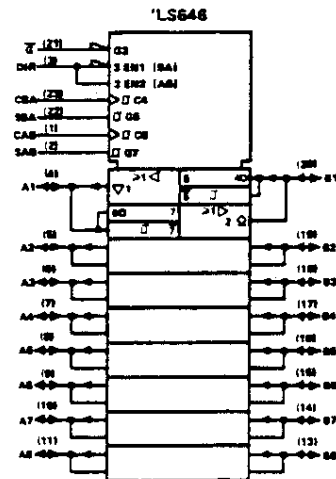
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
\overline{G}	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'LS646, 'LS647	'LS648, 'LS649
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time B Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored A Data to B Bus

H = high level L = low level X = irrelevant ↑ = low-to-high-level transition

*The data output functions may be enabled or disabled by various signals at the \overline{G} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols

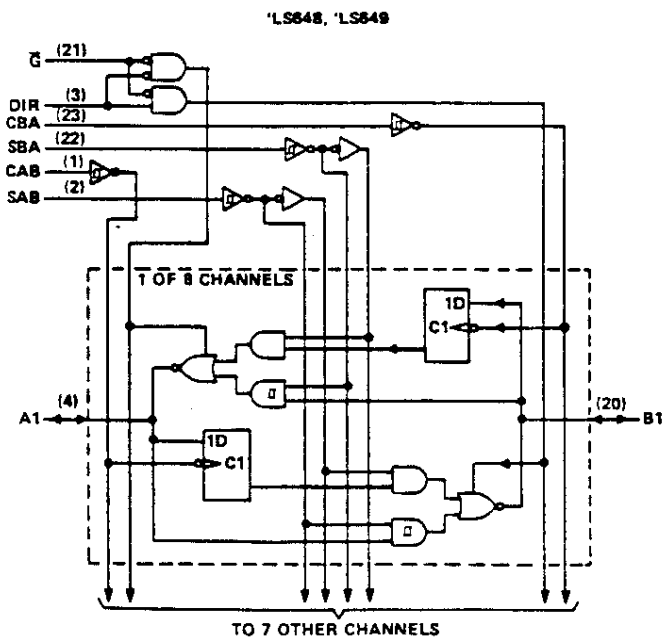
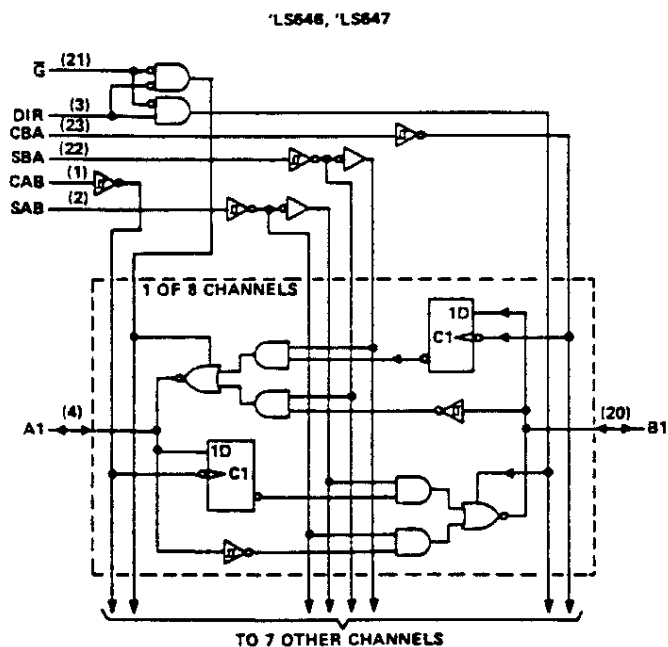


TYPES SN54LS646 THRU SN54LS649, SN74LS646 THRU SN74LS649

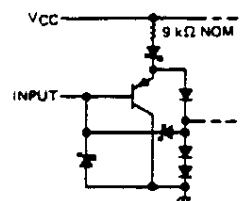
OCTAL BUS TRANSCEIVERS AND REGISTERS

functional block diagram (positive logic)

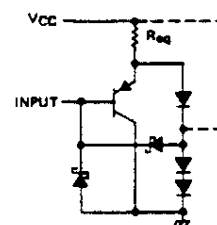
schematics of inputs and outputs



EQUIVALENT OF DIRECTION INPUTS

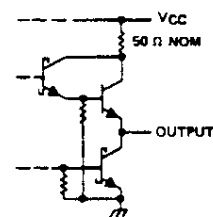


EQUIVALENT OF ALL OTHER INPUTS



A and B: $R_{eq} = 15 \text{ k}\Omega \text{ NOM}$
 CAB and CBA: $R_{eq} = 10 \text{ k}\Omega \text{ NOM}$
 SAB and SBA: $R_{eq} = 6 \text{ k}\Omega \text{ NOM}$

TYPICAL OF ALL 'LS646, 'LS648 OUTPUTS



TYPICAL OF ALL 'LS647, 'LS649 OUTPUTS



TYPES SN54LS646, SN54LS648, SN74LS646, SN74LS648 **OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (control inputs)	7 V
Off-state output voltage (A and B ports)	5.5 V
Operating free-air temperature: SN54LS646, SN54LS648	-55°C to 125°C
SN74LS646, SN74LS648	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54LS646 SN54LS648			SN74LS646 SN74LS648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-12			-15	mA
Low-level output current, I_{OL}				12			24	mA
Width of clock pulse, t_W		20			20			ns
Setup time, t_{SU}	Bus to clock	20			20			ns
Hold time, t_H	Bus from clock	0			0			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

NOTE 1: All voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS646 SN54LS648		SN74LS646 SN74LS648		UNIT	
				MIN	TYP‡	MAX	MIN		TYP‡
V _{IH}	High-level input voltage			2			2	V	
V _{IL}	Low-level input voltage					0.5		0.6	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA				-1.5		-1.5	
	Hysteresis (V _{I+} - V _{I-}), A or B input	V _{CC} = MIN		0.1	0.4		0.2	0.4	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max}	I _{OH} = -3 mA	2.4	3.4		2.4	3.4	
			I _{OH} = MAX	2		2			
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max}	I _{OL} = 12 mA		0.25	0.4		0.25	0.4
			I _{OL} = 24 mA				0.35	0.5	
I _{OZH}	Off-state output current, high-level voltage applied	V _{CC} = MAX, V _O = 2.7 V				20		20	
I _{OZL}	Off-state output current, low-level voltage applied	V _{CC} = MAX, V _O = 0.4 V				-400		-400	
I _I	Input current at maximum input voltage	A or B	V _{CC} = MAX	V _I = 5.5 V			0.1		
		All others		V _I = 7 V			0.1		
I _{IH}	High-level input current	V _{CC} = MAX, V _{IH} = 2.7 V				20		20	
I _{IL}	Low-level input current	V _{CC} = MAX, V _{IL} = 0.4 V				-0.4		-0.4	
I _{OS}	Short-circuit output current‡	V _{CC} = MAX, V _O = 0		-40		-225	-40	-225	
I _{CC}	Total supply current	'LS646	V _{CC} = MAX, Outputs open	Outputs high		91	145	91	145
				Outputs low		103	165	103	165
				Outputs at Hi-Z		103	165	103	165
		'LS648	V _{CC} = MAX, Outputs open	Outputs high		78		78	
				Outputs low		86		86	
				Outputs at Hi-Z		88		88	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

TYPES SN54LS646, SN54LS648, SN74LS646, SN74LS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER ^o	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS646		'LS648		UNIT	
				MIN	TYP	MAX	MIN		TYP
t _{PLH}	Clock	Bus	R _L = 667 Ω, C _L = 45 pF, See Note 2		15	25		15	ns
t _{PHL}					23	35		26	ns
t _{PLH}	Bus	Bus			12	18		25	ns
t _{PHL}					13	20		23	ns
t _{PLH}	Select, with bus input high†	Bus			33	50		36	ns
t _{PHL}					14	25		36	ns
t _{PLH}	Select, with bus input low†				26	40		27	ns
t _{PHL}					21	35		27	ns
t _{PZH}	Enable	Bus			33	55		30	ns
t _{PZL}					42	65		38	ns
t _{PZH}	Direction				28	45		24	ns
t _{PZL}					39	60		35	ns
t _{PHZ}	Enable	Bus	R _L = 667 Ω, C _L = 5 pF, See Note 2		23	35		23	ns
t _{PLZ}					22	35		22	ns
t _{PHZ}	Direction				20	30		23	ns
t _{PLZ}					19	30		19	ns

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition.

TYPES SN54LS647, SN54LS649, SN74LS647, SN74LS649 **OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS**

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (control inputs)	7 V
Off-state output voltage (A and B ports)	5.5 V
Operating free-air temperature range: SN54LS647, SN54LS649	-55°C to 125°C
SN74LS647, SN74LS649	-0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_w	20			20			ns
Setup time, t_{SU}	20			20			ns
Hold time, t_H	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: All voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.5			0.6	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
	Hysteresis ($V_{I+} - V_{I-}$), A or B input	$V_{CC} = \text{MIN}$	0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$			100			100	µA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
		$I_{OL} = 24 \text{ mA}$					0.35	0.5	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			0.1			0.1	mA
		$V_I = 7 \text{ V}$			0.1			0.1	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.5 \text{ V}$			20			20	µA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{CC}	Total Supply Current	LS647	$V_{CC} = \text{MAX},$ Outputs high	Outputs high	79	130	79	130	mA
					94	150	94	150	
		LS649	$V_{CC} = \text{MAX},$ Outputs high	Outputs high	76		76		
					90		90		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All Typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

TYPES SN54LS647, SN54LS649, SN74LS647, SN74LS649
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS647			'LS649			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Clock	Bus	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$. See Note 2		22	35		24		ns
t_{PHL}					28	45		26		ns
t_{PLH}	Bus	Bus			17	26		23		ns
t_{PHL}					18	27		23		ns
t_{PLH}	Select, with bus input high†	Bus			39	60		42		ns
t_{PHL}					19	30		36		ns
t_{PLH}	Select, with bus input low†				33	50		36		ns
t_{PHL}					29	45		27		ns
t_{PLH}	Enable	Bus			25	40		25		ns
t_{PHL}					33	50		35		ns
t_{PLH}	Direction				23	35		32		ns
t_{PHL}					25	40		29		ns

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

† These parameters are measured with the internal outputs state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition.