

OPERATIONS MANUAL

DSTD DUAL DENSITY
711 FLOPPY DISK
CONTROLLER
WITH DMA
AND 64K
DYNAMIC RAM
DY00483



dy-4 SYSTEMS INC.

**DSTD-711 DUAL DENSITY FLOPPY DISK CONTROLLER
WITH DMA AND 64K DYNAMIC RAM
OPERATIONS MANUAL**

DY00483

covering part numbers:

DSTD-711-2.5	DSTD-711A-2.5
DSTD-711-4.0	DSTD-711A-4.0

Acknowledgements

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PREPARED BY: dy-4 SYSTEMS INC.

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SECTION 1

1.0 GENERAL INFORMATION

1.1 DSTD Series General Description

The dy-4 DSTD Series of Z80/STD-BUS compatible products was designed to satisfy the need for high performance microcomputer modules that could be quickly and inexpensively integrated into a variety of end-user applications. The popular STD-BUS motherboard interconnect system concept provides expandability as needs change. Support by numerous manufacturers provides the user with a choice from scores of compatible products.

The modules for the Z80/STD-BUS are a compact 4.5 x 6.5 inches (11.43 X 16.51 cm) which provides for system partitioning by function, i.e. CPU, Memory, I/O, etc. dy-4 SYSTEMS has been able to combine most popular functions on single cards to reduce system card count and cost. In addition, we pride our dedication to quality and innovation; delivering reliable solutions to tomorrow's problems.

1.2 DSTD-711 Features

The DSTD-711 combines two necessary system functions on a single card: Floppy Disk Control and Dynamic Ram.

In typical development system and data processing applications, a disk based operating system is required. Today, these systems are usually configured with 64K bytes of main memory; the maximum allowed with an eight bit microprocessor. By combining both these functions on a single card, total system card count, and cost usually, are reduced.

The Floppy Disk Controller Section utilizes a Western Digital WD1797B02 which provides the user with macro-level disk control commands greatly simplifying the manipulation of data on both 5-1/4" and 8" floppy disks. Various sector size, stepping rate, head movement, read/write and format options can be programmed using one of its 11 command types. (Complete programming details are included in Appendix E.)

The DSTD-711 includes a four bit wide Drive Select Register which can be used with both radial and binary select type floppy disk drives. A two bit register allows selection of single and double sided drives for both 5-1/4" and 8" types. Finally, another two bit register allows the user to dynamically select the density and size of drive to be used.

The DMA Section incorporates a Zilog/Mostek DMA Controller that provides a closely coupled data transfer capability between main memory and the Data Port of the Floppy Disk Controller. Although data transfers can be performed under processor control, (either in a polled or interrupt driven mode,) the DMA simplifies this job and allows the processor to do other jobs during data transfer. The DMA may also be used for memory - memory transfers.

1.3 Configuration by Part Number

DSTD-711 part numbers subscripted with the letter 'A' do not include the Dynamic Memory Section. A '-2.5' subscript indicates that the card is rated for 2.5 MHz operation; a '-4.0' subscript indicates 4 MHz operation.

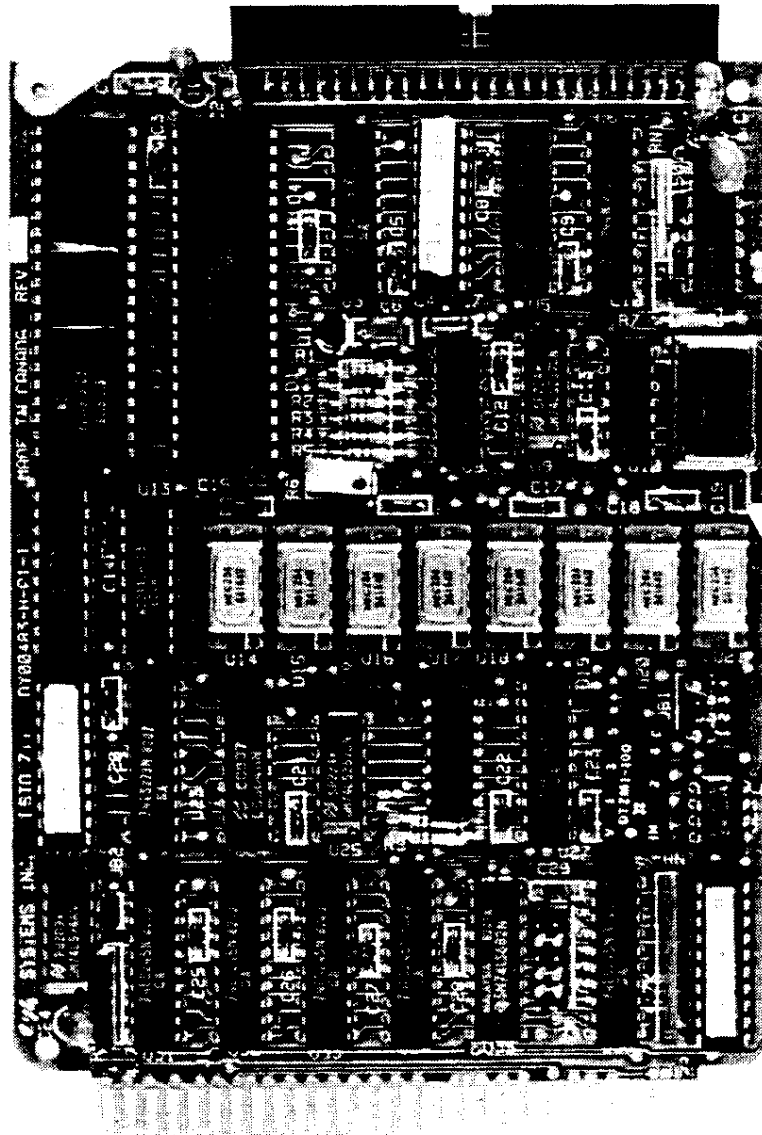


FIGURE 1-1 DSTD-711 MODULE

SECTION 2

2.0 FUNCTIONAL DESCRIPTION

2.1 Use/Application

The DSTD-711 is usually one of several cards configured in a software development system utilizing CP/M as the DOS. This system can include as few as two cards: a DSTD-102 providing Z80 CPU, Z80 SIO (two RS-232C Channels,) and bootstrap PROMS, and the DSTD-711. The dy-4 SYSTEMS implementation of CP/M incorporates several features which make it faster and more convenient to use than most. Because it can be bought to work directly on this combination of hardware, it is recommended.

2.2 Floppy Disk Controller Section

The Floppy Disk Controller Section on the DSTD-711 includes digital data separation, write precompensation, drive select, density select and side select circuitry which allows the use of single or double density, single or double sided, soft sector 5-1/4" or 8" floppy disk drives.

Only Shugart compatible interface floppy drives can be used.

The I/O Base Port at which the DSTD-711 can be strapped is described later in Section 3 - 3. Table 2 - 1 below defines these ports and their use.

TABLE 2 - 1

PORT ALLOCATION

Base Port+0:	R/W	1797	Command/Status Register
Base Port+1:	R/W	1797	Track Register
Base Port+2:	R/W	1797	Sector Register
Base Port+3:	R/W	1797	Data Register
Base Port+4:	R/W		DMA Command Register
Base Port+5:	W/O		Drive Select Register
Base Port+6:	W/O		Mode Register
Base Port+7:	W/O		Memory Page Select Register

Where: R/W = The register may be both read from and written to
W/O = The register may only be written to, (reading these registers has no effect on their contents)

Complete programming information for both the Western Digital WD1797B02 and Mostek/Zilog DMA are included in the appendix.

The DSTD-711 may be used in an interrupt driven mode either by itself or with other interrupting devices, (where its location within the STD BUS PCI/PCO chain must be nearest the processor to avoid data lost errors from the 1797 data register.) The powerful Z80 Mode 2 interrupt type may be used if interrupts are generated by the Z-80 DMA.

2.2.1 Drive Select Register

The drive select register is used to select which drive on the floppy disk cable daisy chain should respond to commands from the controller. A six bit non-inverting latch is used to hold this information. Four bits select the drive and two bits select the side for 8" and 5-1/4" drives.

The drive select data in this register is passed directly to the drive interface cable. Since the drive select lines are active low, to select drive 0 you would place 1110B in the lower four bits of the Drive Select Register.

Most eight inch drives decode one of four bits (active low at the interface) and thus allow up to four drives to be accessed. Five inch drives reserve bit three for 'motor on' and thus typically only access three drives. The DSTD-711 utilizes an otherwise unused pin 50 on the drive cable connector, for the drive-four select so that four drives may be used in systems that use a combination of eight and five inch drives.

In systems using four drives, pin 50 on the connector from the controller cable at the fourth drive must be jumpered to the drive-four select pin on the floppy disk drive (pin 32.) This connection should be made instead of the normal jumper block between pairs of pins to select drives one through three, (pins 26, 28, and 30 on Shugart compatible drives.)

Table 2 - 2 below summarizes the standard drive select values used with eight inch floppy drives.

TABLE 2 - 2
DRIVE SELECT VALUES
(Radial Select Technique)

	Binary	Hex
Drive 0 or 'A':	1110B	0EH
Drive 1 or 'B':	1101B	0DH
Drive 2 or 'C':	1011B	0BH
Drive 3 or 'D':	0111B	07H

Some drives allow binary selection. This technique is also supported on the DSTD-711. A bit pattern is presented to the drive

which is in binary code, i.e. 1110B for one, 1100B for three, 1010B for five, etc. (Remember that drive select is active low.) In this way up to 15 drives which are equipped for this decoding method may be accessed.

The bit patterns written to select drives one through three in a five inch drive system are identical. The DSTD-711 automatically sets the motor on signal at the drive interface when the 5" mode has been loaded into the Mode Register.

Double sided drives make use of another set of bits in the Drive Select Register. To enable the second side of eight inch drives bit four is set to 0, to access the second side of five inch drives, bit five is set to 0. Table 2 - 3 below defines all bits used in the Drive Select Register.

TABLE 2 - 3
DRIVE SELECT REGISTER BIT DEFINITION
(Base Port + 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n/a	n/a	SS-5"	SS-8"	DS3	DS2	DS1	DS0

Where: SS-5" = 1 if side zero, 0 if side one wanted for 5-1/4" drives

SS-8" = 1 if side zero, 0 if side one wanted for 8" drives

DS0-1 = Drive select value as described in TABLE 2 - 2

The data written to the drive select register may not be read back directly. You should keep this data in RAM memory if it needs to be determined by your application program at a later time.

2.2.2 The Mode Register

The mode register is used to select the size and density of the drive to be used. Only two bits of the word written are interpreted. (This makes storage of four drives worth of information in a single byte possible; rotating this byte twice for each drive number will position the correct value in bits zero and one.)

Bit 0 sets the drive's size and bit 1 sets the density. A one selects either an eight inch or double density setting, a zero selects a five inch or single density setting. A complete word is described in TABLE 2 - 4 below.

TABLE 2 - 4
MODE WORD BIT DEFINITION

Drive 3	Drive 2	Drive 1	Drive 0
bits 7,6	bits 5,4	bits 3,2	bits 1,0
density!size	density!size	densty!size	density!size

As an example, suppose drive three was eight inch double density, drive two was five inch single density, drive one was five inch double density and drive zero was eight inch single density, the Mode Word, (which could be stored in memory,) would look like this:

11 00 10 01

This pattern could be fetched from memory when required and rotated twice for each drive (other than zero) that was to be set. If all the drives were the same, the mode register need only be set once. Keep in mind that on reset, the register contains 00, this would be interpreted as 5", single density.

2.3 DMA Section

The interrupt request line from the WD1797 is fed to the ready input of the DMA to signal when a byte is ready (or required) to be transferred to (or from) the DMA.

dy-4 SYSTEMS STD BUS Motherboards (and STD Modules with on-board DMA devices,) incorporate a multiple DMA feature that allows more than one DMA device to be used in the same system. This feature is important to note when configuring the DSTD-711 for operation in your system. If you are using a backplane which does not incorporate this capability, the information in Section 3 - 5 should be noted.

2.4 Dynamic RAM Section

The DSTD-711 includes 64K bytes of Dynamic Memory which can be enabled in 8K byte pages by writing a '1' to the appropriate bit of the Page Select Register. Likewise, loading a '0' into the Page Register bit disables the page. The Memory on the DSTD-711 is disabled after a reset or power-on. Table 2 - 5 below describes this feature.

TABLE 2 - 5

PAGE REGISTER BIT ASSIGNMENTS
Base Port + 7

Address Range								
	E000	C000	A000	8000	6000	4000	2000	C000
	FFFF	DFFF	BFFF	9FFF	7FFF	5FFF	3FFF	1FFF
BIT	7	6	5	4	3	2	1	0

2.5 Installation Guidelines

The ground reference for the DSTD-711 is taken from pins three and four and NOT from the auxilliary ground at pins 53 and 54 next to the +/-12v at pins 55 and 56. The user is urged to connect his +/-12v supply ground with the +5v supply ground at the source to avoid drifting. This condition will result in unreliable performance of the DSTD-711.

Pin one of the drive cable connector is located next to the card ejector. Reversing this connection will cause you much frustration. Since all the odd pins are grounded, a reversal of the cable brings all the active low logic lines (such as drive select, head load, write,) ACTIVE. Any drive with power on and diskette inserted will be 'erased' at the current track location. Before inserting a diskette in a newly configured system it is wise to close the door without a diskette inserted and observe the drive select-head load lamp. If it comes on, you have misinstalled the drive cable.

The cable used between the DSTD-711 and the drives is 50 wide for eight inch and 34 wide for five inch drives. In the case of five inch drives, the connector should be offset towards the pin 50 side of the header. For combination systems, 34 position edge connectors for five inch drives should be installed on that section of cable while 50 position connectors for eight inch drives are attached across the entire width of the cable. This cable should be kept as short as practical but in no event be longer than 5'.

The DSTD-711 is designed to control soft sector diskettes only, sector pulses presented at pin 24 from drives capable of using hard sector diskettes are not required and may cause unreliable performance. This trace should be cut on the drive if hard sector index pulses are generated by the drive.

Likewise, pins 48 and 50 present separated data and clock to the interface, (remember that pin 50 is sometimes used as the drive four select in systems with four drives.) The DSTD-711 utilizes an internal digital data separator and thus does not require these signals. These lines should be cut prior to connection to the DSTD-711.

With adequate voltage and the cable connected properly some simple tests may be run to see if the DSTD-711 is working in your system. Using a monitor program that is capable of writing to and reading from I/O ports, the following simple tests may be made. They assume that the DSTD-711 has been addressed at Base Port AOH and that an eight inch, single density diskette has been inserted in drive 0.

PORT READ/WRITE TEST

This simplest of tests should be run if there is any doubt that you have correctly addressed the card and can communicate with it.

3E0D	LD A,ODOH	MVI A,ODOH	GET 1797 RESET COMMAND IN A
D3A0	OUT PORT,A	OUT PORT	RESET 1797
DBA0	IN A,PORT	IN PORT	GET DATA FROM COMMAND REGISTER
DBA1	IN A,PORT+1	IN PORT+1	GET DATA FROM TRACK REGISTER
DBA2	IN A,PORT+2	IN PORT+2	GET DATA FROM SECTOR REGISTER
DBA3	IN A,PORT+3	IN PORT+3	GET DATA FROM DATA REGISTER

The values returned in the read/write registers should be:

0 for the command register
 0 for the track register
 1 for the sector register
 0 for the data register

By writing data into the track, sector and data registers and reading it back, you can be assured of a correct communication link.

RESTORE TEST

This code will load the head, restore the drive (place the head over track zero) and read the diskette to confirm track zero has been reached. (Assumes you are using a formatted, single sided, single density, eight inch diskette in drive zero.)

3E0D	LD A,ODOH	MVI A,ODOH	GET THE 1797 RESET COMMAND IN A
D3A0	OUT PORT,A	OUT PORT	SEND TO COMMAND REGISTER
3E01	LD A,1	MVI A,1	GET MODE VALUE READY, 8" SD
D3A6	OUT PORT+6,A	OUT PORT+6	SEND TO MODE REGISTER
3E0E	LD A,OEH	MVI A,OEH	GET DRIVE SELECT FOR DRIVE 0
D3A5	OUT PORT+5,A	OUT PORT+5	SEND TO DRIVE SELECT REGISTER
3E0A	LD A,OA H	MVI A,OA H	1797 CMND FOR RESTORE W/VERIFY
D3A0	OUT PORT,A	OUT PORT	SEND TO COMMAND REGISTER
DBA0	IN A,PORT	IN PORT	GET COMPLETION STATUS

You should notice the head load lamp and/or drive select lamp light after the last OUT operation. Also, if the head was not already on track zero, it should be stepped back until it gets there.

The A register should contain a 4 (bit 2 set) in the lower nibble to indicate that track zero has been reached. This register must be tested prior to the drive becoming deselected.

TRACK SEEK TEST

This last test involves getting the DSTD-711 to seek a track on the diskette. A bit in the command register will be set if a seek error occurred.

3ED0	LD A,0DOH	MVI A,0DOH	GET 1797 RESET COMMAND IN A
D3A0	OUT PORT,A	OUT PORT	SEND TO COMMAND REGISTER
3E01	LD A,1	MVI A,1	SET UP FOR MODE
D3A6	OUT PORT+6,A	OUT PORT+6	SET MODE, SINGLE DENSITY, 8"
3E0E	LD A,0EH	MVI A,0EH	SET UP FOR DRIVE 0
D3A5	OUT PORT+5,A	OUT PORT+5	SET DRIVE ZERO
3E0A	LD A,0AH	MVI A,0AH	SET UP RESTORE COMMAND
D3A0	OUT PORT,A	OUT PORT	RESTORE DRIVE
3E30	LD A,30H	MVI A,30H	SET UP FOR TRACK 48 (DECIMAL)
D3A3	OUT PORT+3,A	OUT PORT+3	PUT THIS VALUE IN THE DATA REG
3E1A	LD A,1AH	MVI A,1AH	GET SEEK COMMAND W/VERIFY
D3A0	OUT PORT,A	OUT PORT	SEND TO COMMAND REGISTER
DBA0	IN A,PORT	IN PORT	GET COMPLETION STATUS

You should notice the head load and seek track zero after the 0AH is sent to the command register and then load again and step out to track 48 after the 1AH is sent. The data from the command register (PORT) should be read first to be sure that no seek errors occurred. If there was an error, bit four (a one in the upper nibble) will be set. Next you should read from the track register (PORT+1) to see if the value there agrees with the value you put into the data register. (in this case 30H.)

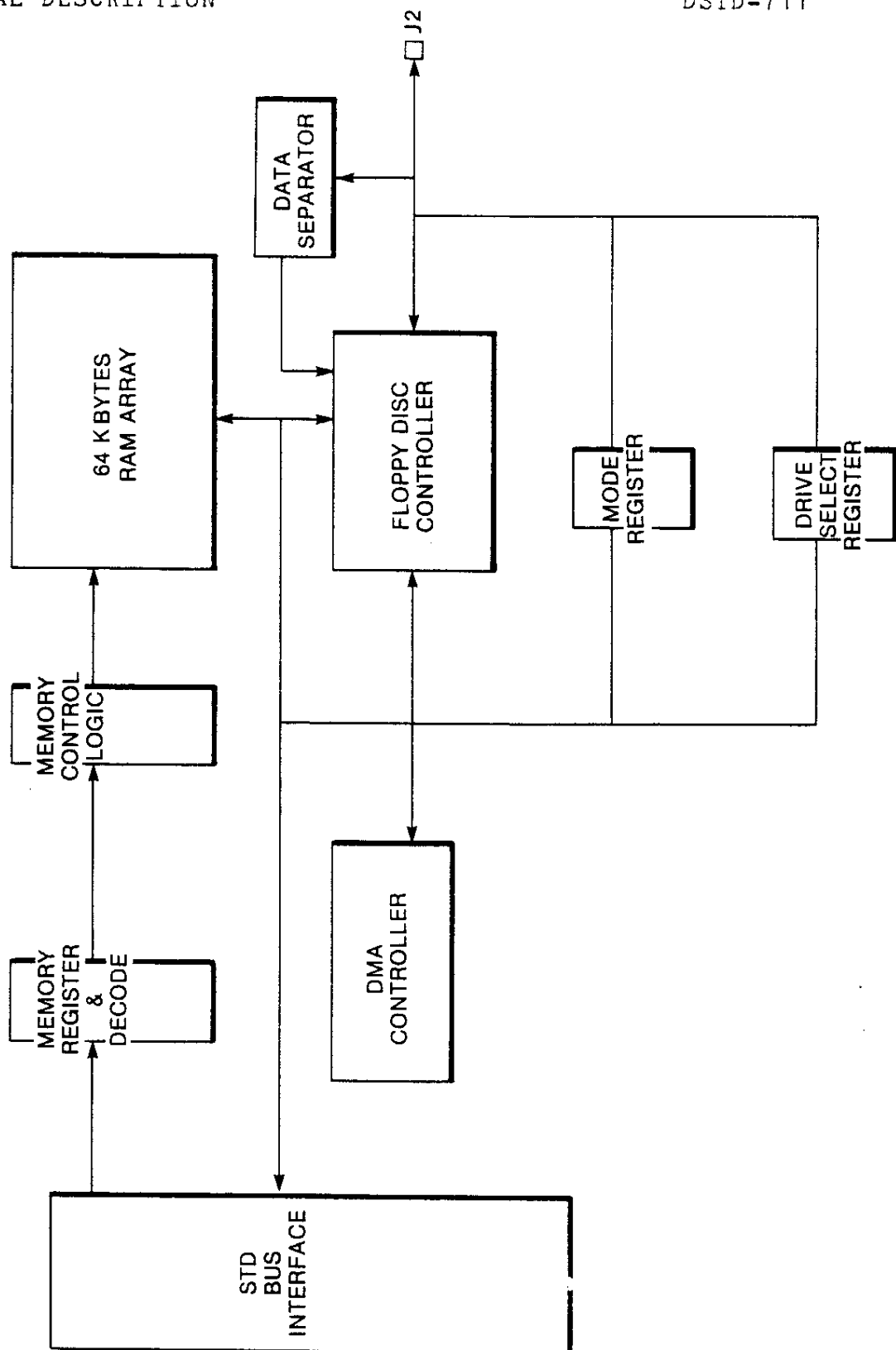


FIGURE 2-1 FUNCTIONAL BLOCK DIAGRAM

SECTION 3

3.0 OPTION PROGRAMMING

The DSTD-711 includes several user selectable options which must be configured prior to its use.

3.1 RAM Timing Selection - JB1

This factory set option selects memory timing for operation in either 2.5 or 4.0 MHz systems. Figure 3 - 1 below describes the two settings:

FIGURE 3 - 1
MEMORY TIMING OPTION

JB - 1		
	A	B
1	o	o
2	o	o
3	o	o
4	o	o

For 4.0 Mhz Operation: 1B - 1A, 3B - 4B
For 2.5 Mhz Operation: 2A - 1B, 3A - 4B

3.2 Test Jumper JB2

This is a test jumper used by the factory. It is normally left open.

3.3 I/O Port Address Selection JB3

The Base Port address of the DSTD-711 is selected at Jumper Block JB3. Only five address bits are provided because the on-board devices decode eight addresses internally. The Base Port is selected by setting an address at JB3 as described in Figure 3.- 2 below.

FIGURE 3 - 2
BASE PORT ADDRESS SELECTION

JB - 3

A	B	
2 o-----o		Compare with address bit 3
3 o-----o		Compare with address bit 4
4 o o		Compare with address bit 5
5 o-----o		Compare with address bit 6
6 o o		Compare with address bit 7

A '1' is set by leaving the jumper out

A '0' is set by connecting A - B

The factory setting is 0A0H, as shown.

3.4 Extend DMA Ready Input JB3 1A-1B

The DSTD-711 allows an option where an external Ready signal may be input to the DMA chip. This option is connected to pin 35 of the STD BUS via jumper block 3 pin 1A-1B. This option allows the DSTD-711 to work as a general purpose DMA controller with an external RDY connected to pin 35 of the STD BUS. Note that this pin is IOEXP*, hence if IOEXP* is used by the system the external DMA capabilities of the DSTD-711 cannot be used.

Figure 3 - 3

External DMA Ready Input

B o external ready signal

A o optional ready I/P to DMA controller

1

3.5 DMA Chain Selection JB4

The dy-4 SYSTEMS STD BUS definition incorporates a DMA chain capability which allows more than one DMA device to coexist in the same system. Many STD BUS backplanes cannot support multiple DMA devices and this feature must thus be disabled on the DSTD-711. Figure 3 - 4 describes this option.

FIGURE 3 - 4

DMA PRIORITY CHAIN OPTION
JB4

	A	B	
/BUSACK output	1 o	o	STD BUS trace 41
STD BUS trace 40	2 o	o	/BUSACK input

To operate the DSTD-711 with a dy-4 SYSTEMS' backplane, jumper 1A - 1B and 2A - 2B. To operate in other backplanes, jumper 1B - 2B only.

SECTION 4

4.0 SPECIFICATIONS

4.1 Function Specifications

4.1.1 Word Size

Data 8 bits
I/O address 8 bits

4.1.2 Memory Capacity

64K bytes

4.1.3 Memory Access Times

	Memory Access Time	Memory Cycle Time
DSTD-711-2.5	350 ns	465 ns
DSTD-711-4.0	200 ns	325 ns

4.1.4 I/O Port Addressing

The DSTD-711 occupies 8 contiguous I/O address. The base address is user selectable by JB3 (see Section 3).

4.2 Electrical Specifications

4.2.1 STD BUS Interface

Bus Inputs : one 74L load max.
Bus Outputs: I_{OL} 24 mA min @ V_{OL} 0.5 Volts
 I_{OH} 15 mA min @ V_{OH} 2.4 Volts

4.2.2 Operating Temperature

0 degrees Celsius to 60 degrees Celsius

4.2.3 Power Supply Requirements

+5VDC 5% @ 1.5 Amps Max
+12VDC 5% @ 0.05 Amps Max

4.3 Mechanical Specification

4.3.1 Card Dimensions

4.5 inches (11.43 cm.) wide by 6.50 inches (16.52 cm.) long
 0.48 inches (1.22 cm.) maximum height
 0.062 inches (0.16 cm.) printed circuit board thickness

4.3.2 STD BUS Edge Connector

56 Pin dual readout: 0.125 inch centers

4.3.3 Floppy Disk Mating Connector

Cable:

8" drives: Ansley 171-50: 50 conductor 28 AWG ribbon cable
 5" drives: Ansley 171-34: 34 conductor 28 AWG ribbon cable

Connectors for the DSTD-711:

8"- Ansley 609-5000M: 50 position female socket connector
 5"- Ansley 609-3400M: 34 position female socket connector

Connectors for standard Floppy Drives: (one each required per drive)

8"- Ansley 609-5015M: 50 position female card edge connector
 5"- Ansley 609-3415M: 34 position female card edge connector

SECTION 5

5.0 FACTORY NOTICES

5.1 Factory Repair Service

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. **THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL.** Enclose a letter containing the following information with the returned circuit board:

Name, address and phone number of purchaser
Date and place of purchase
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

dy-4 SYSTEMS INC.,
888 Lady Ellen Place,
Ottawa, Ontario
K1Z 5M1, Canada

Securely package and mail the circuit board, prepaid and insured, to the same address.

5.2 Limited Warranty

Dy-4 warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

NOTICE

The antistatic bag is provided for shipment of the dy-4 PC boards to prevent damage to the components due to electrostatic discharge.

Failure to use this bag in shipment will **VOID** the warranty.

APPENDIX A
OPTION JUMPER SUMMARY

APPENDIX A OPTION JUMPER SUMMARY

A-1

JB1	RAM Timing
JB2	Factory Test
JB3	I/O Base Address Select
JB4	dy-4/Mostek Backplane Select

A-2 RAM Timing (JB1)

o	o	o	--o	B	o	o	o	o	B
1					4MHz	\		/	2.5 MHz
o	o	o	o	A	o	o	o	o	A
1	2	3	4		1	2	3	4	

1A	20ns tap
1B	SELROW to address MUX
2A	40ns tap
2B	60ns tap
3A	80ns tap
3B	60ns tap
4A	100ns tap
4B	CASCLK to CAS gate

A-3 I/O Base Address Select (JB3)

B	o	o	o	o	o	o
A	o	o	o	o	o	o
	1	2	3	4	5	6

1A	optional ready I/P to DMA controller
1B	external ready signal (pin 35 of STD BUS)
2B	address 3
3B	address 4
4B	address 5
5B	address 6
6B	address 7
2A - 6A	ground

A-4

dy-4/Mostek Backplane Select

B	o	o		B	o--o	
	1	1	for dy-4	A	o	o
A	o	o			1	2
	1	2				

1A BAO from DSTD-711
1B BUSAK pin 41 on STD backplane [BAO on dy-4]
2A Status 0 pin 40 on STD backplane [BAI on dy-4]
2B BAI to DSTD-711

APPENDIX B
STD-Z80 BUS SIGNALS

APPENDIX B

STD-280 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	Ground - System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	Address Bus (Tri-state, output, active high).
13	D0	
14	D4	
15	A7	
16	A15	
17	A6	
18	A14	

STD-Z80 BUS PIN OUT

19	A5	A0-A15 make up a 16-bit address bus. The address bus provides the address for memory (up to 65k bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Memory Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Memory Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-State output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 Systems DSTD.

STD-Z80 BUS PIN OUT

36	/MEMEX	Memory expansion, not used on dy-4 Systems DSTD cards.
37	/REFRESH	/REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic zero and the upper 8 bits of the address bus contains the I register.
38	/DEBUG	/DEBUG (Input) used in conjunction with DDT-80 operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the /DEBUG line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
39	/M1	Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the opcode fetch cycle of an instruction. Note that during the execution of a 2-byte opcodes, /M1 will be generated as each opcode is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
40	STATUS 0	DMA priority chain input.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

STD-Z80 BUS PIN OUT

- 42 /BUSRQ Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.
- 43 /INTAK Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.
- 44 /INTRQ Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.
- 45 /WAITRQ WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

STD-Z80 BUS PIN OUT

46	/NMIRQ	Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will over-ride a /NMIRQ.
47	/SYSRESET	System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H and set Interrupt Mode 0.
48	/PBRESET	Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset.
49	/CLOCK	Processor Clock (Output, active low). Single phase system clock.
50	CNTRL	Auxiliary Timing
51	PCO	Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

STD-Z80 BUS PIN OUT

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.

APPENDIX C
PARTS LIST

APPENDIX C

PARTS LIST

DY00483-I-A1-2

QTY.	DESIGNATION	PART NUMBER
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INTEGRATED CIRCUITS

1	U35	74LS682
1	U30	74LS74
22	U29	SMC9216B
1	U28	DL100
6	U27,31-34,36	74LS245
1	U26	74S32
1	U23	74LS273
1	U22	PAL16L8
8	U14-21	4164-3
1	U13	WD2143-01
1	U12	WD1691
1	U11	K1116-8.0MHZ
1	U10	74LS393
1	U9	74LS257
1	U8	74LS04
1	U7	74LS123
1	U6	74LS244
1	U5	74LS374
2	U4,37	PAL12L6
1	U3	74LS240
1	U2	3883-DMA
1	U1	WD1797

PRINTED CIRCUIT BOARD

1	PCB	DY00483-H-A1-2
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RESISTORS

1	R7	330K 1/4W 5%
1	R6,8,9	10K 1/4W 5%
1	R5	2K 1/4W 5%
1	R4	1.2K 1/4W 5%
1	R3	2.2M 1/4W 5%
2	R1,2	220ohm 1/4W 5%
1	RN3	RNET 4.7K 10-PIN SIP
1	RN2	RNET 4.7K 6-PIN SIP
1	RN1	RNET 150 6-PIN SIP

CONNECTORS

1	JB4	CHD6902-W1S
1	JB3	CHD6906-W1S
1	JB1	CHD6904-W1S
1	JB2	CHS6902-W1S

CAPACITORS

1	C7	DG468Z474M
1	C1, 3-5, 8-10, 12-23, 25-29	R3134GZ104M
1	C6	CK058X330K
1	C11	TAG47M25
2	C2, 24	TAG10M25

DIODE

1	D1	1N4148
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TRANSISTOR

1	Q1	2N3906
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APPENDIX D
SCHEMATIC

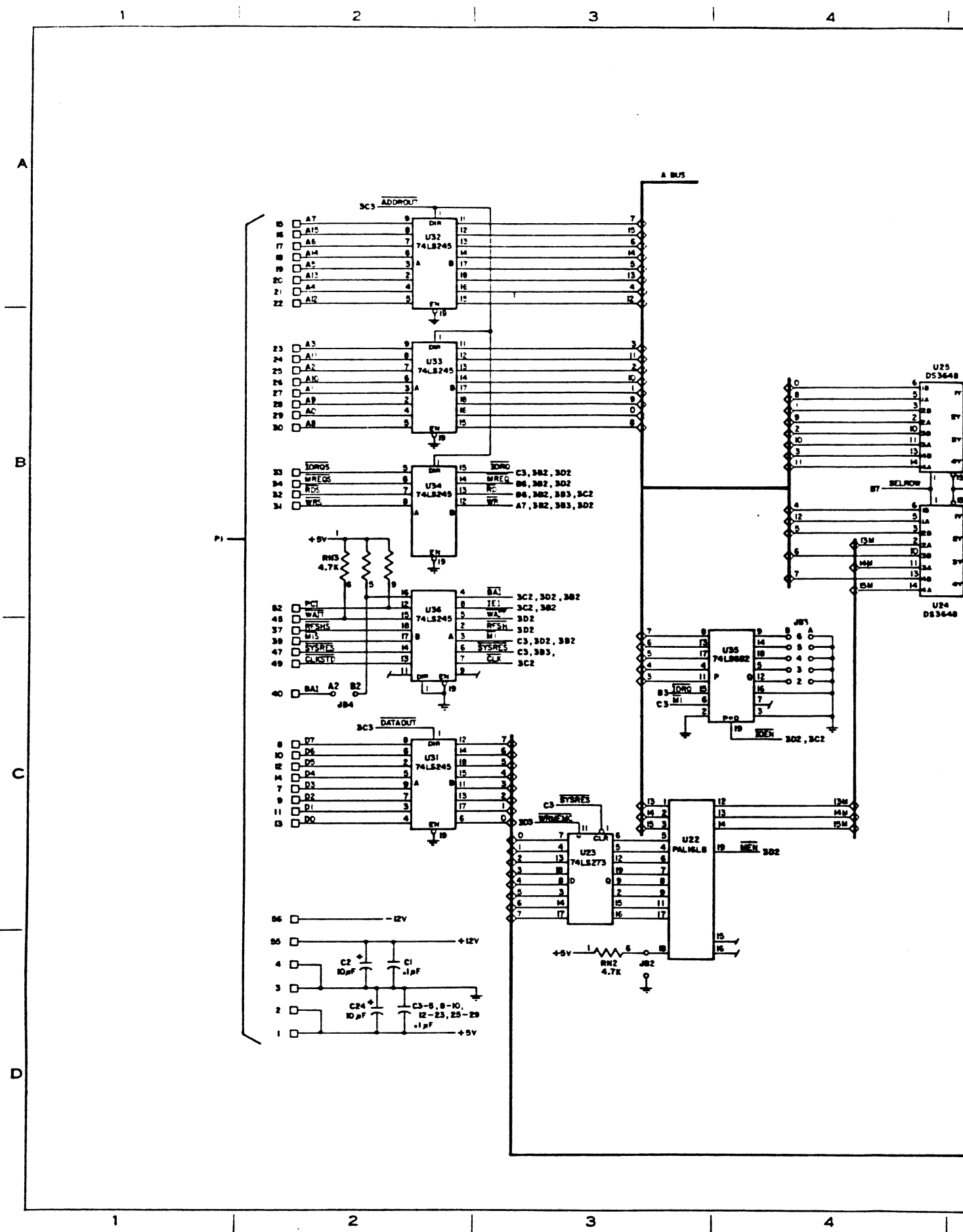
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49	1		RESISTOR FIXED COMP 330K 1/4W 5%	R7	
48	3		↑ ↑ ↑ 10K ↑ ↑	R6, 8, 9	
47	1		↑ ↑ ↑ 2K ↑ ↑	R5	
46	1		↑ ↑ ↑ 1.2K ↑ ↑	R4	
45	1		↑ ↑ ↑ 2.2M ↑ ↑	R3	
44	2		RESISTOR FIXED COMP 220 1/4W 5%	R1, 2	
43					
42	1		RESISTOR NETWORK 4.7K 10-PIN S.I.P.	RK3	
41	1		RESISTOR NETWORK 4.7K 6-PIN S.I.P.	RK2	
40	1		RESISTOR NETWORK 150 6-PIN S.I.P.	RK1	
39	1	CH06902-W15	CONNECTOR, 2x2 STRAIGHT HEADER	J84	
38	1	CH06906-W15	CONNECTOR, 2x6 STRAIGHT HEADER	J83	
37	1	CH06904-W15	CONNECTOR, 2x4 STRAIGHT HEADER	J81	
36	1	CHS6902-W15	CONNECTOR, 1x2 STRAIGHT HEADER	J82	
35					
34	1	DC468Z474M	CAPACITOR MONO .47UF	C7	
33	24	RS134G2104M	↑ CERAMIC 1UF 50V	C1, 3-5, 8-10, 12-23, 25-28	
32	1	CH058X330K	↓ CERAMIC 33pF	C6	
31	1	TAG47M25	↓ TANTALUM 47UF 25V	C11	
30	2	TAG10M25	CAPACITOR TANTALUM 10UF 25V	C2, 24	
29					
28	1	1N4148	DIODE	D1	
27					
26	1	2N3906	TRANSISTOR	Q1	
25	2	253648	INTEGRATED CIRCUIT	U24, 25	
24	1	74LS682	↑ ↑	U35	
23	1	74LS74		U30	
22	1	94C32168		U29	
21	1	DL100		DELAY LINE	U28
20	6	74LS245		U27, 31-34, 36	
19	1	74S32		U26	
18	1	74LS273		U23	
17	1	PAL16L8		U22	
16	3	4164-3		U14-21	
15	1	MC2143-01		U13	
14	1	MD1691		U12	
13	1	K1116-8.0MHZ		OSCILLATOR 8.0MHZ	U11
12	1	74LS393		U10	
11	1	74LS257		U9	
10	1	74LS04		U8	
9	1	74LS123		U7	
8	1	74LS244		U6	
7	1	74LS374		U5	
6	2	PAL12L6		U4, 37	
5	1	74LS240		U3	
4	1	2883-DMA	↑ ↓	J2	
3	1	MD1797	INTEGRATED CIRCUIT	J1	
2					
1			PRINTED CIRCUIT BOARD		
ITEM	QTY	PART NUMBER	DESCRIPTION	DESIGNATION	

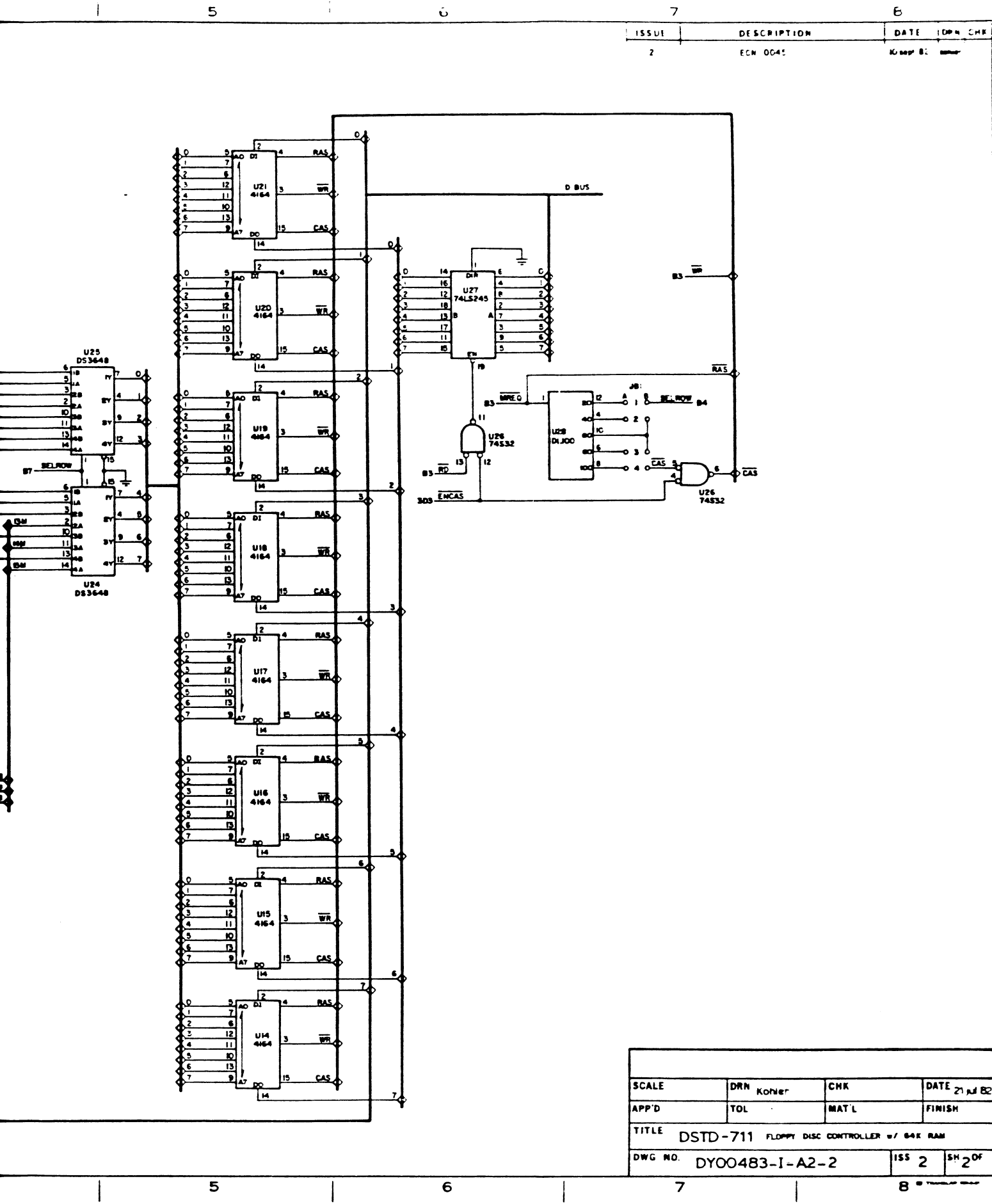
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ITEM	QTY

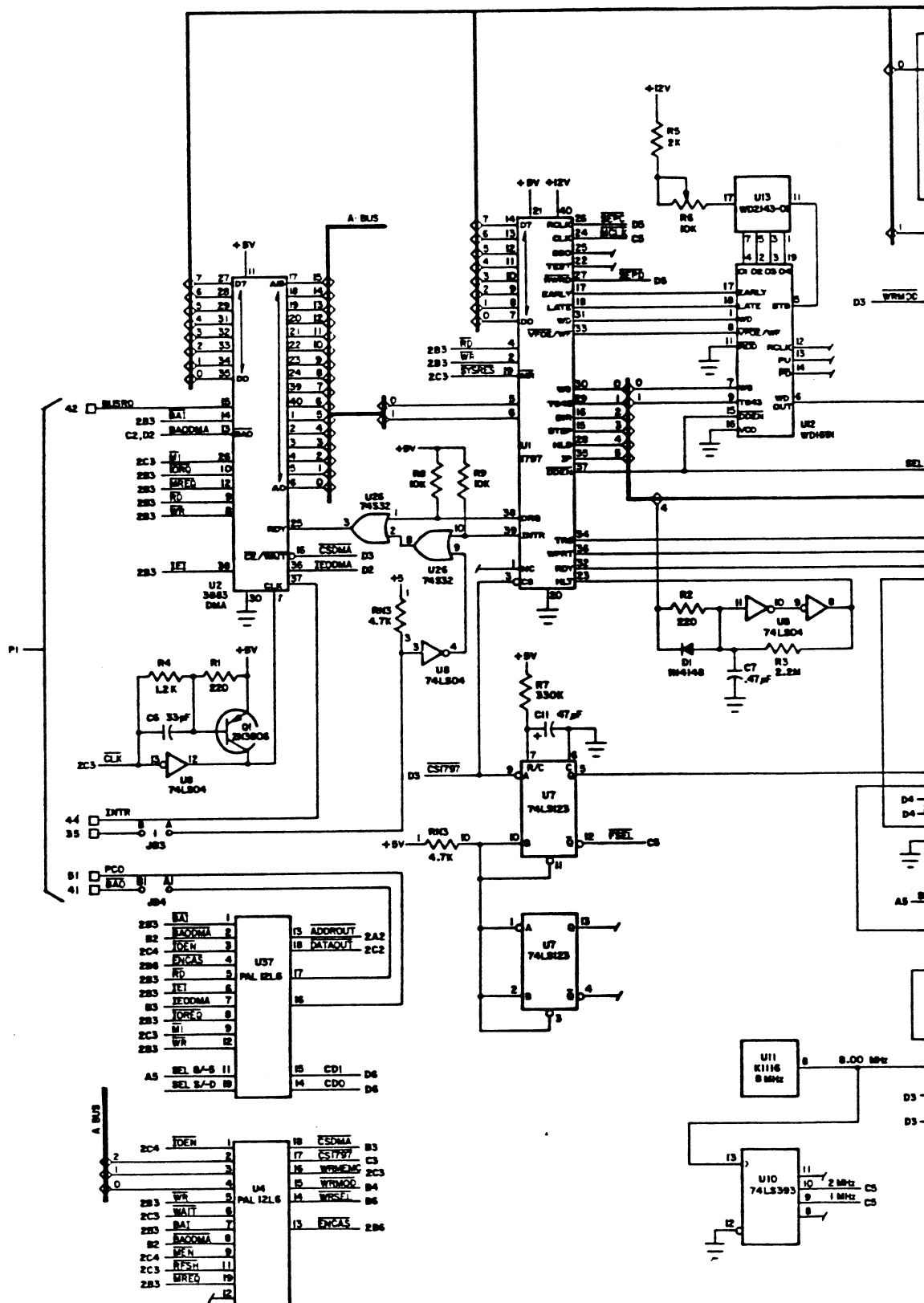
ISSUE	DESCRIPTION	DATE	DRN	CHK
2	ECN 0045	0 sept 52	homer	

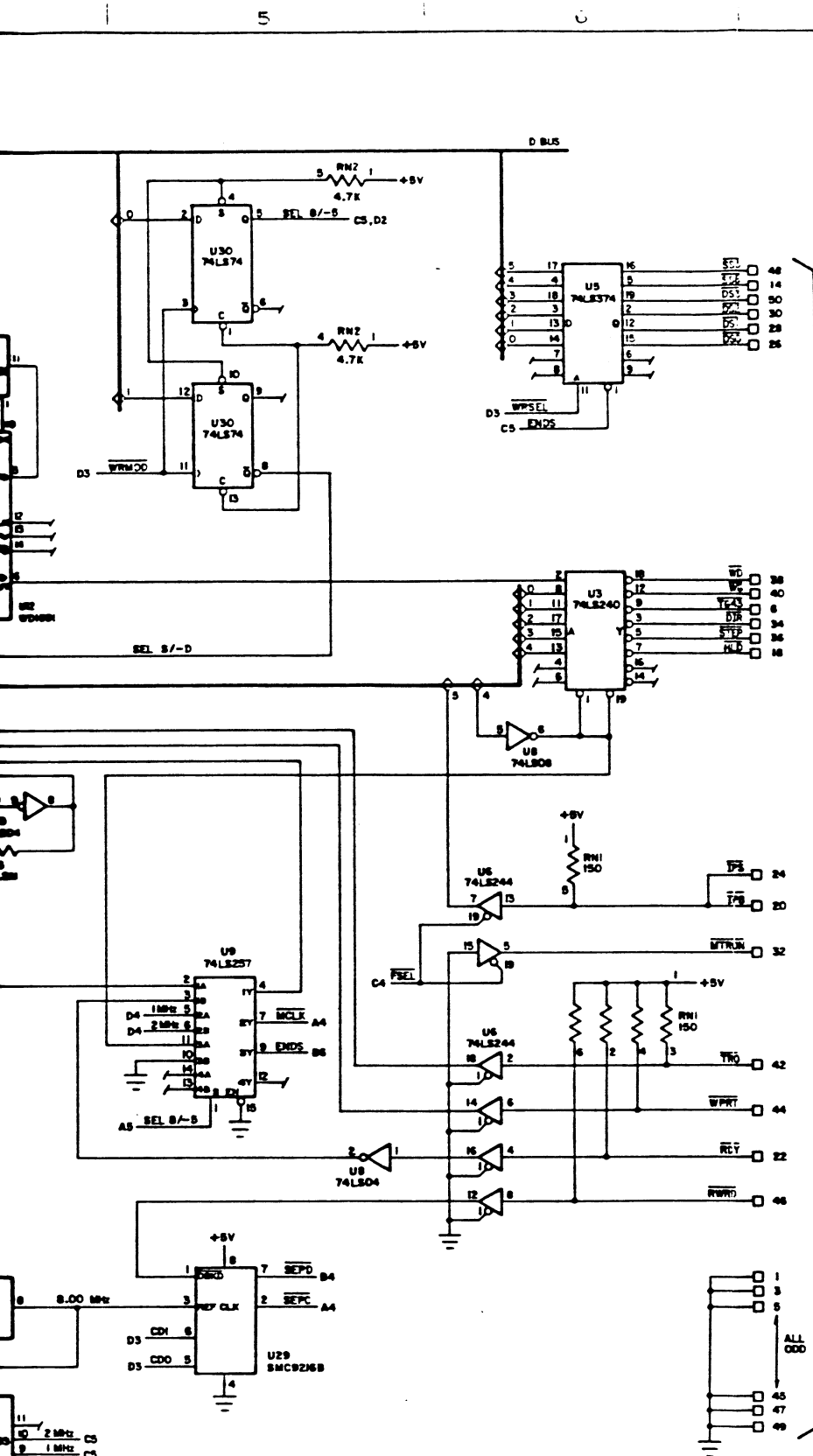
[illegible][illegible]

SCALE	DRN	CHK	DATE 5 aug 82
APP D	TOL	MAT L	FINISH
TITLE DSTD-711 FLOPPY DISC CONTROLLER w/ 64K RAM			
DWG NO DY00483-I-A1-2		ISS 2	OF 3









ISSUE	DESCRIPTION	DATE	OWN	CHK
2	ECN 0045	10 Sep 82	DRN	

SCALE	DRN Kohler	CHK	DATE 21 Jul 82
APP'D	TOL	MAT'L	FINISH
TITLE DSTD-711 FLOPPY DISC CONTROLLER w/ 64K RAM			
DWG NO. DY00483-I-A3-2	ISS 2	SH 3 OF	

APPENDIX E
WD1797 DATA SHEET

FD 179X-02 Floppy Disk Formatter/Controller Family

FEATURES

- TWO VFO CONTROL SIGNALS
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
 - IBM 3740 Single Density (FM)
 - IBM System 34 Double Density (MFM)
- READ MODE
 - Single/Multiple Sector Read with Automatic Search or Entire Track Read
 - Selectable 128 Byte or Variable length Sector
- WRITE MODE
 - Single/Multiple Sector Write with Automatic Sector Search
 - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
 - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
 - DMA or Programmed Data Transfers
 - All inputs and Outputs are TTL Compatible
 - On-Chip Track and Sector Registers/Comprehensive Status Information

- PROGRAMMABLE CONTROLS
 - Selectable Track to Track Stepping Time
 - Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

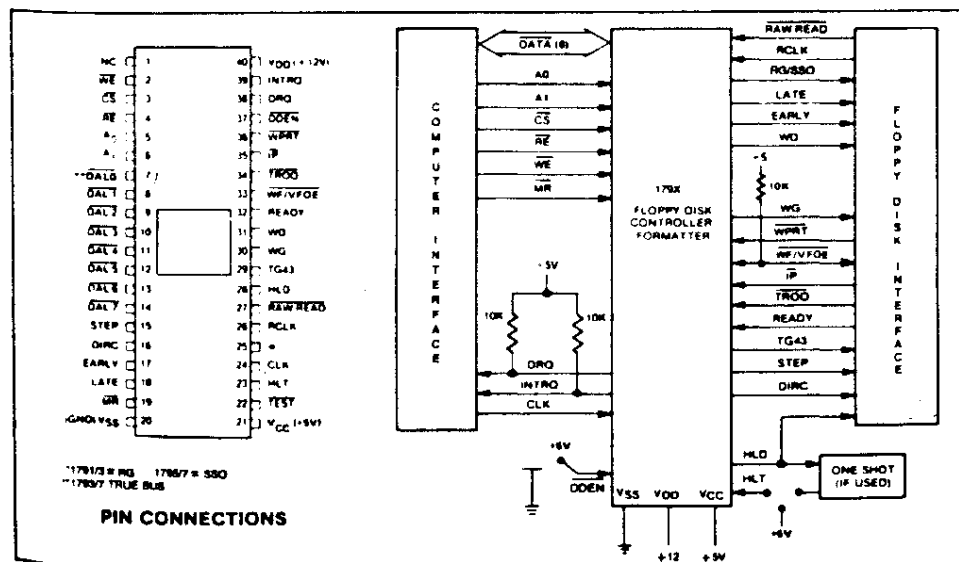
179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1793	1795	1797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Write Precomp	X	X	X	X
Side Selection Output			X	X

APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/
FORMATTER
NEW MINI-FLOPPY CONTROLLER

MAY 1980



FD179X SYSTEM BLOCK DIAGRAM

GENERAL DESCRIPTION

The FD179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load

control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793. On these devices, DDEN must be left open.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION																				
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.																				
19	<u>MASTER RESET</u>	<u>MR</u>	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during <u>MR</u> ACTIVE. When <u>MR</u> is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.																				
20	POWER SUPPLIES	V _{ss}	Ground																				
21		V _{cc}	+5V ±5%																				
40		V _{dd}	+12V ±5%																				
COMPUTER INTERFACE:																							
2	<u>WRITE ENABLE</u>	<u>WE</u>	A logic low on this input gates data on the DAL into the selected register when <u>CS</u> is low.																				
3	<u>CHIP SELECT</u>	<u>CS</u>	A logic low on this input selects the chip and enables computer communication with the device.																				
4	<u>READ ENABLE</u>	<u>RE</u>	A logic low on this input controls the placement of data from a selected register on the DAL when <u>CS</u> is low.																				
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under <u>RE</u> and <u>WE</u> control: <table><tr><td>A1</td><td>A0</td><td><u>RE</u></td><td><u>WE</u></td></tr><tr><td>0</td><td>0</td><td>Status Reg</td><td>Command Reg</td></tr><tr><td>0</td><td>1</td><td>Track Reg</td><td>Track Reg</td></tr><tr><td>1</td><td>0</td><td>Sector Reg</td><td>Sector Reg</td></tr><tr><td>1</td><td>1</td><td>Data Reg</td><td>Data Reg</td></tr></table>	A1	A0	<u>RE</u>	<u>WE</u>	0	0	Status Reg	Command Reg	0	1	Track Reg	Track Reg	1	0	Sector Reg	Sector Reg	1	1	Data Reg	Data Reg
A1	A0	<u>RE</u>	<u>WE</u>																				
0	0	Status Reg	Command Reg																				
0	1	Track Reg	Track Reg																				
1	0	Sector Reg	Sector Reg																				
1	1	Data Reg	Data Reg																				
7-14	<u>DATA ACCESS LINES</u>	<u>DAL0-DAL7</u>	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by <u>WE</u> or transmitter enabled by <u>RE</u> .																				
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for mini-drives.																				

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.
25	READ GATE (1791/3)	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S = 1, SSO is set to a logic 1. When S = 0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE FAULT VFO ENABLE	WF/VFOE	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field.
34	TRACK 00	TR00	This input informs the FD179X that the Read/Write head is positioned over Track 00.
35	INDEX PULSE	IP	This input informs the FD179X when the index hole is encountered on the diskette.
36	WRITE PROTECT	WPRT	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	DDEN	This pin selects either single or double density operation. When DDEN = 0, double density is selected. When DDEN = 1, single density is selected. This line must be left open on the 1792/4

ORGANIZATION

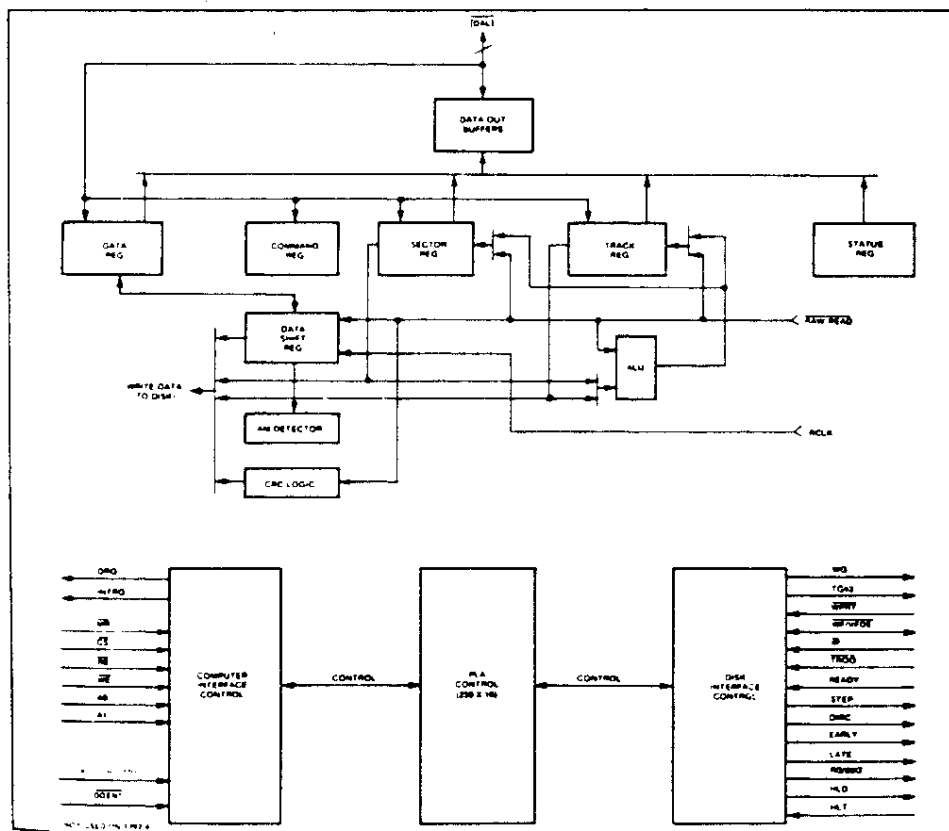
The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register—This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.



FD179X BLOCK DIAGRAM

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791/3 has two different modes of operation according to the state of DDEN. When DDEN = 0 double density (MFM) is assumed. When DDEN = 1, single density (FM) is assumed.

AM Detector—The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD179X. The DAL are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (\overline{RE}) are active (low logic state) or act as input receivers when CS and Write Enable (\overline{WE}) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The address bits A1 and A0, combined with the signals \overline{RE} during a Read operation or \overline{WE} during a Write operation are interpreted as selecting the following registers:

A1-A0	READ (\overline{RE})	WRITE (\overline{WE})
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The 179X has two modes of operation according to the state of DDEN (Pin 37). When DDEN = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

HEAD POSITIONING

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If TEST = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 μ s (MFM) or 4 μ s (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μ s before the first stepping pulse is generated.

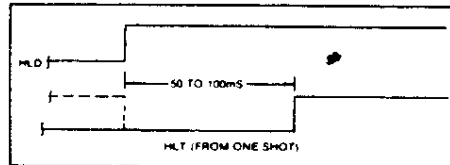
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

Table 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
DDEN	0	1	0	1	X	X
A1 A0	TEST=1	TEST=1	TEST=1	TEST=1	TEST=0	TEST=0
0 0	3 ms	3 ms	6 ms	6 ms	184 μ s	368 μ s
0 1	6 ms	6 ms	12 ms	12 ms	190 μ s	380 μ s
1 0	10 ms	10 ms	20 ms	20 ms	196 μ s	396 μ s
1 1	15 ms	15 ms	30 ms	30 ms	208 μ s	416 μ s

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of a Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if $h = 0$ and $V = 0$, HLD is reset. If $h = 1$ and $V = 0$, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If $h = 0$ and $V = 1$, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If $h = 1$ and $V = 1$, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, DDEN should be placed to logical "1." For MFM formats, DDEN should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table.)

For read operations, the FD179X requires RAW READ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be

derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations ($WG = 0$), the \overline{VFOE} (Pin 33) is provided for phase lock loop synchronization. \overline{VFOE} will go active when:

- Both HLT and HLD are True
- Settling Time, if programmed, has expired
- The 179X is inspecting data off the disk

If $\overline{WF}/\overline{VFOE}$ is not used, leave open or tie to a 10K resistor to +5.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($DDEN = 1$) and 250 ns pulses in MFM ($DDEN = 0$). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

Table 2 COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	h	V	r ₁	r ₀	
I	Seek	0	0	0	1	h	V	r ₁	r ₀
I	Step	0	0	1	u	h	V	r ₁	r ₀
I	Step In	0	1	0	u	h	V	r ₁	r ₀
I	Step Out	0	1	1	u	h	V	r ₁	r ₀
II	Read Sector	1	0	0	m	F ₂	E	F ₁	0
II	Write Sector	1	0	1	m	F ₂	E	F ₁	a ₀
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	i ₃	i ₂	i ₁	i ₀

Note: Bits shown in TRUE form.

Table 3 FLAG SUMMARY

TYPE I COMMANDS	
<u>h = Head Load Flag (Bit 3)</u>	
h = 1, Load head at beginning	
h = 0, Unload head at beginning	
<u>V = Verify flag (Bit 2)</u>	
V = 1, Verify on destination track	
V = 0, No verify	
<u>r₁r₀ = Stepping motor rate (Bits 1-0)</u>	
Refer to Table 1 for rate summary	
<u>u = Update flag (Bit 4)</u>	
u = 1, Update Track register	
u = 0, No update	

Table 4 FLAG SUMMARY

TYPE II & III COMMANDS

m = Multiple Record flag (Bit 4)

m = 0, Single Record

m = 1, Multiple Records

a₀ = Data Address Mark (Bit 0)

a₀ = 0, FB (Data Mark)

a₀ = 1, FB (Deleted Data Mark)

E = 15 ms Delay (2MHz)

E = 1, 15 ms delay

E = 0, no 15 ms delay

(F₂) S = Side Select Flag (1791/3 only)

S = 0, Compare for Side 0

S = 1, Compare for Side 1

(F₁) C = Side Compare Flag (1791/3 only)

C = 0, disable side select compare

C = 1, enable side select compare

(F₁) S = Side Select Flag

(Bit 1, 1795/7 only)

S = 0 Update SSO to 0

S = 1 Update SSO to 1

(F₂) b = Sector Length Flag

(Bit 3, 1975/7 only)

	Sector Length Field			
	00	01	10	11
b = 0	256	512	1024	128
b = 1	128	256	512	1024

Table 5 FLAG SUMMARY

TYPE IV COMMAND	
<u>i₃ = Interrupt Condition flags (Bits 3-0)</u>	
i ₀ = 1, Not-Ready to Ready Transition	
i ₁ = 1, Ready to Not-Ready Transition	
i ₂ = 1, Index Pulse	
i ₃ = 1, Immediate Interrupt	
i ₃ -i ₀ = 0, Terminate with no Interrupt	

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r₁r₀), which determines the stepping motor rate as defined in Table 1.

The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If $h = 1$, the head is loaded at the beginning of the command (HLD output is made active). If $h = 0$, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD179X receives a command that specifically disengages the head. If the FD179X is idle ($\text{busy} = 0$) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

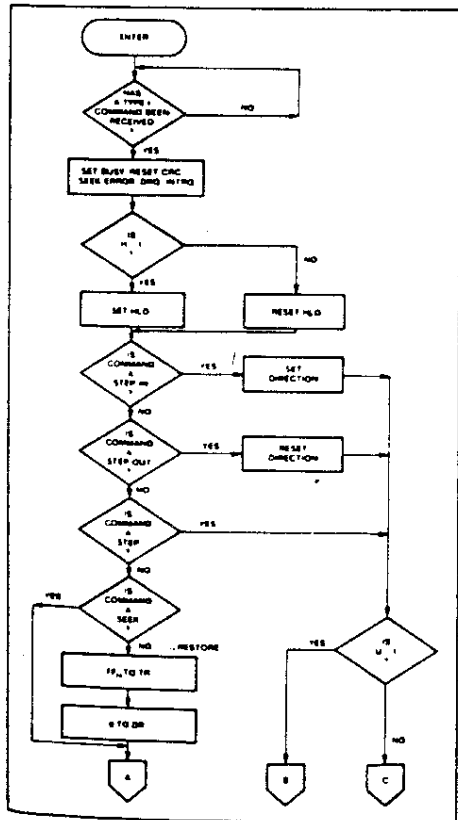
The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If $V = 1$, a verification is performed, if $V = 0$, no verification is performed.

During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the

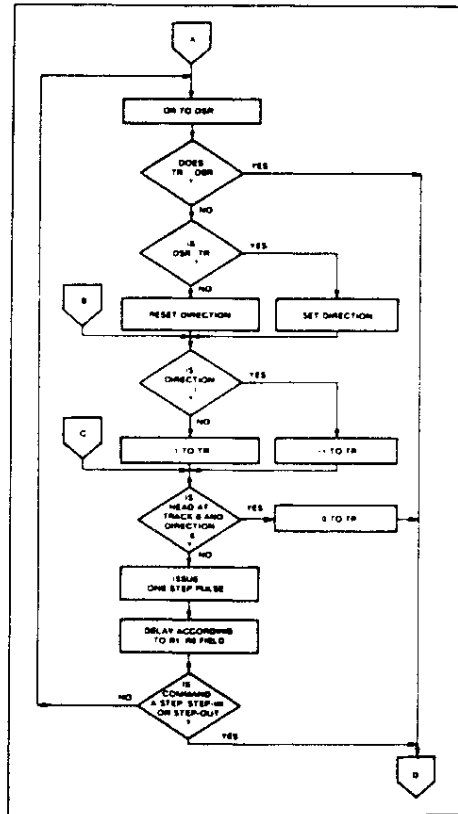
ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FD179X terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When $U = 1$, the track register is updated by one for each step. When $U = 0$, the track register is not updated.

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.



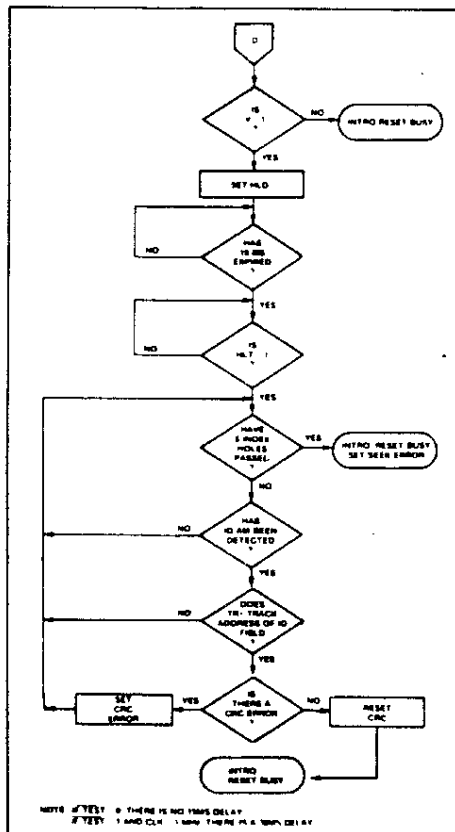
TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{\text{TROO}}$) input is sampled. If $\overline{\text{TROO}}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{\text{TROO}}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_{16} field are issued until the $\overline{\text{TROO}}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{\text{TROO}}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{\text{MR}}$ goes from an active to an inactive state.



TYPE I COMMAND FLOW

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_{16} field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_{16} field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r_{16} field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next en-

```

graph TD
    START([START]) --> IS_COMMAND[IS TYPE 0 COMMAND RECEIVED?]
    IS_COMMAND -- NO --> IS_COMMAND
    IS_COMMAND -- YES --> SET_BUSY[SET BUSY, RESET DRG, LOST DATA ACCORDING TO HOLDING & STATUS BITS & & INTRQ]
    SET_BUSY --> IS_DRG_READY[IS DRG READY?]
    IS_DRG_READY -- NO --> INTRQ_RESET_BUSY([INTRQ RESET BUSY])
    INTRQ_RESET_BUSY --> IS_DRG_READY
    IS_DRG_READY -- YES --> COPY_PLD[COPY 5 PLD TO SRD LINE 11 (PLD ONLY)]
    COPY_PLD --> SET_HOLD[SET HOLD]
    SET_HOLD --> IS_E1[IS E-1?]
    IS_E1 -- NO --> IS_E1
    IS_E1 -- YES --> SEE_NOTE[SEE NOTE]
    SEE_NOTE --> IS_MSR[IS MSR LURNED?]
    IS_MSR -- NO --> IS_MSR
    IS_MSR -- YES --> IS_HLT_T1[IS HLT-1?]
    IS_HLT_T1 -- NO --> IS_HLT_T1
    IS_HLT_T1 -- YES --> IS_TR_43[IS TR > 43?]
    IS_TR_43 -- YES --> SET_TG43[SET TG43]
    SET_TG43 --> RESET_TONG[RESET TONG]
    RESET_TONG --> IS_WRITE_PROTECT[IS WRITE PROTECT ON?]
    IS_WRITE_PROTECT -- YES --> INTRQ_RESET_BUSY_WRITE([INTRQ, RESET BUSY, SET WRITE PROTECT])
    INTRQ_RESET_BUSY_WRITE --> IS_WRITE_PROTECT
    IS_WRITE_PROTECT -- NO --> IS_COMMAND_WRITE[IS COMMAND A WRITE?]
    IS_COMMAND_WRITE -- YES --> IS_COMMAND_WRITE
    IS_COMMAND_WRITE -- NO --> END([END])
  
```

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

```

graph TD
    Start([1]) --> D1{SINCE X NO LBS PASSED}
    D1 -- YES --> R1([RYING, RESET BUZY SET RECORD-NOT FOUND])
    D1 -- NO --> D2{HAS COMMAND BEEN DETECTED}
    D2 -- NO --> D1
    D2 -- YES --> D3{DOES TR - TRACK ADDRESS OF ID FIELD}
    D3 -- NO --> D1
    D3 -- YES --> D4{DOES SR - SECTOR ADDRESS OF ID FIELD}
    D4 -- NO --> D1
    D4 -- YES --> D5{DOES S - SIDE NO OF ID FIELD}
    D5 -- NO --> D1
    D5 -- YES --> P1[SPRING IN SECTOR LENGTH FIELD STORE LENGTH IN INTERNAL REGISTER]
    P1 --> D6{IS THERE A CRC ERROR}
    D6 -- YES --> R2[SET CRC STATUS ERROR]
    R2 --> D1
    D6 -- NO --> D7{IS COMMAND A WRITE}
    D7 -- YES --> End1([3])
    D7 -- NO --> R3[RESET CRC]
    R3 --> D6
    End2([2]) --> D6
  
```

TYPE II COMMAND

ter exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

The Type II commands also contain side select compare flags. When C = 0, no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

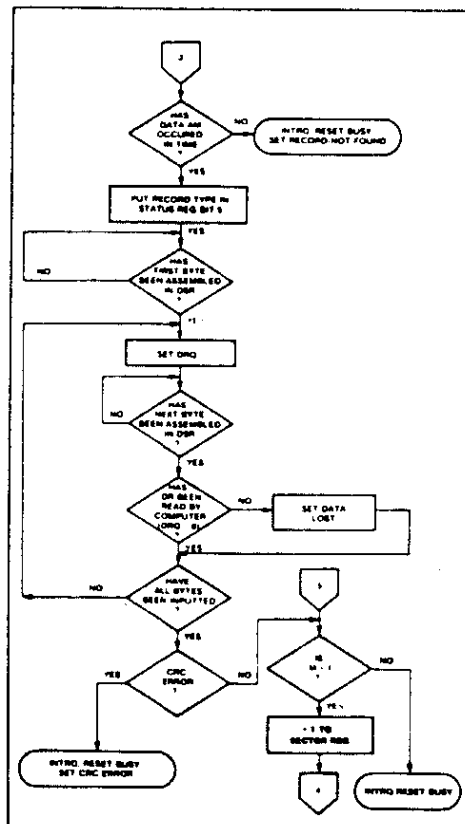
The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'b' flag should be set to a one. The

's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

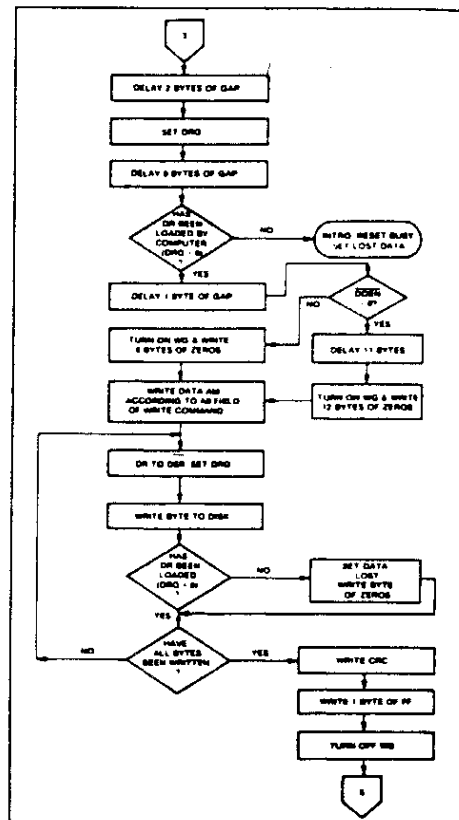
READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and



TYPE II COMMAND



TYPE II COMMAND

the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the *aa* field of the command as shown below:

<i>aa</i>	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The

next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

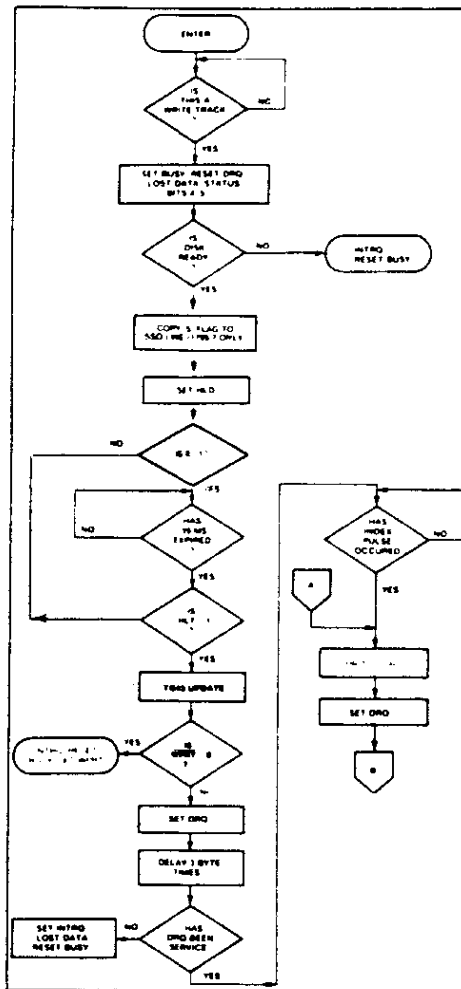
Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

WRITE TRACK

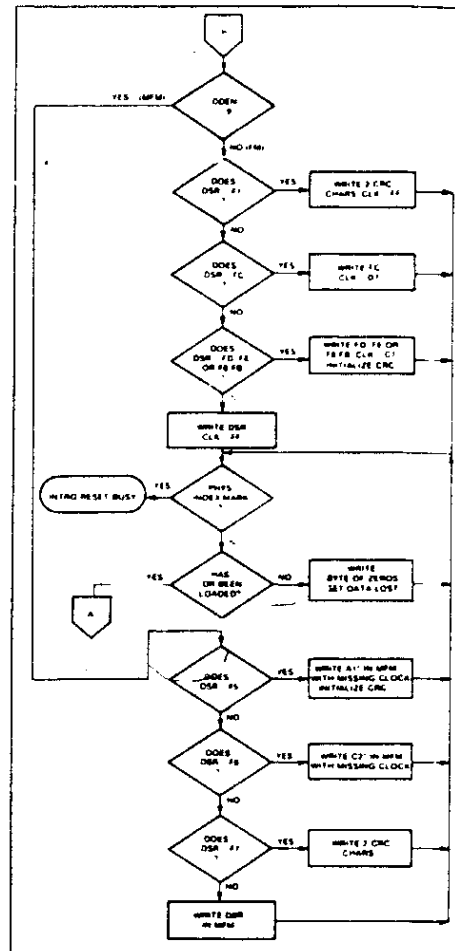
Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRG generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.



TYPE III COMMAND WRITE TRACK



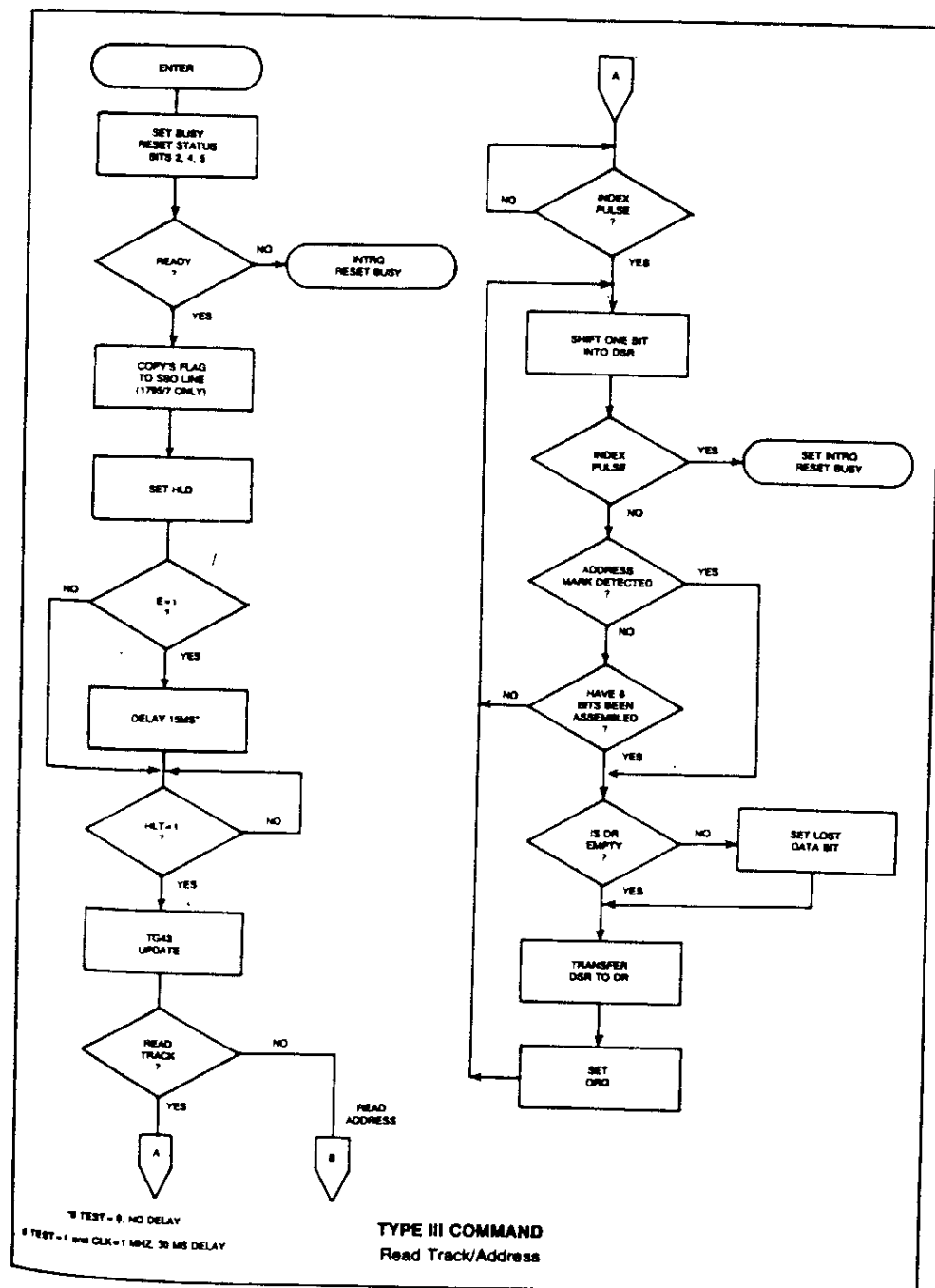
TYPE III COMMAND WRITE TRACK

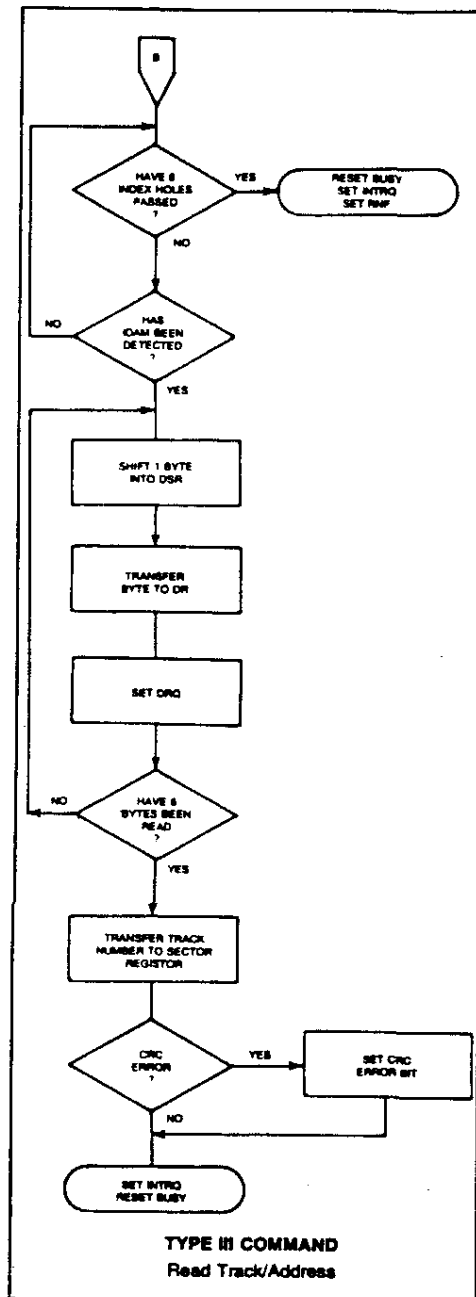
CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM (DDEN = 1)	FD1791/3 INTERPRETATION IN MFM (DDEN = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5

**Missing clock transition between bits 3 & 4





TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition

I_1 = Ready-To-Not-Ready Transition

I_2 = Every Index Pulse

I_3 = Immediate Interrupt (requires reset, see Note)

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. This is the only command that will enable the immediate interrupt to clear on a subsequent Load Command Register or Read Status Register.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

(Refer to section on Type III commands for flow diagrams.)

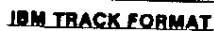
Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

*Write bracketed field 26 times

****Continue writing until FD179X interrupts out.
Approx. 247 bytes.**

1-Optional '00' on 1795/7 only.



IBM SYSTEM 34 FORMAT- 256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6
1	FC (Index Mark)
50*	4E
12	00
3	F5
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01
1	F7 (2 CRCs written)
22	4E
12	00
3	F5
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

* Write bracketed field 26 times
 **Continue writing until FD179X interrupts out. Approx. 598 bytes.

1. NON-IBM FORMATS

Variations in the IBM format are possible to a limited extent if the following requirements are met: sector size must be a choice of 128, 256, 512, or 1024 bytes; gap size must be according to the following table. Note that the Index Mark is not required by the 179X. The minimum gap sizes shown are that which is required by the 179X, with PLL lock-up time, motor speed variation, etc., adding additional bytes.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
"	6 bytes 00	12 bytes 00 3 bytes A1
Gap III	10 bytes FF	24 bytes 4E 3 bytes A1
**	4 bytes 00	8 bytes 00
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.

**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground) = 15 to -0.3V

Max. Voltage to Any Input With Respect to V_{SS} = 15 to -0.3V

Operating Temperature

0°C to 70°C

Storage Temperature

-55°C to +125°C

V_{DD} = 10 ma Nominal V_{CC} = 35 ma Nominal

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{DD} = + 12V \pm .6V, V_{SS} = 0V, V_{CC} = + 5V \pm .25V

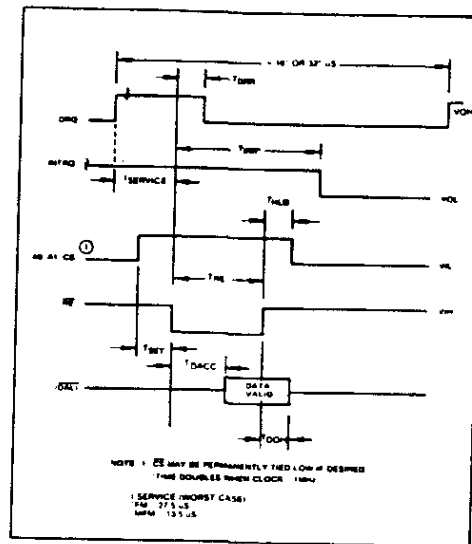
SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I_L	Input Leakage		10	μA	$V_{in} = V_{DD}$
I_{OL}	Output Leakage		10	μA	$V_{out} = V_{DD}$
V_{IH}	Input High Voltage	2.6		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.8		V	$I_o = -100 \mu A$
V_{OL}	Output Low Voltage		0.45	V	$I_o = 1.6 mA$
P_D	Power Dissipation		0.5	W	

TIMING CHARACTERISTICS

$T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{DD} = +12\text{V} \pm .6\text{V}$, $V_{SS} = 0\text{V}$, $V_{CC} = +5\text{V} \pm .25\text{V}$

READ ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{\text{RE}}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{\text{RE}}$	10			nsec	
TRE	$\overline{\text{RE}}$ Pulse Width	400			nsec	$C_L = 50\text{ pf}$
TDRR	DRQ Reset from $\overline{\text{RE}}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{\text{RE}}$		500	3000	nsec	See Note 5
TDACC	Data Access from $\overline{\text{RE}}$			350	nsec	$C_L = 50\text{ pf}$
TDOH	Data Hold From $\overline{\text{RE}}$	50		150	nsec	$C_L = 50\text{ pf}$



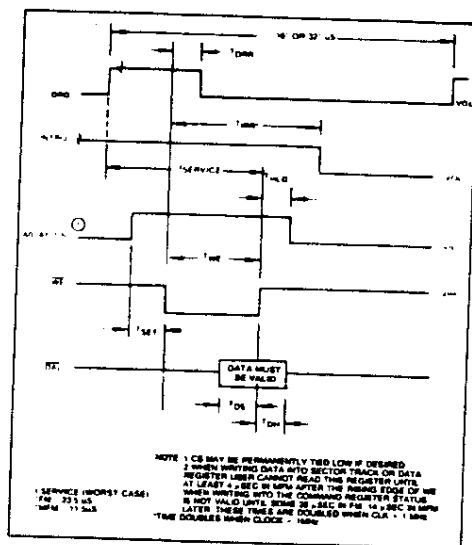
READ ENABLE TIMING

WRITE ENABLE TIMING

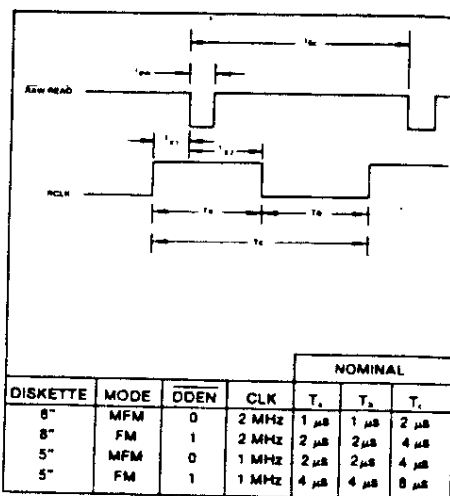
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to \overline{WE}	50			nsec	See Note 5
THLD	Hold ADDR & CS from \overline{WE}	10			nsec	
TWE	\overline{WE} Pulse Width	350			nsec	
TDRR	DRQ Reset from \overline{WE}		400	500	nsec	
TIRR	INTRQ Reset from \overline{WE}		500	3000	nsec	
TDS	Data Setup to \overline{WE}	250			nsec	
TDH	Data Hold from \overline{WE}	70			nsec	

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Tpw	Raw Read Pulse Width	100	200		nsec	See Note 1
tbc	Raw Read Cycle Time		1500		nsec	1800 ns @ 70°C
Tc	RCLK Cycle Time		1500		nsec	1800 ns @ 70°C
Tx ₁	RCLK hold to Raw Read	40			nsec	See Note 1
Tx ₂	Raw Read hold to RCLK	40			nsec	



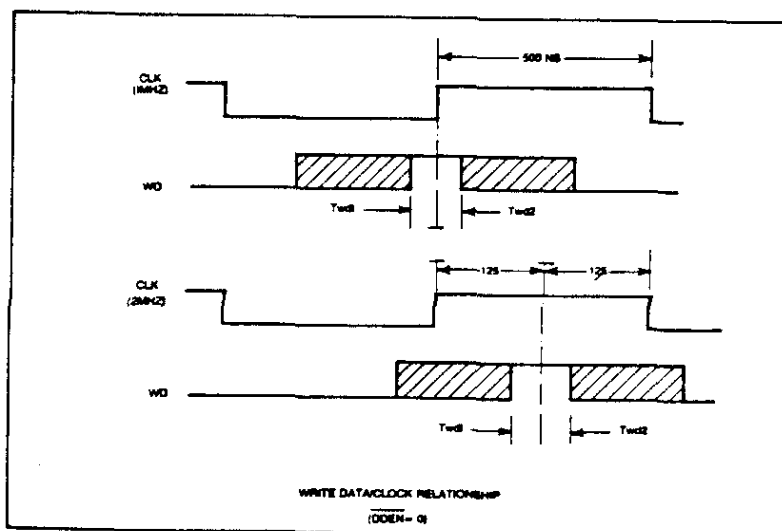
WRITE ENABLE TIMING



INPUT DATA TIMING

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz)

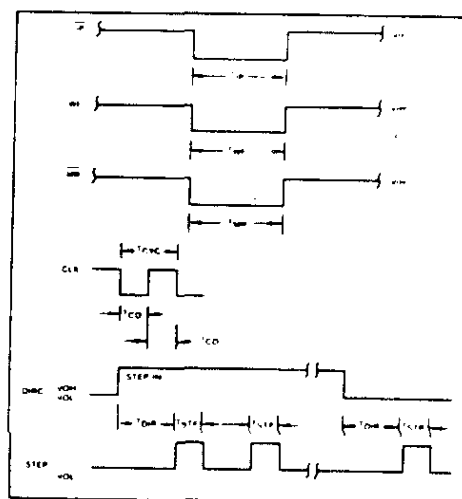
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width	450	500	550	nsec	FM
Twg	Write Gate to Write Data	150	200	250	nsec	MFM
Tbc	Write data cycle Time		2		μsec	FM
Ts	Early (Late) to Write Data		1		μsec	MFM
Th	Early (Late) From Write Data	125	2.3, or 4		μsec	± CLK Error
Twf	Write Gate off from WD	125			nsec	MFM
Twf	Write Gate off from WD		2		μsec	FM
Twf	Write Gate off from WD		1		μsec	MFM
Twcl	WD Valid to Clk	100			nsec	CLK = 1 MHZ
Twcl	WD Valid to Clk	50			nsec	CLK = 2 MHZ
Twcl2	WD Valid after CLK	100			nsec	CLK = 1 MHZ
Twcl2	WD Valid after CLK	30			nsec	CLK = 2 MHZ



WRITE DATA TIMING

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD ₁	Clock Duty (low)	230	250	20000	nsec	See Note 5 ± CLK ERROR
TCD ₂	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			μsec	
TD:R	Dir Setup to Step		12		μsec	
TMR	Master Reset Pulse Width	50			μsec	See Note 5
TIP	Index Pulse Width	10			μsec	
TWF	Write Fault Pulse Width	10			μsec	



MISCELLANEOUS TIMING

NOTES:

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2 μs, nominal in MFM and 4 μs nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during RAW READ (Polarity is unimportant).
5. Times double when clock = 1 MHz.

Table 6 STATUS REGISTER SUMMARY

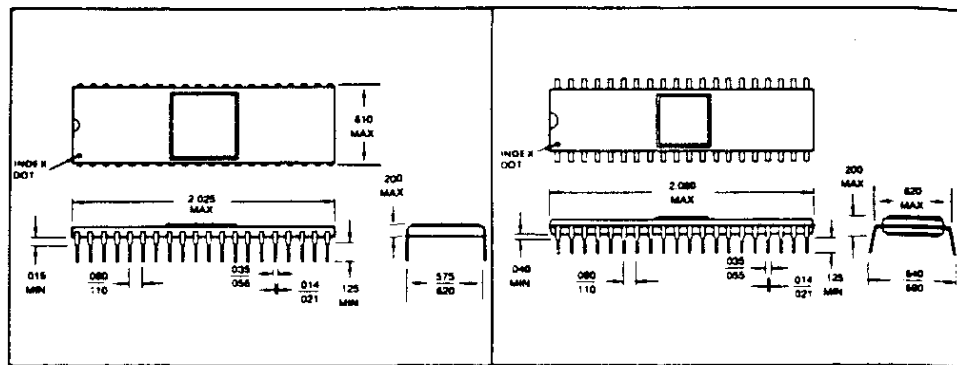
BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the TROO input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.



FD179XA-02 CERAMIC PACKAGE

FD179XB-02 PLASTIC PACKAGE

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