

# **DSTD-806**

## **6-SLOT STD CARD CAGE OPERATION MANUAL**

#### NOTICE

The proprietary information contained in this document must not be disclosed to others for any purpose, nor used for manufacturing purposes, without written permission of dy-4 SYSTEMS INC. The acceptance of this document will be construed as an acceptance of the foregoing condition.

## DSTD-806

### DESCRIPTION

The DSTD-806 is a 6 slot Z80-STD BUS Card cage consisting of a PCB backplane and metalwork.

The DSTD-806 uses dy-4 SYSTEMS' Z80-STD BUS implementation which supports multiple processors. Multiple processors are made possible on the STD bus by using a master/multi-slave arrangement. The slaves gain access to the bus using DMA cycles. To support multiple DMA devices, a DMA priority chain is used, similar to the interrupt priority chain. This chain uses pins 41 (/BA0) and pin 40 (BAI) and starts in the bottom slot. (refer to schematic).

The DSTD-806 also provides the cross-coupled NAND gates for reset switch debouncing. If the gates are not installed, Jumper JB1 should be installed. Provision is made for the installation of resistor terminators for the data bus, address bus and most of the control lines.

## **MATING CONNECTORS FOR BACKPLANE**

### **POWER CONNECTOR**

MOLEX:	Housing	09-50-3081
	Pins	08-50-0106

### **AUX. CONNECTOR**

AMP:	Housing	1-87499-1
	Pins	86016-5

NOTE: 1) Check PCB Orientation Label before inserting cards. PCB Component Side should be facing Up.

## **INTERRUPT PRIORITY CHAIN**

Board Position No. 1 Highest Priority

Board Position No. 6 Lowest Priority

Priority Chain flows from Bottom to Top

## **DMA PRIORITY CHAIN**

Board Position No.1 has Highest Priority

Board Position No.6 has Lowest Priority

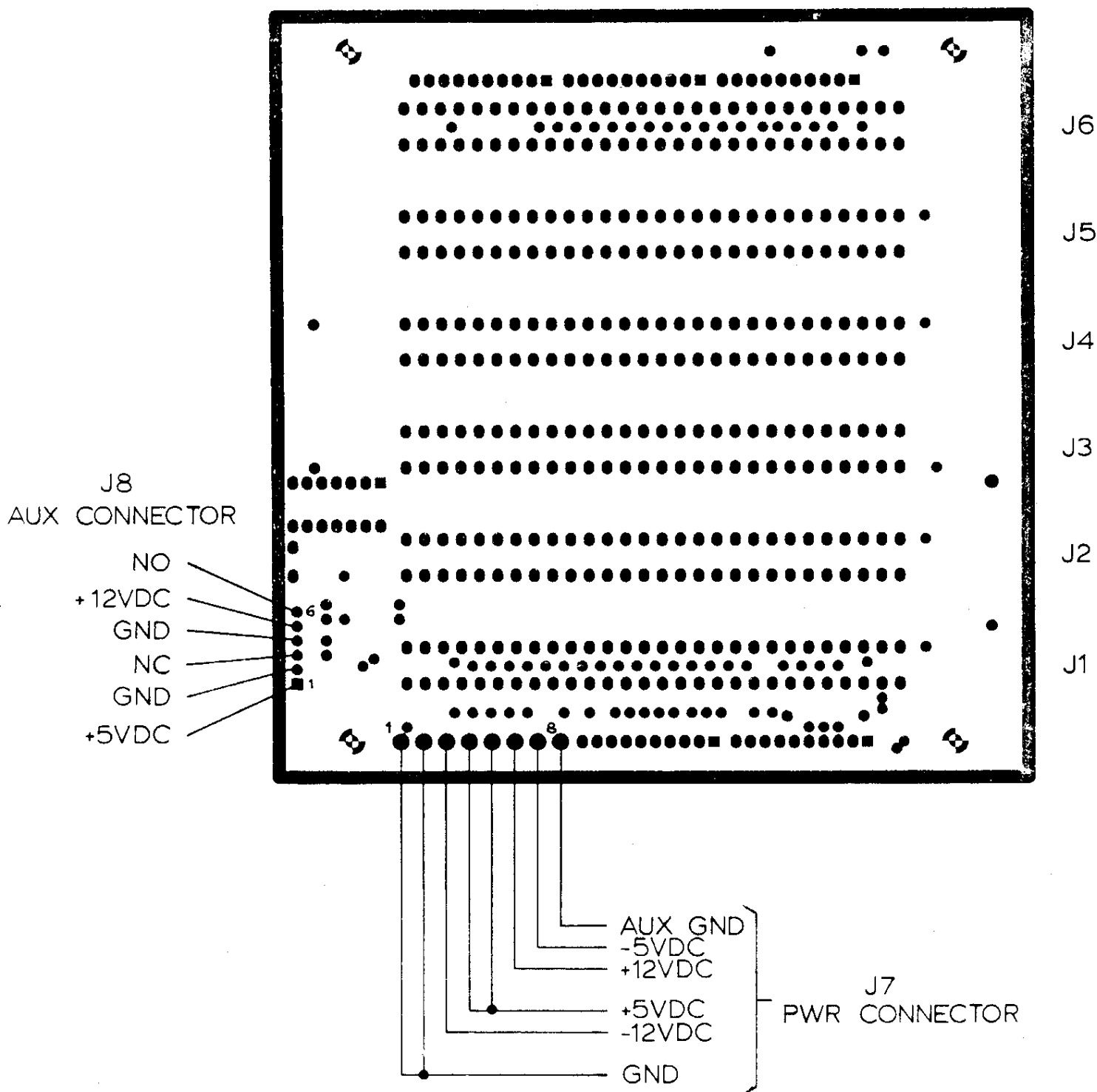
Priority Chain flows from Bottom to Top. DMA boards must be placed above the processor board.

## **MECHANICAL**

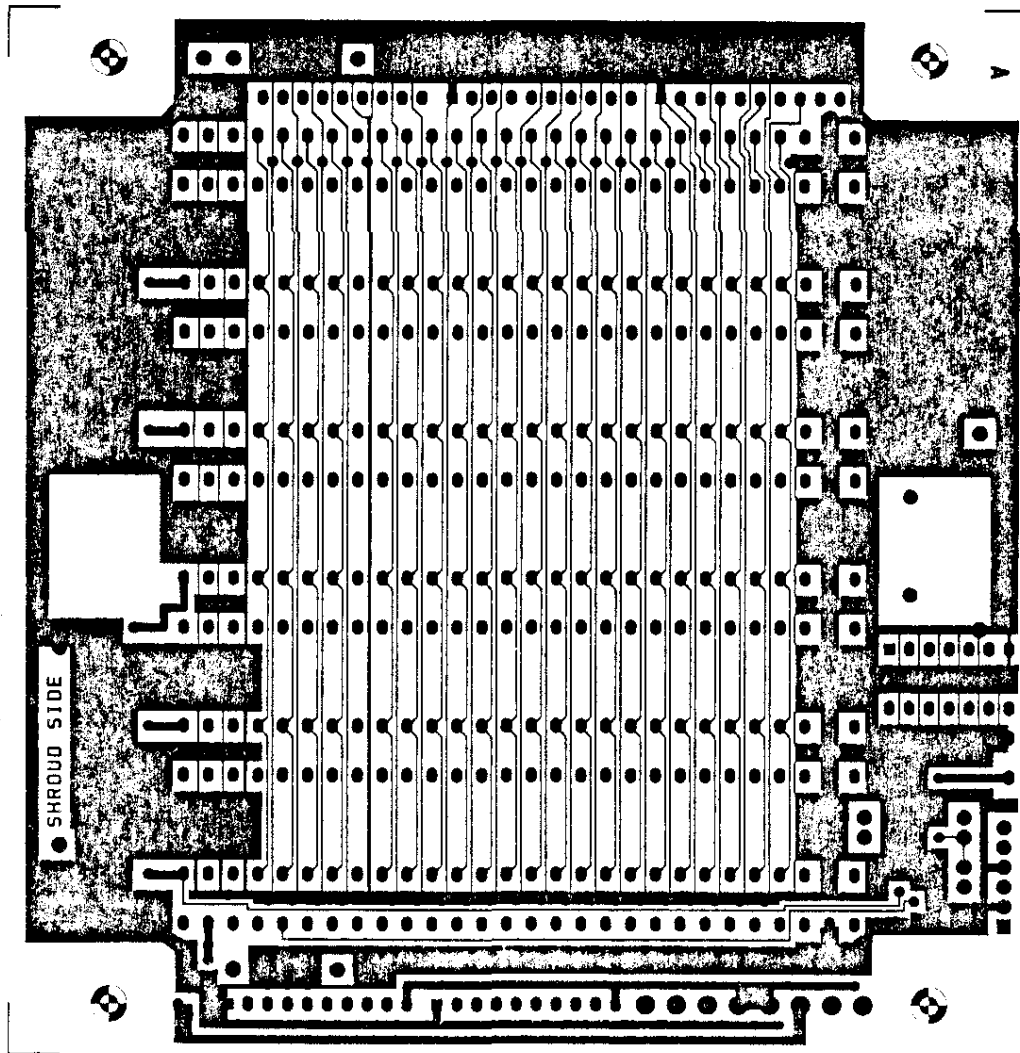
Height: 5.50"

Width: 6.0"

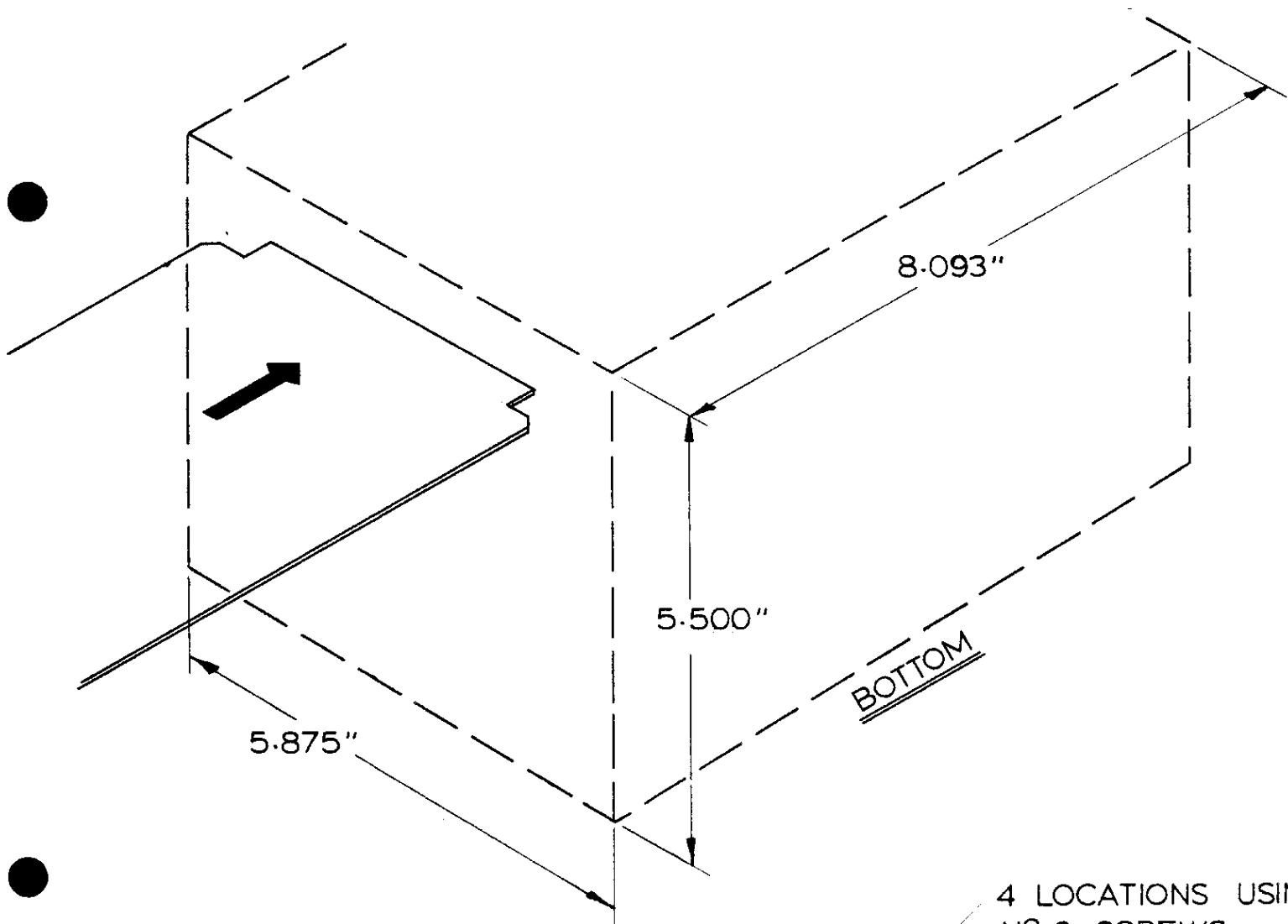
Depth: 8.375"



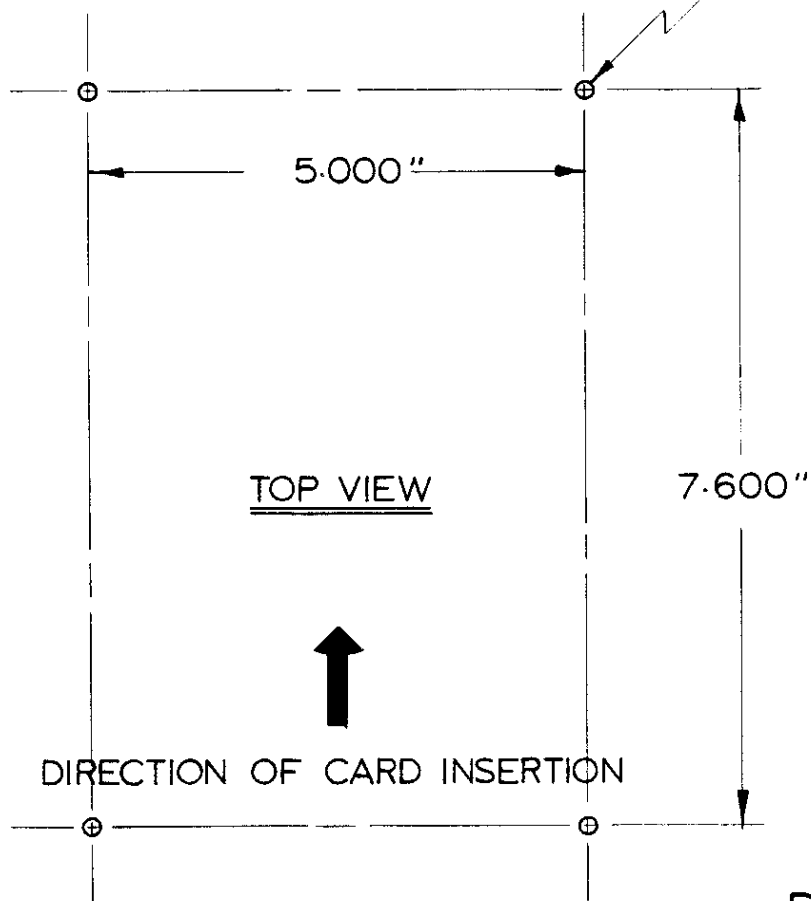
DSTD-806 BACKPLANE CONNECTOR CONFIGURATION



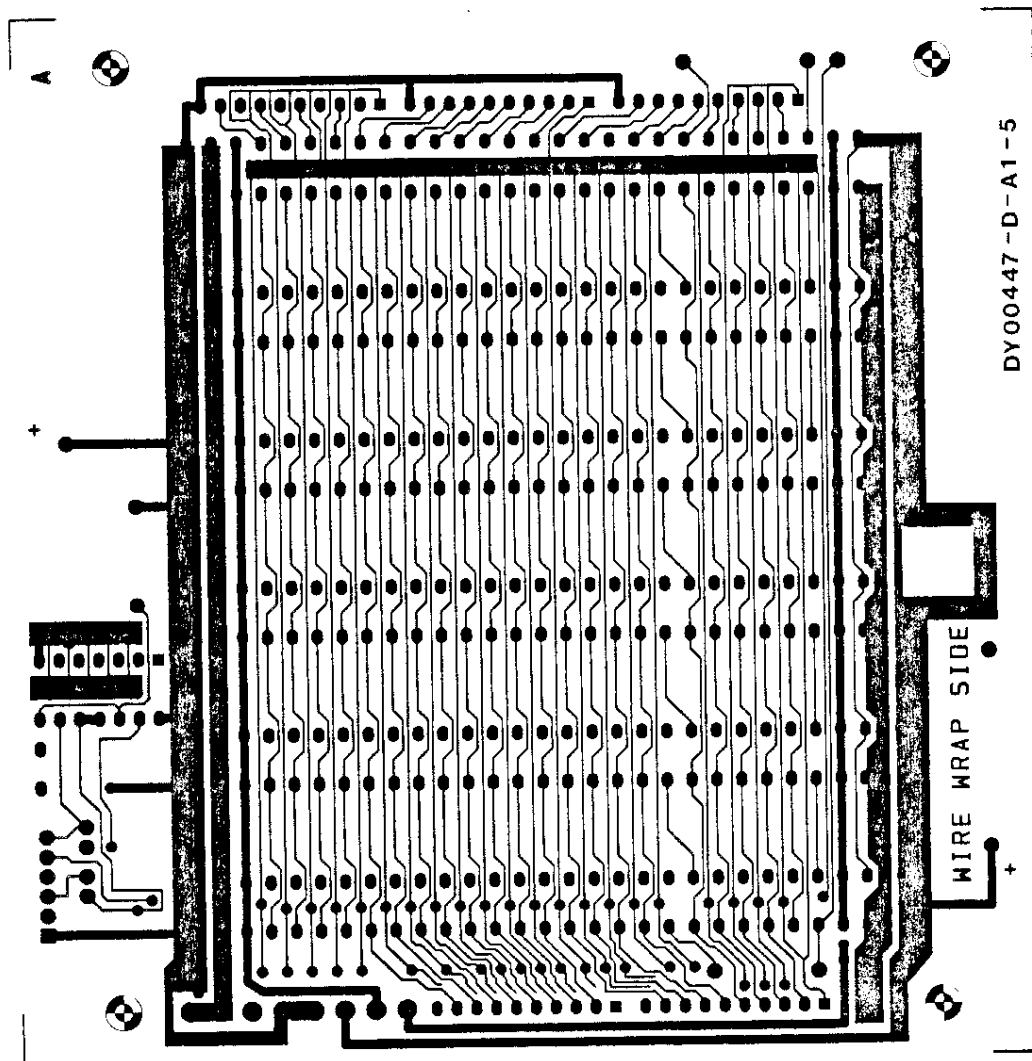
DSTD-806 BACKPLANE LAYOUT COMPONENT SIDE



4 LOCATIONS USING  
№ 6 SCREWS



DSTD-806



DSTD-806 BACKPLANE LAYOUT SOLDER SIDE



**APPENDIX A**

## **FACTORY NOTICES**

### **Factory Repair Service**

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a unit, enclose a letter containing the following information.

Name, address and phone number of purchaser  
Date and place of purchase  
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

dy-4 SYSTEMS INC.,  
888 Lady Ellen Place,  
Ottawa, Ontario  
K1Z 5M1, Canada

Securely package and mail the unit, prepaid and insured, to the same address.

### **Limited Warranty**

Dy-4 warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

**APPENDIX B**

**STD-Z80 BUS PIN OUT**

## APPENDIX B

### STD-Z80 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	Ground - System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	
15	A7	Address Bus (Tri-state, output, active high).
16	A15	
17	A6	
18	A14	

# STD-Z80 BUS PIN OUT

19	A5	A0-A15 make up a 16-bit address bus. The address bus provides the address for memory (up to 65k bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Memory Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Memory Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-State output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 Systems DSTD.

## STD-Z80 BUS PIN OUT

36	/MEMEX	Memory expansion, not used on dy-4 Systems DSTD cards.
37	/REFRESH	/REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic zero and the upper 8 bits of the address bus contains the I register.
38	/DEBUG	/DEBUG (Input) used in conjunction with DDT-80 operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the /DEBUG line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
39	/M1	Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the opcode fetch cycle of an instruction. Note that during the execution of a 2-byte opcodes, /M1 will be generated as each opcode is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
40	STATUS 0	DMA priority chain input.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

## STD-Z80 BUS PIN OUT

- 42        /BUSRQ        Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.
- 43        /INTAK        Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.
- 44        /INTRQ        Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.
- 45        /WAITRQ        WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

## STD-Z80 BUS PIN OUT

46	/NMIRQ	Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will over-ride a /NMIRQ.
47	/SYSRESET	System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H and set Interrupt Mode 0.
48	/PBRESET	Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset.
49	/CLOCK	Processor Clock (Output, active low). Single phase system clock.
50	CNTRL	Auxiliary Timing
51	PCO	Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.



## STD-Z80 BUS PIN OUT

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

### NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.

APPENDIX C

PARTS LIST

## APPENDIX C

## DSTD-806 PARTS LIST

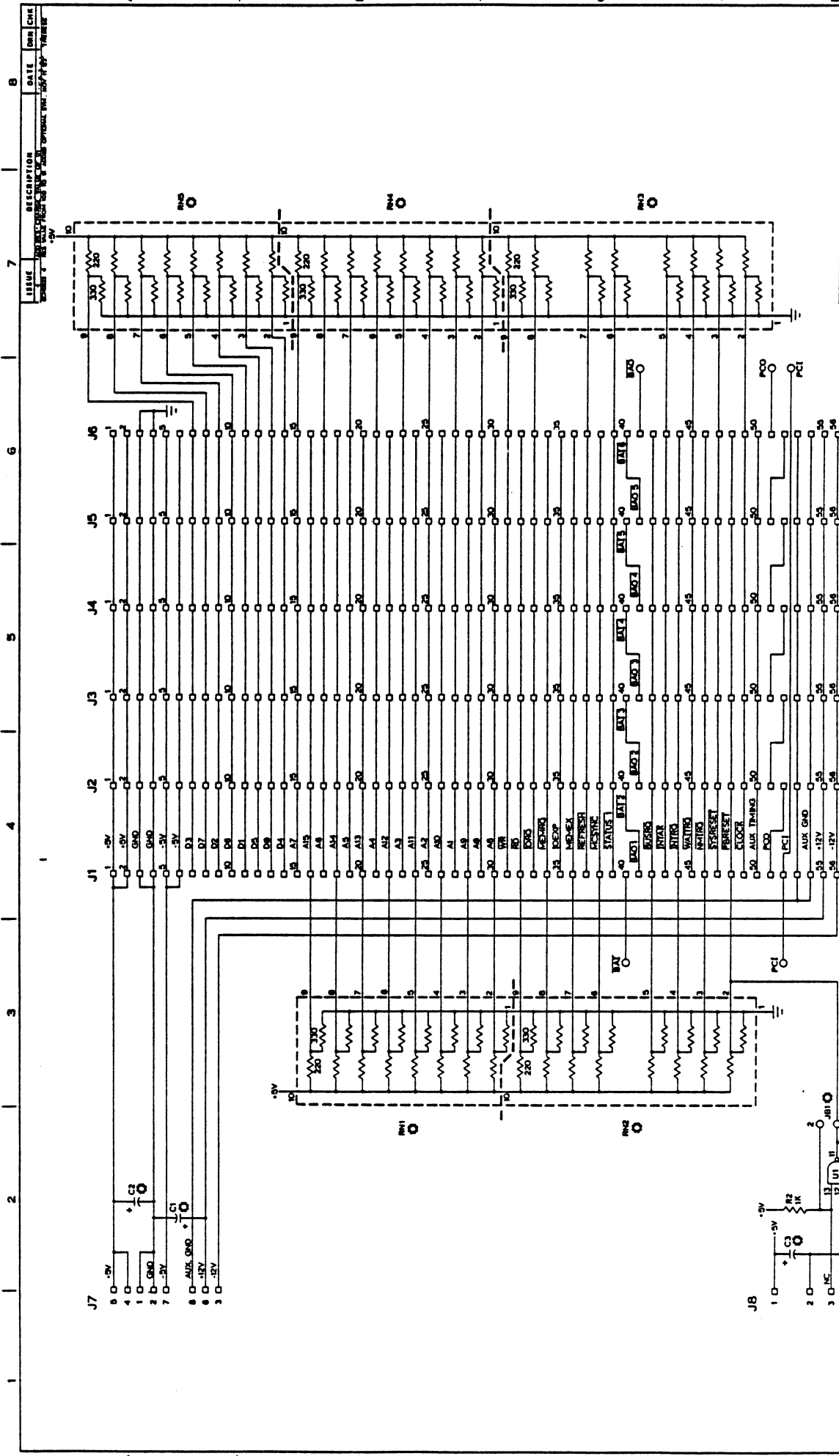
QTY	DESCRIPTION	DESIGNATION
1	741803 TTL-LS	Q1
3	1/4 WATT, 1K OHM, 5% RESISTOR	R1,R2,R3
12	11433-2 CARD GUIDE (SMALL)	
5	1-530942-7 SOLDER TAIL CONNECTOR	J1,J2,J3,J4,J5
1	4-530925-6 WIRE WRAP CONNECTOR	J6
0	65499-136 36 PIN HEADER (FOR BACKPLANES ONLY)	J8
1	640388-8 8 PIN WHITE HEADER	J7
1	640357-3 14 PIN I.C. SOCKET	U1
2	DSTD 806 & 812 CARDCAGE SIDES DY00471-M-H1-2	
1	4 FOOT CARDCAGE BOTTOM DY00471-M-L1-1	
1	DSTD 804,805,806 SLOT CARDCAGE TOP DY00471-M-H1-2	
1	6 SLOT BACKPLANE DY00447-H-41-4	

# APPENDIX C

## DSTD-806 PARTS LIST

SYSPART	QTY	DESCRIPTION	DESIGNATION
PT012003	1	74LS03 TTL-L6	U1
PT041102	3	1/4 WATT, 1K OHM, 5% RESISTOR	R1,R2,R3
PT111069	12	11639-2 CARD GUIDE (SMALL)	
PT121000	5	1-530842-7 SOLDER TAIL CONNECTOR	J1,J2,J3,J4,J5
PT121001	1	4-530825-4 WIRE WRAP CONNECTOR	J6
PT122007	0	65499-156 36 PIN HEADER (FOR BACKPLANES ONLY)	J8
PT123007	1	640389-9 9 PIN WHITE HEADER	J7
PT126014	1	640357-3 14 PIN I.C. SOCKET	U1
PT247109	2	DSTD 806 & 812 CARDCAGE SIDES DY00471-M-H1-2	
PT247110	1	2 FOOT CARDCAGE BOTTOM DY00471-M-H1-2	
PT247113	1	DSTD 804,805,806 SLOT CARDCAGE TOP DY00471-M-H1-2	
PT344701	1	3 SLOT BACKPLANE DY00447-H-A1-A	

**APPENDIX D**



dy-4 SYSTEMS INC.			
SCALE	DATE	CHK	DATE
APP'D	APP'D	CHK	CHK
TOL	TOL	MAT'L	MAT'L
6-SLOT BACKPLANE SCHEMATIC			
REV NO. DY00447-I-A1-5			
113 5 11 1			

