

TABLE 4

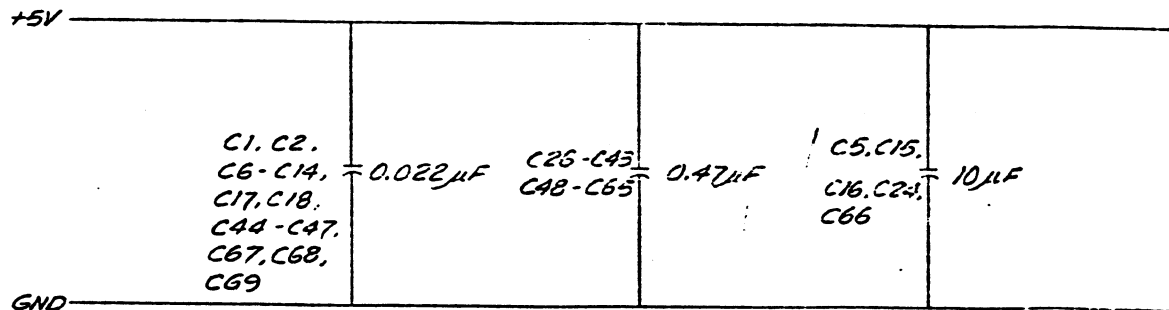
REFERENCE NO.	OUTPUT PINS NOT USED
U4	3
U22	12
U27	8, 12
U29	10, 12
U30	8, 11
U33	11
U34	9
U37	6, 8, 10, 12
U1	3
U47	6, 8, 11
U52	12
U54	11
U58	4, 10, 13
U71	8, 9
U73	11
U75	8, 12
U76	12
U98	3, 8, 11
U99	8
U102	6
U123	5
U132	8, 11

TABLE 3

HIGHEST DESIGNATION USED	DESIGNATION NOT USED
U155	
C70	
R47	
R19	
POT3	
Y2	
J14	
D1	
Q1	
LED1	

TABLE 2

JUMPER T	
CONNECTION	
J8	27-28, 25-26 23-24, 21-22 19-20, 17-18 15-16, 1-3 5-7,
J9	27-28, 25-26 23-24, 21-22 19-20, 17-18 15-16, 1-3 5-7,
T5	IN FOR NO 8087 OUT FOR 8087
T18	IN FOR NORMAL OUT FOR DIAGNOST.



REV	ECO	DESCRIPTION	DATE	BY	CHE	APPROV
01		PREPARED BY (1111-1)	02/03/87	ET	-	K

TABLE 2

JUMPER TABLE	
NO	FUNCTION
25-26 21-22 7-18 1-3	I/O PORT J3 ASYNCHRONOUS OPERATION
25-26 21-22 7-18 1-3	I/O PORT J4 ASYNCHRONOUS OPERATION
NO 8087 CO-PROCESSOR FOR 8087 CO-PROCESSOR PRESENT	
NORMAL OPERATION	
DIAGNOSTIC TEST	

TABLE 1

POWER AND GND LOCATION TABLE				
REFERENCE NO.	POWER PINS			
	+5V	GND	+12V	-12V
U22, 24-30, 32-34, 37, 41, 43, 45, 47-58, 72-76, 98- 100, 102, 113, 114, 116-119, 131-133, 135, 137	14	7	-	-
U19, 21, 70, 82, 83, 95, 101, 112, 120, 130, 136, 147, 150-155	16	8	-	-
U15-17, 20, 40, 42, 44, 46, 59-66, 69, 81, 84, 85, 96, 97, 148, 149	20	10	-	-
U2, 5, 8, 11	14	7	-	-
U3, 6, 9, 12	26	4	-	-
U13, 14, 67, 68	24	12	-	-
U18	18	9	-	-
U23, 31	4	11	-	-
U95, 36	28	14	-	-
U38, 39	40	120	-	-
U78	26	7	-	-
U79	21	20	40	-
U80	15, 16	8, 9	-	-
U86-94, 103-113, 121- 129, 138-146	8	16	-	-
U115	31	20	-	-
U1, 4, 7, 10	-	7	14	1

+5V



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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES .00 ± 0.01 ANGLES ± 30° 30' .000 ± .005		DR	CHK	ESGN	OTTAWA CONSOLIDATED COMPUTER INC. CANADA
MATERIAL	SPEC.	ENGRY	DESIGNED FOR	APPROVED	
NEXT ASSY.	USED ON	FINISH	APPROVED	DRW CODE	CPU MAIN LOGIC MPEU 1600
APPLICATION	SPEC.	APPROVED	APPROVED	SCALE	

DATE: 82-8-14

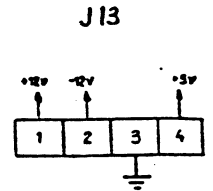
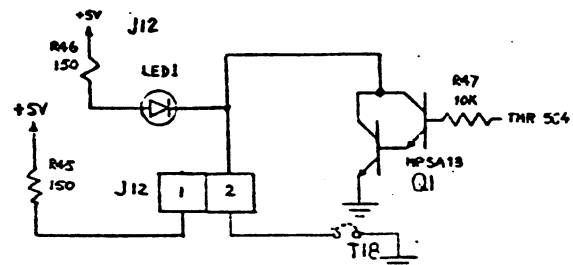
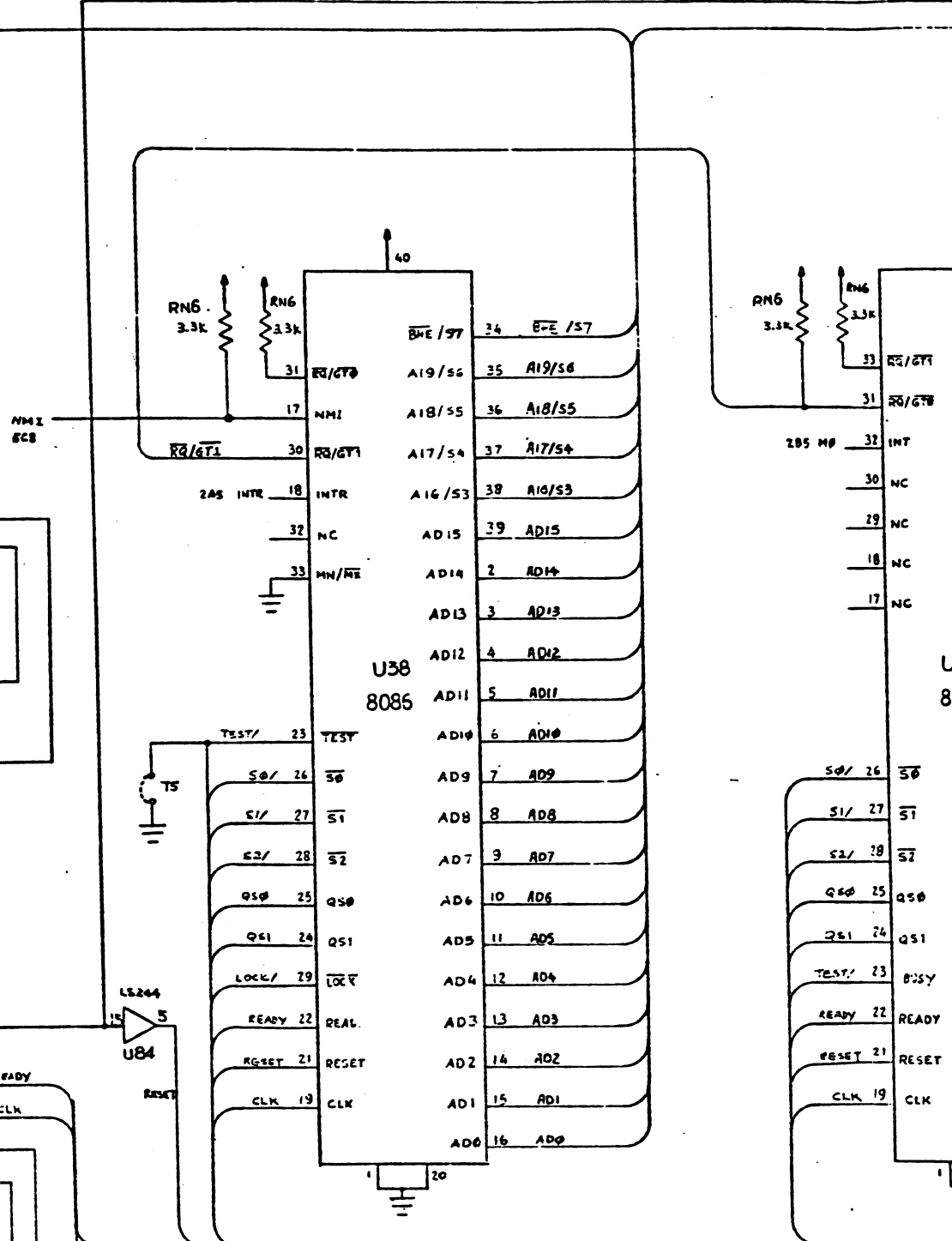
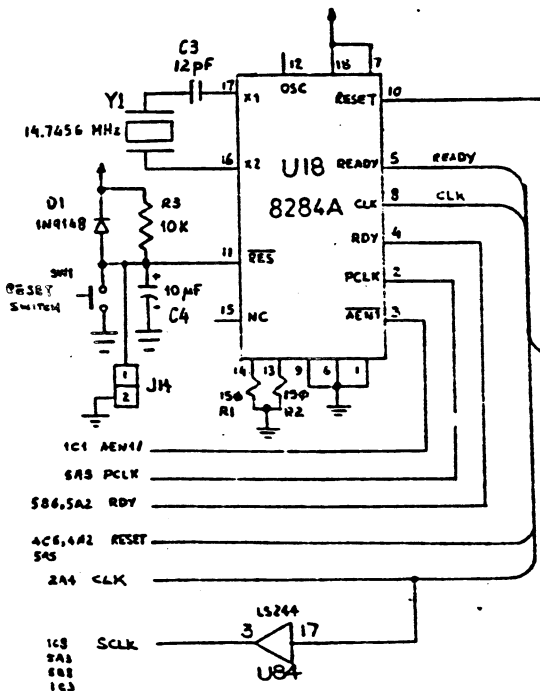
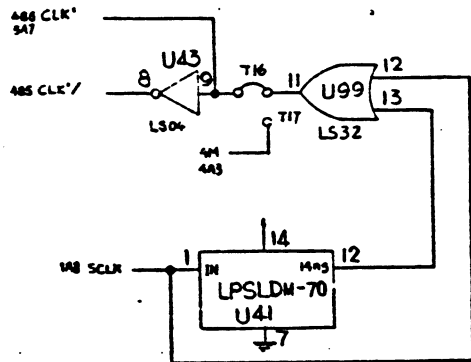
SIZE: D 06-90000-420

SHEET 1 OF 4

B [022-90000-91]

A

2DR. SCB { BWE/S7
A16/S3 - A19/S6
AD0-AD15
508 { 507 - 521

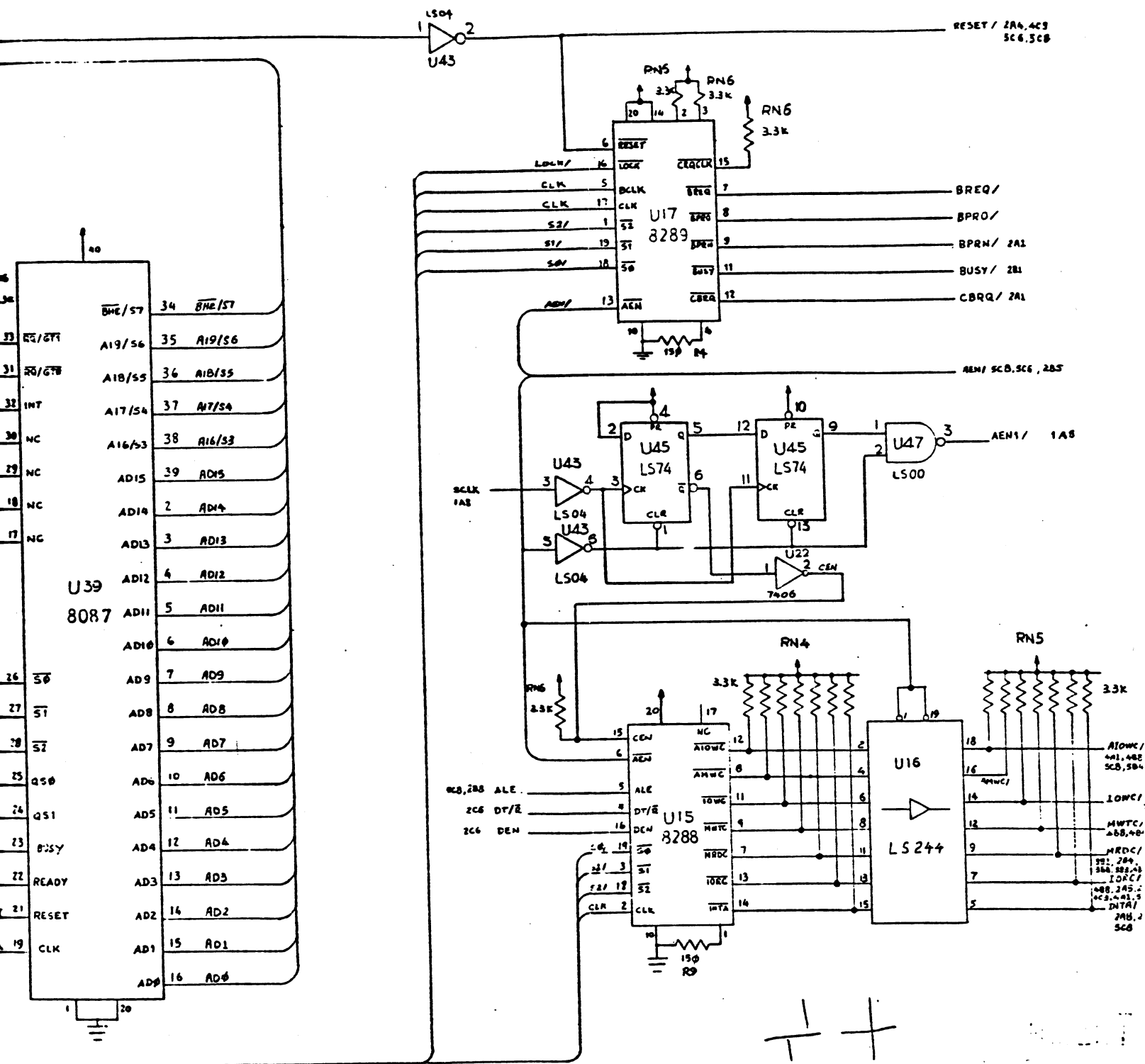


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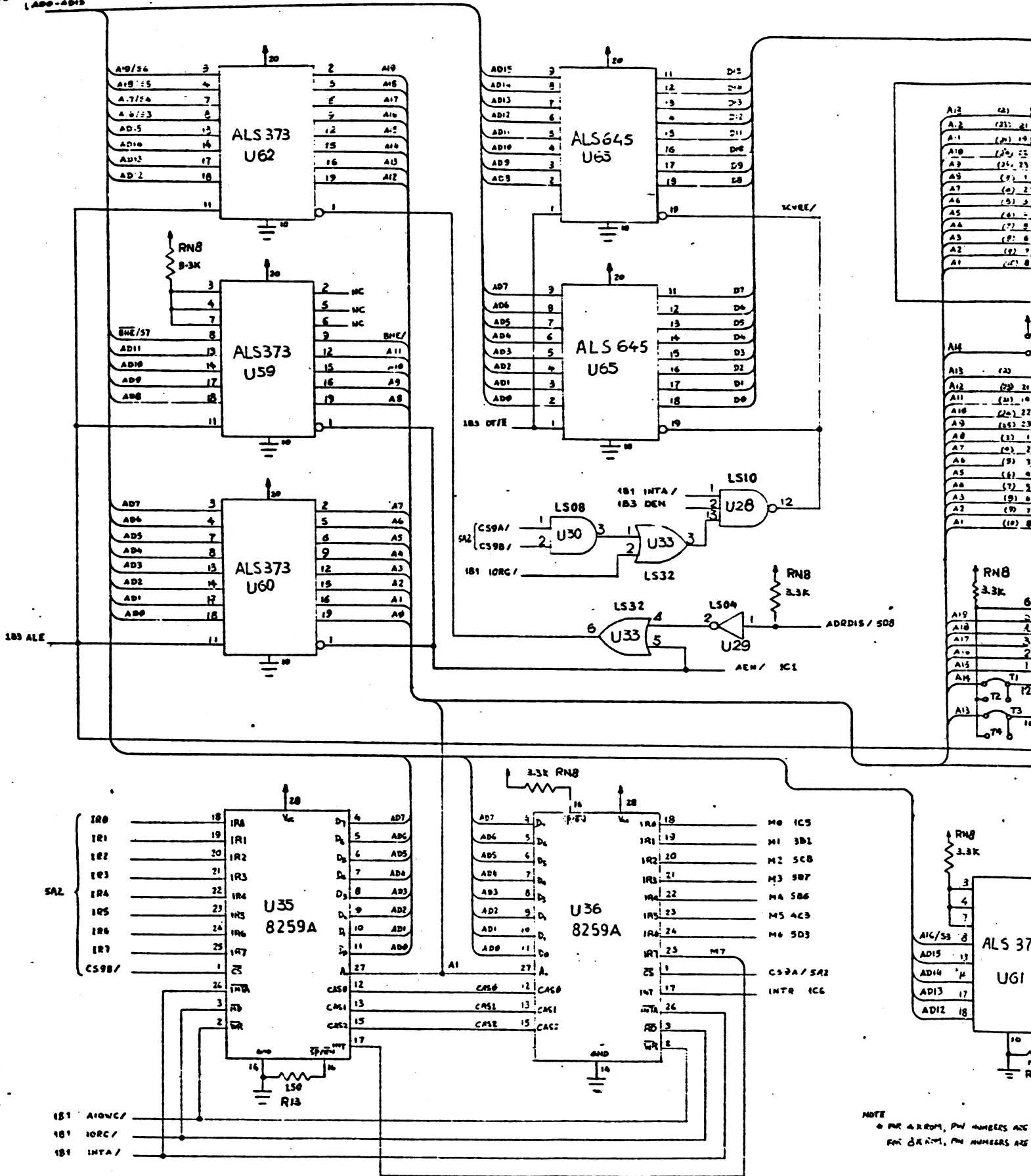
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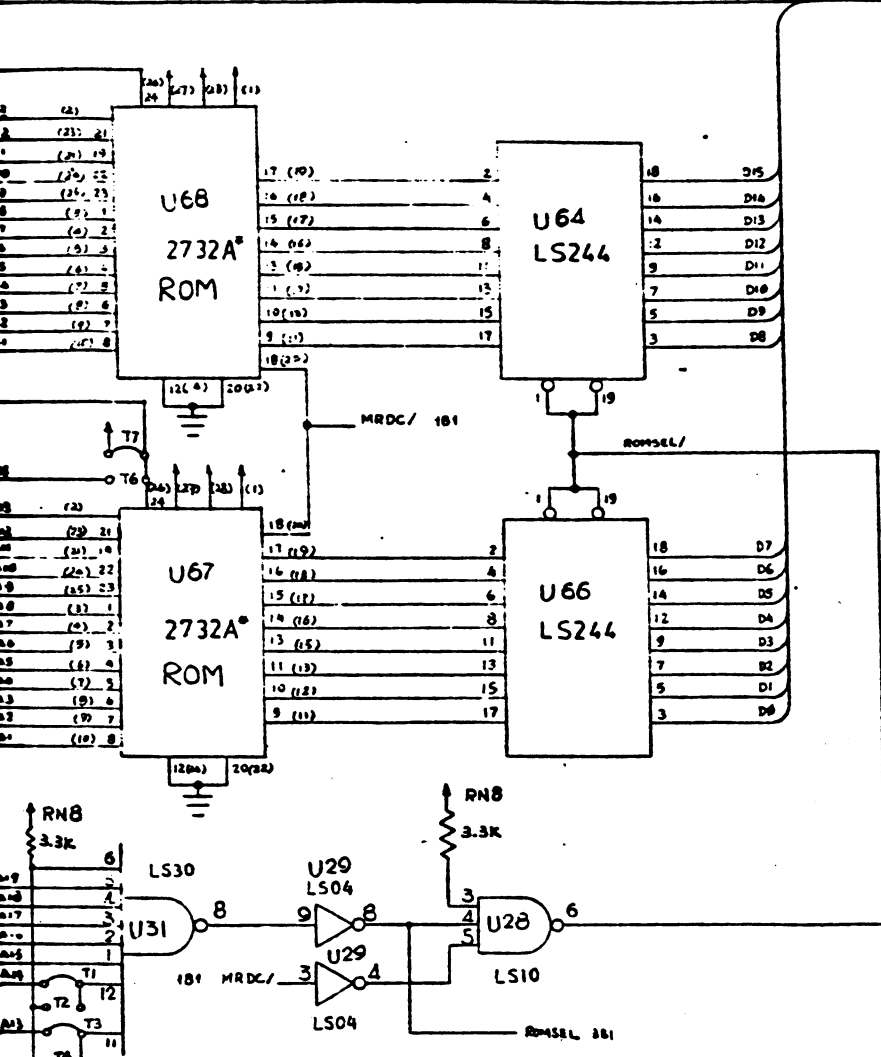


APPROVED	W. SIM	SIZE	CODE	DWG NO.	REVISION
CHECKED	S. HOW	D		C6-90000420	0
DRAWN	J. LIBAQUE	SCALE	NONE	ISSUED	MAY 82 SHEET 2 OF

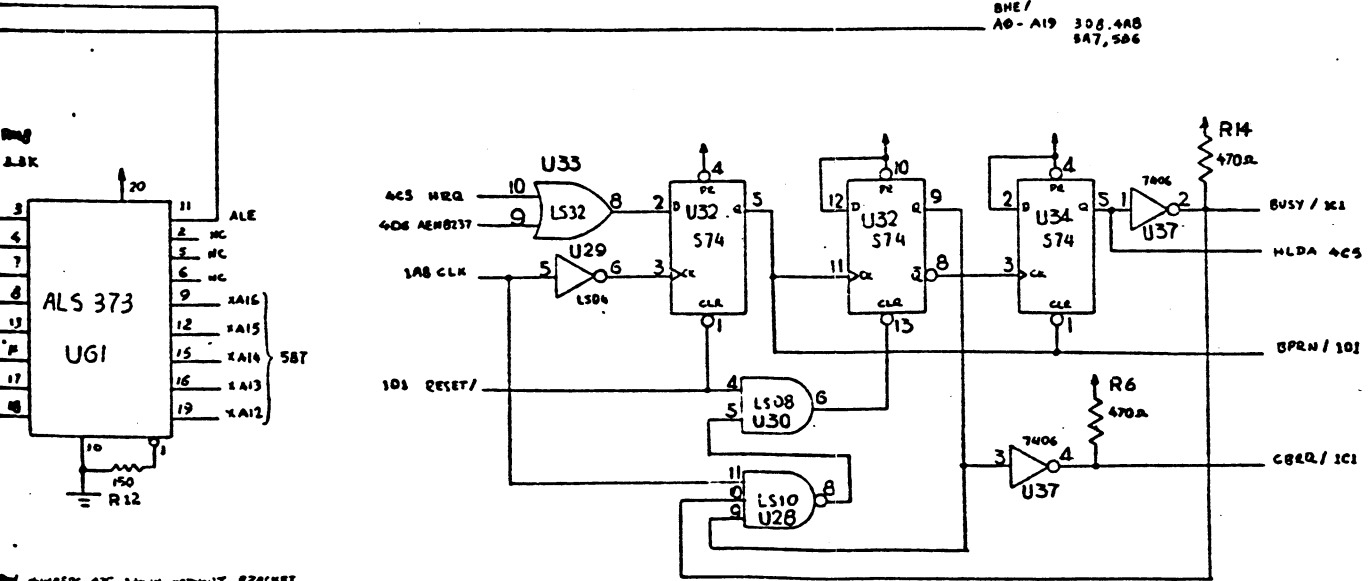


NOTE
 * PIN # R001, PIN NUMBERS ARE
 FOR 8K R01, PIN NUMBERS ARE

D0-D15 301,305



BHE / A0-A19 308,4A8 8A7,506



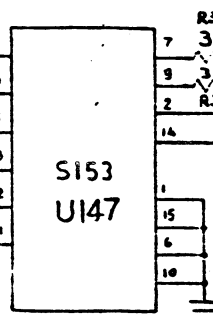
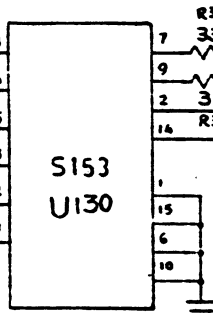
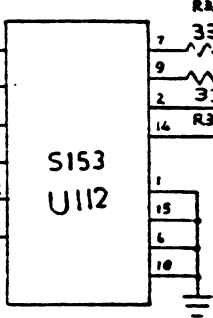
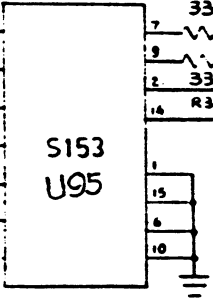
ALL NUMBERS ARE SHOWN WITHOUT BRACKET
ALL NUMBERS ARE SHOWN WITH BRACKET

APPROVED	W. SIM	SIZE	D	CODE	DWG. NO.	06-90000420	REV.	0
CHECKED	S. CHNW	SCALE	NONE	ISSUED	MAY 62	SHEET	3	OF
DRAWN	J. LIBAQUE							

ABA BME/
AG-A19

J10
55 PINS

- 35 A2
- 47 A1
- 51 A5
- 54 A4
- 52 A5
- 50 A6
- 46 A6
- 38 A7
- 42 A9
- 37 A9
- 49 A10
- 39 A11
- 53 A12
- 41 A13
- 48 A14
- 45 A15
- 40 A16
- 24 A17
- 23 A18
- 25 A19
- 6 D0
- 10 D1
- 14 D2
- 18 D3
- 19 D4
- 15 D5
- 11 D6
- 7 D7
- 5 D8
- 9 D9
- 13 D10
- 17 D11
- 20 D12
- 16 D13
- 12 D14
- 8 D15
- 29 MDC/181
- 30 MTC/3A3
- 31 RFSH/3A8
- 27 DMPH 30A
- 43 DMPH 30B
- 32 DMPH 30C
- 36 DMPH 30D
- 28 CAS/3A1
- 26 SEL 3A1
- 3 BME/
- 1
- 4
- 22
- 33
- 55
- 2
- 21
- 34
- 44
- 56

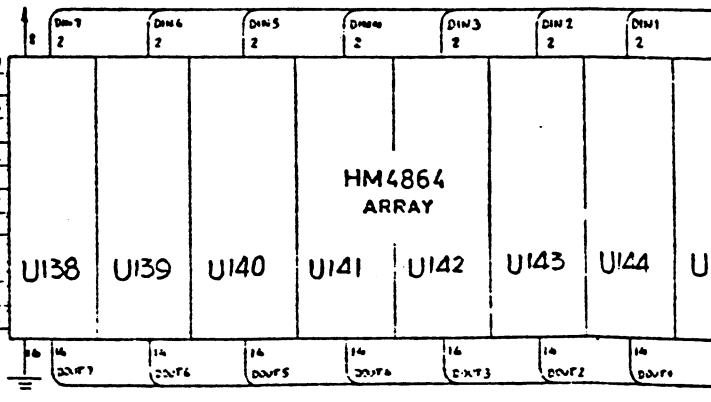
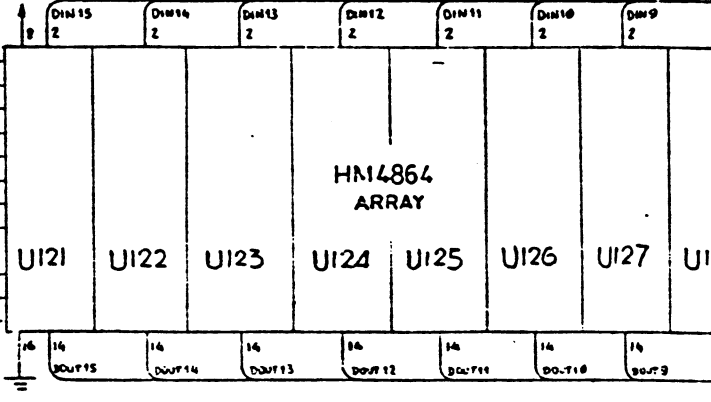
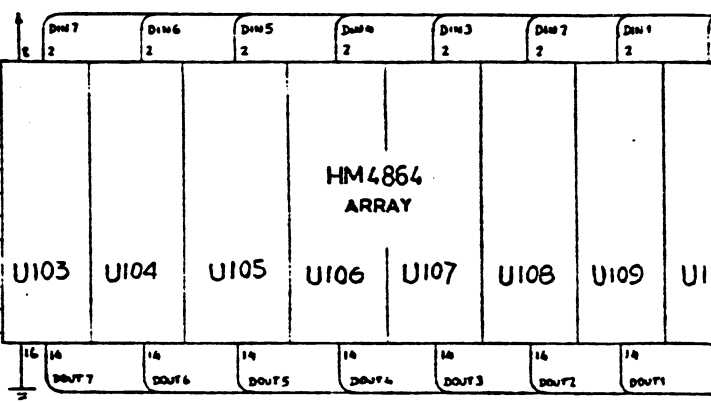
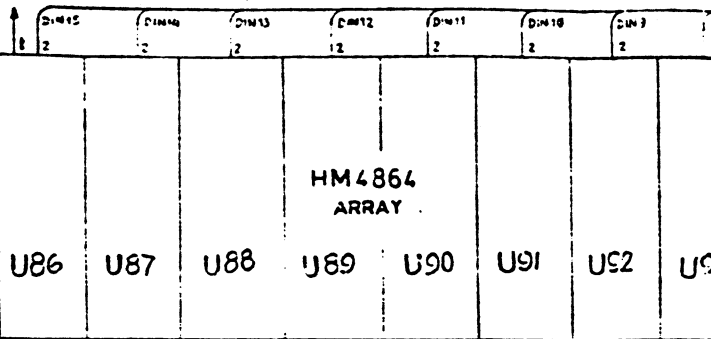


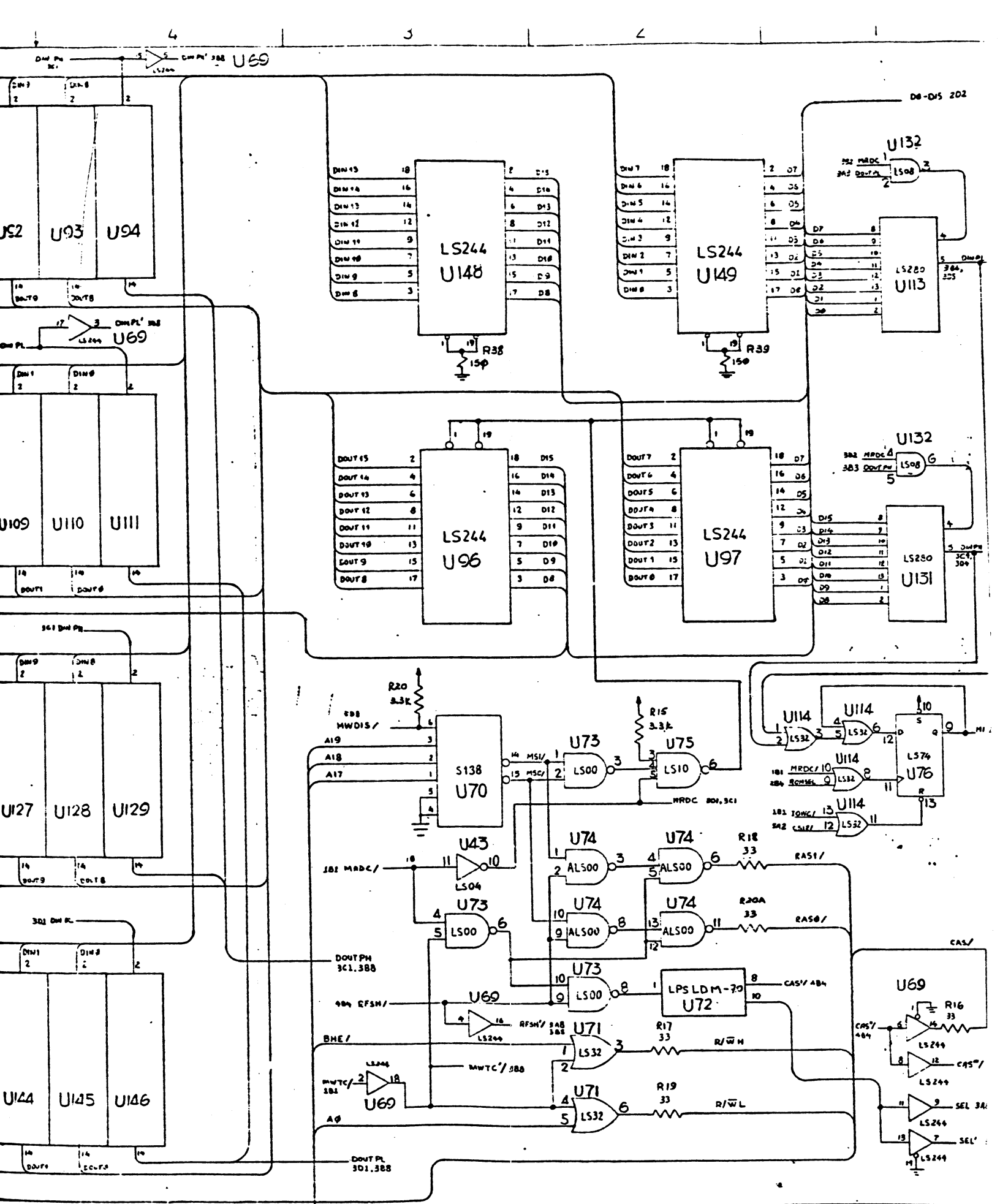
- MA7 9
- MA6 13
- MA5 10
- MA4 11
- MA3 12
- MA2 6
- MA1 7
- MA0 5
- RAS/ 4
- CAS/ 15
- R/W 3

- MA7 9
- MA6 13
- MA5 10
- MA4 11
- MA3 12
- MA2 6
- MA1 7
- MA0 5
- RAS/ 4
- CAS/ 15
- R/W 3

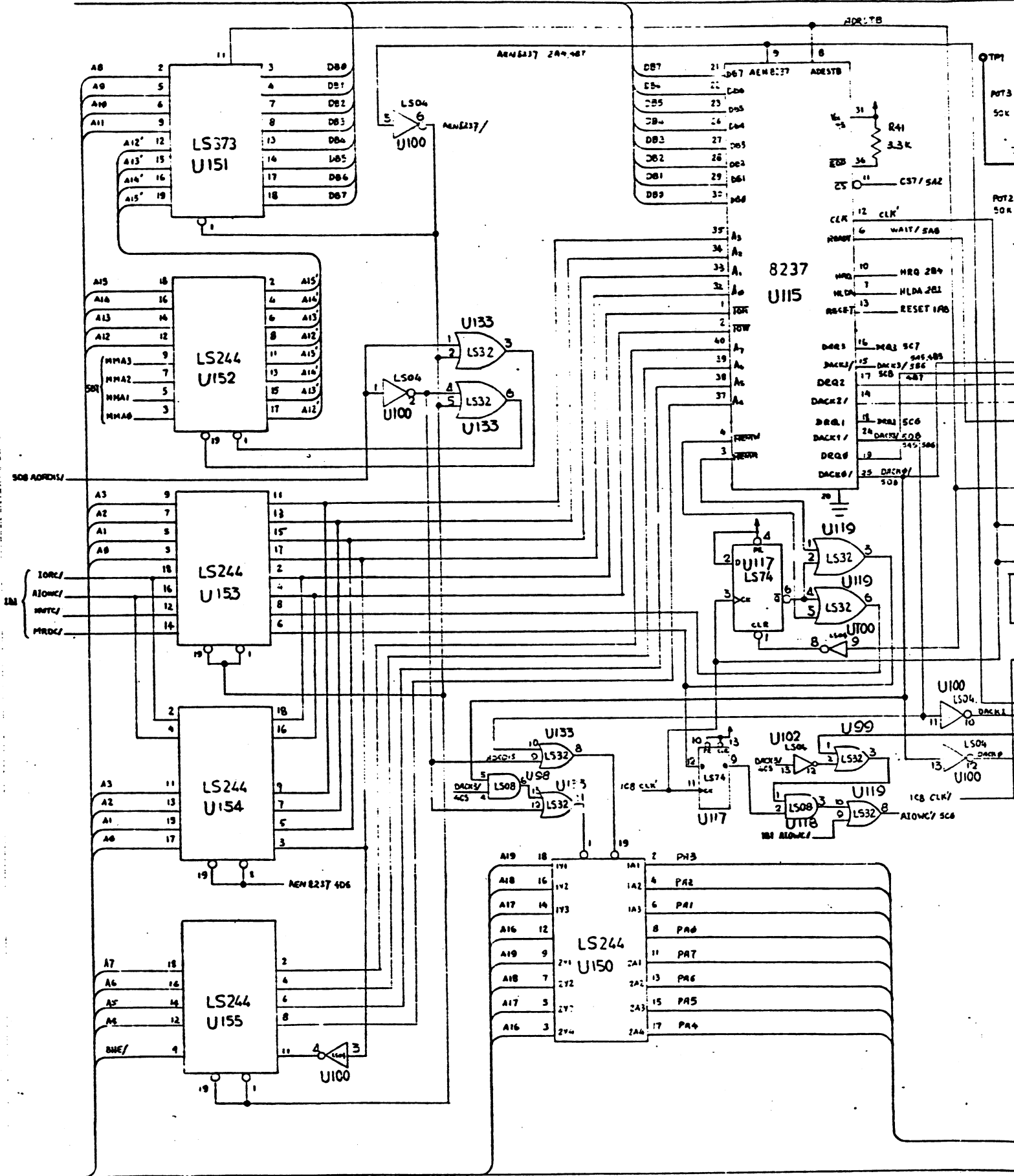
- MA7 9
- MA6 13
- MA5 10
- MA4 11
- MA3 12
- MA2 6
- MA1 7
- MA0 5
- RAS/ 4
- CAS/ 15
- R/W 3

- MA7 9
- MA6 13
- MA5 10
- MA4 11
- MA3 12
- MA2 6
- MA1 7
- MA0 5
- RAS/ 4
- CAS/ 15
- R/W 3





APPROVED	W S W	SIZE	D	SOLE	DWG NO.	06-3000420	REV	0
CHECKED	S CH W	SCALE	NONE	ISSUED	MAY 82	SHEET	4	OF
DRAWN	J LIBAQUE							



282 A0-A19
BnE/

8

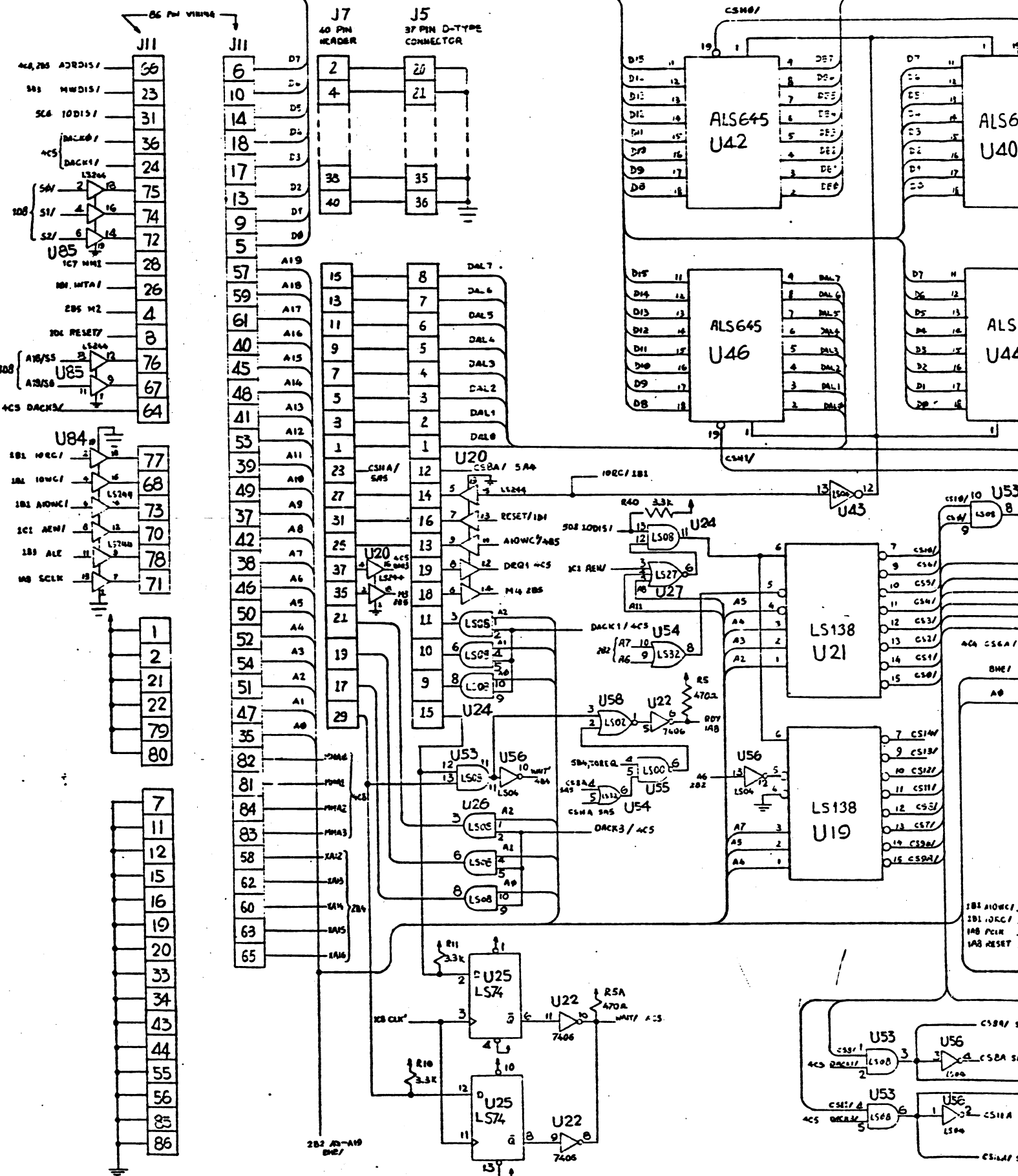
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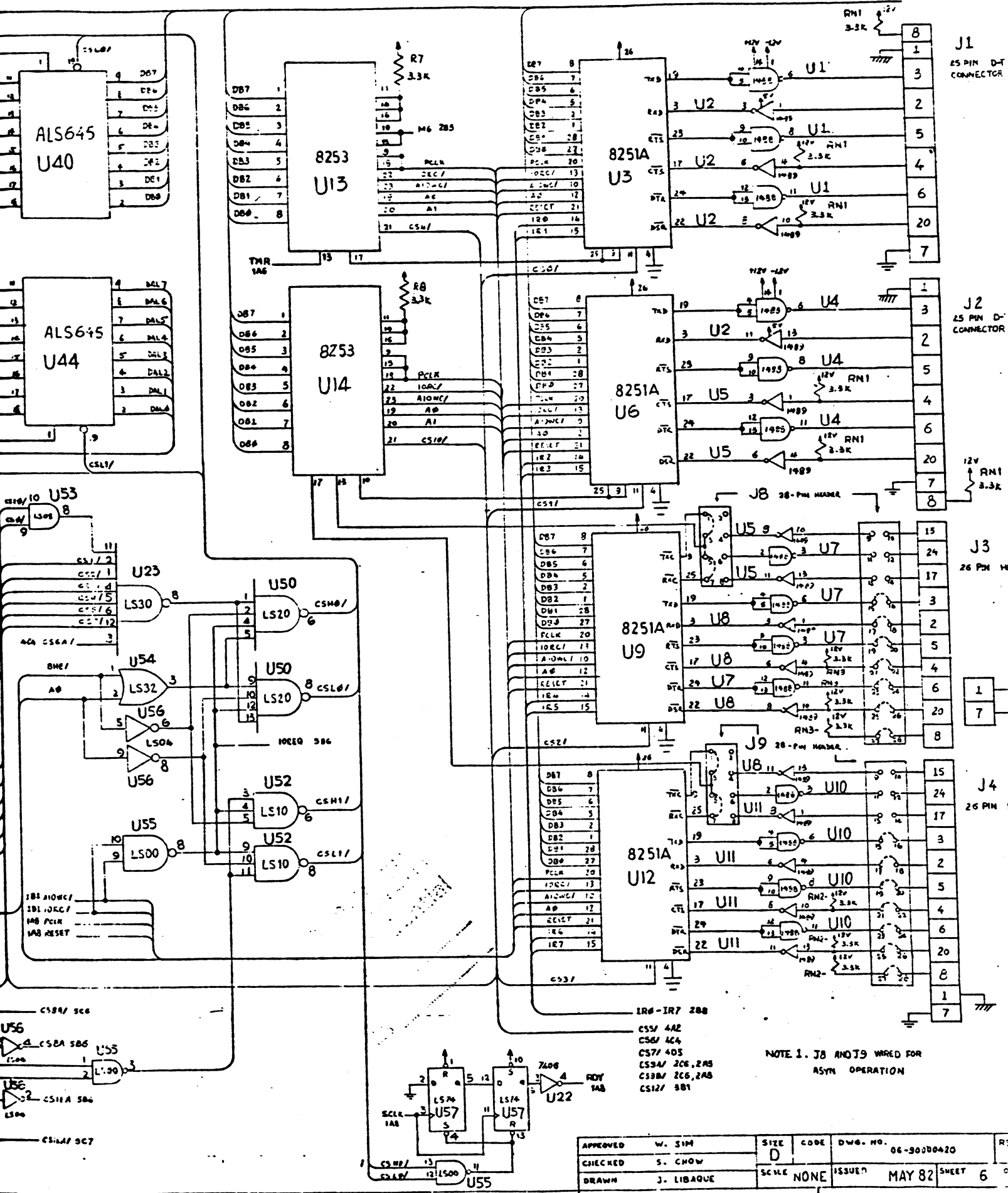
6

5

202 D15-D0

06 PM VIBRA





APPROVED	W. SIM	SIZE	D	CODE	DWG. NO.	06-30300420	R:
CHECKED	S. CHOW	SCALE	NONE	ISSUED	MAY 82	SHEET	6
DRAWN	J. LIBAQUE						

4.

3

2

1

TABLE 1 CHIP CHART

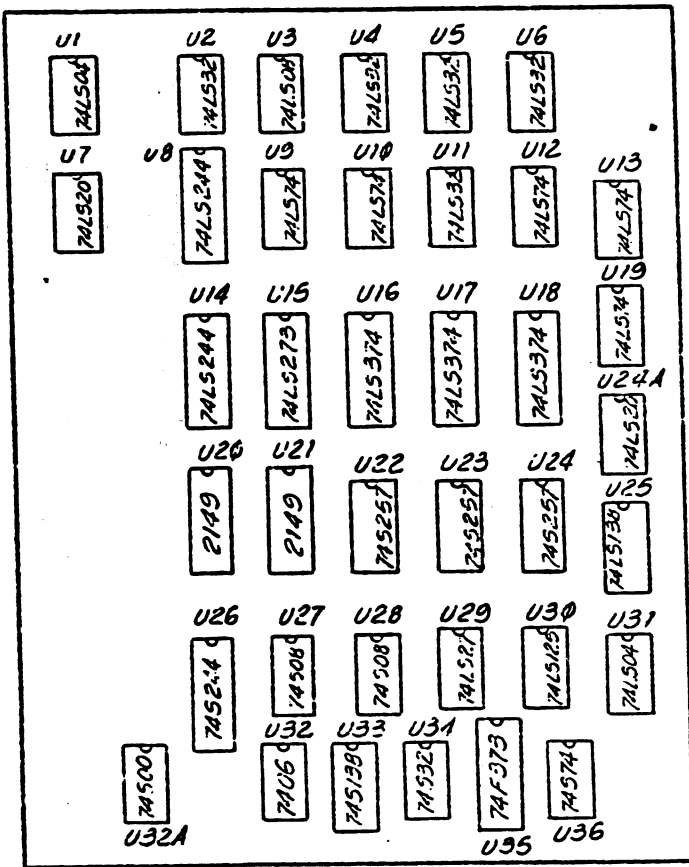


TABLE 2 POWER AND GROUND

CHIP NO.	PIN NO				
	+5V	GND	-5V	-12V	-12V
U1 - U13, U19, U24A, U27, U28, U29, U35, U31, U32, U32A, U34, U36	14	7			
U22 - U25, U33	16	8			
U3, U14 - U18, U26, U35	20	10			
U20, U21	18	9			

TABLE 3 SPARE GATES

LOCATION	OUTPUT PINS
U1	4, 6, 10, 12
U2	3, 8
U3	6
U4	6
U28	6, 8
U30	8
U32A	3, 6, 11
U34	6, 8, 11

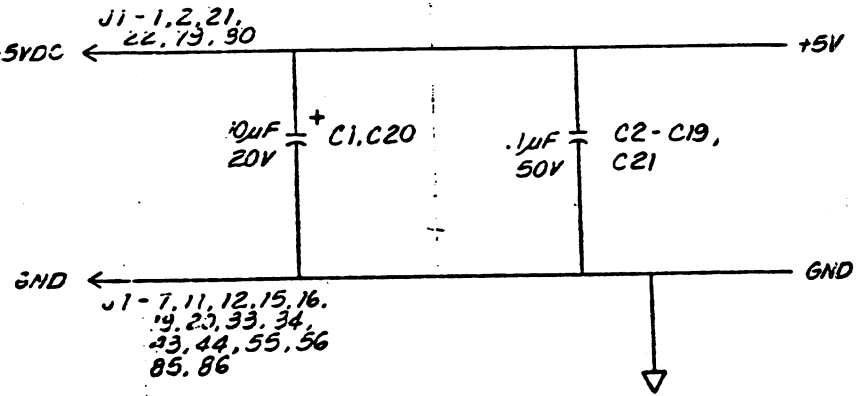
+5VDC ←

TABLE 4 COMPONENT REF.

HIGHEST DESIG. USED	DESIGNATION NOT USED
C21	
J1	
R1	
U36	

GND ←

REV	DATE	DESCRIPTION	BY	APP'D
02		ERR (11.22)	BT	GA



L UNLESS OTHERWISE SPECIFIED ALL RESISTORS 1/4 WATT.

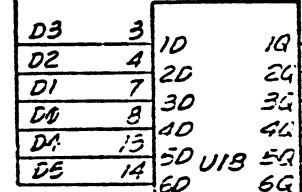
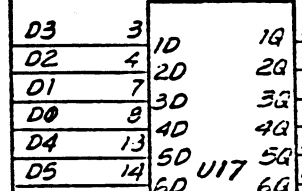
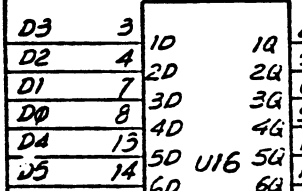
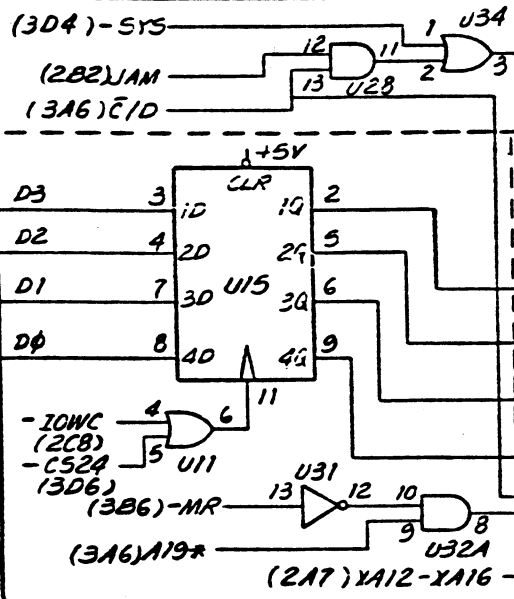
NOTES: REFERENCE SYMBOL

-0		AS SHOWN	
PART NUMBER AND VARIANT DESCRIPTION			
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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES .0005 .001 ANGLES ± 20° 30° 90° ± .005	BY <i>ELIN</i> <i>EBG/K</i>	CONSOLIDATED COMPUTER INC.	
MATERIAL	DESIGNED BY <i>DOONER</i> <i>EBG/RE</i>	LOGIC DIAGRAM	
SPEC	ENGRS	MMU (OPTION) 16XX	
FINISH	ORIGINALLY DESIGNED BY <i>16XX</i>	SCALE <i>1:1</i>	D <i>90000430</i>
SPEC	APPROVED	DWG CODE	SHEET <i>1</i> OF <i>3</i>
	APPROVED		DATE

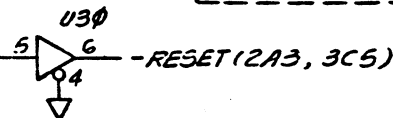
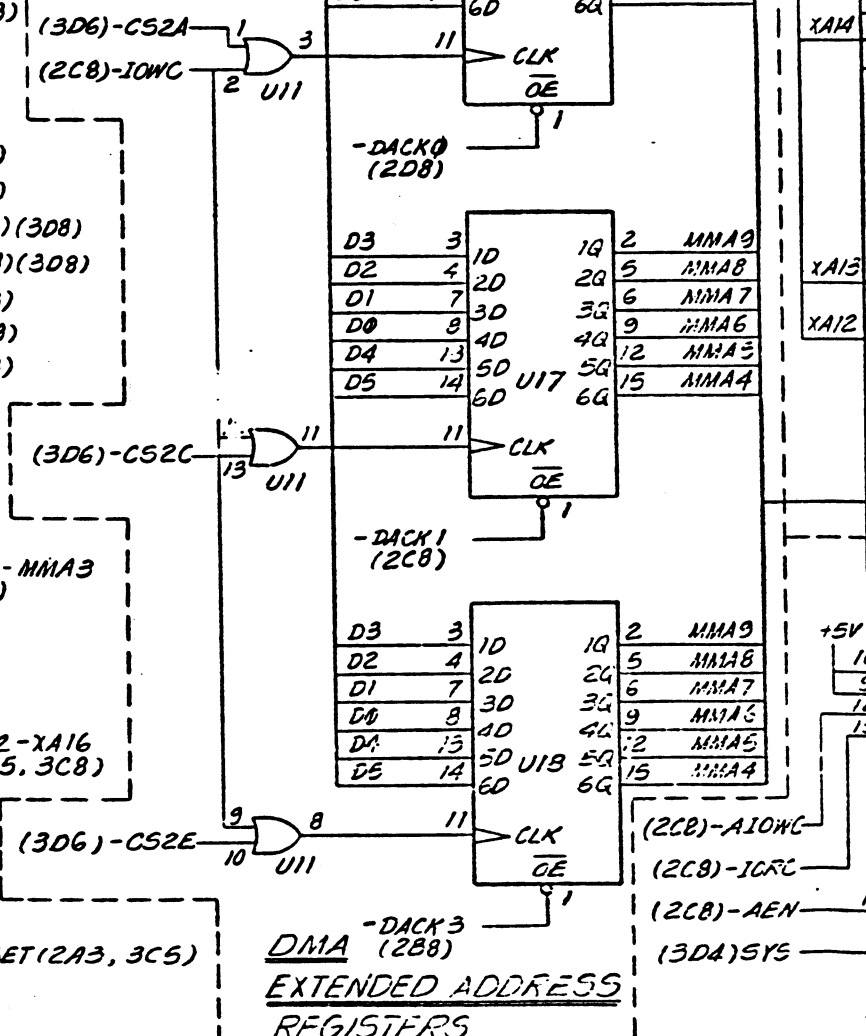
(2A3, 3A2, 3D5) D0-D7

(30A) - ADDRIS	66	6	D7
(3B4) - MWDIS	23	10	D6
(3D3) - IODIS	31	14	D5
(2B6) - DACK 0	36	18	D4
(2B6) - DACK 1	34	17	D3
(3A8) - S0	75	13	D2
(3A8) - S1	74	9	D1
(3A8) - S2	72	5	D0
(3C2) NMI	28	57	A19
(3D5) - INTA	26	59	A18
(3B2) M2	4	61	A17
(3C5) A18/55	76	40	A16
(3C5, 3A7) A19/56	67	45	A15
(3D4, 3A3 - IORC 2A5, 2B3)	77	48	A14
(3D5, 3A3 - IOWC 2B3)	68	41	A13
(2A5) - A10WC (2A5, 3A4, - AEN 2B4, 3D8)	73	53	A12
(2A5, 3A4, - AEN 2B4, 3D8)	70	39	A11
(3A7, 3B3) ALE	78	49	A10
(3B6) SCLK	71	37	A9
(2A6) - DACK 3	64	42	A8
	3	38	A7
	25	46	A6
		50	A5
		52	A4
		54	A3
		51	A2
		47	A1
		35	A0
		82	MMA0
		81	MMA1
		84	MMA2
		83	MMA3
		58	XAI2
		62	XAI3
		60	XAI4
		63	XAI5
		65	XAI6
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		29	
		30	
		32	
		69	
		8	

TASK NUMBER REGISTER



DMA EXTENDED ADDRESS REGISTERS

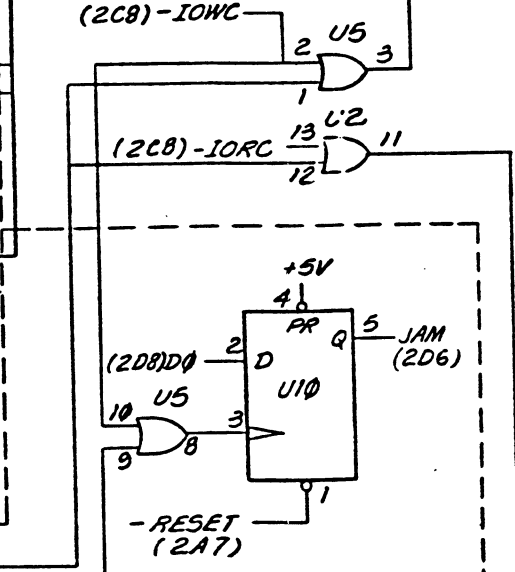
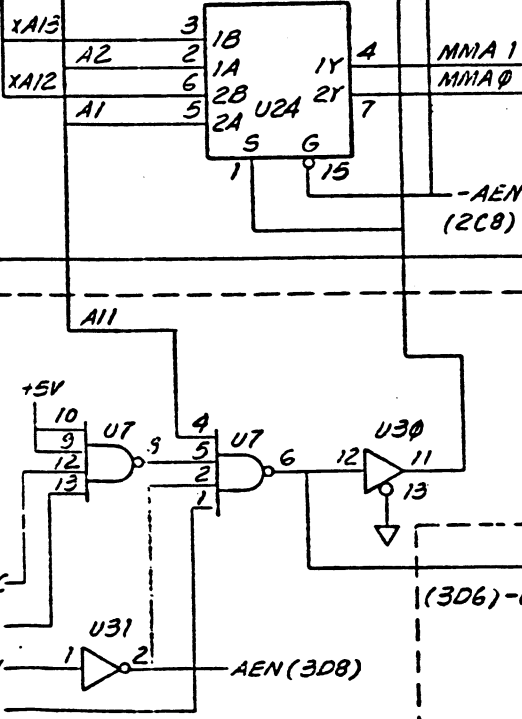
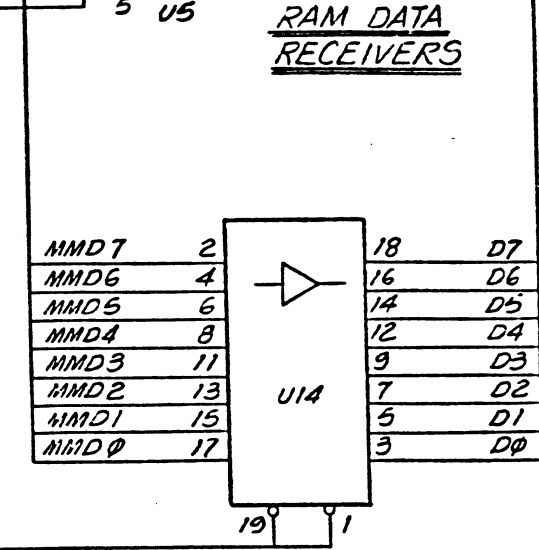
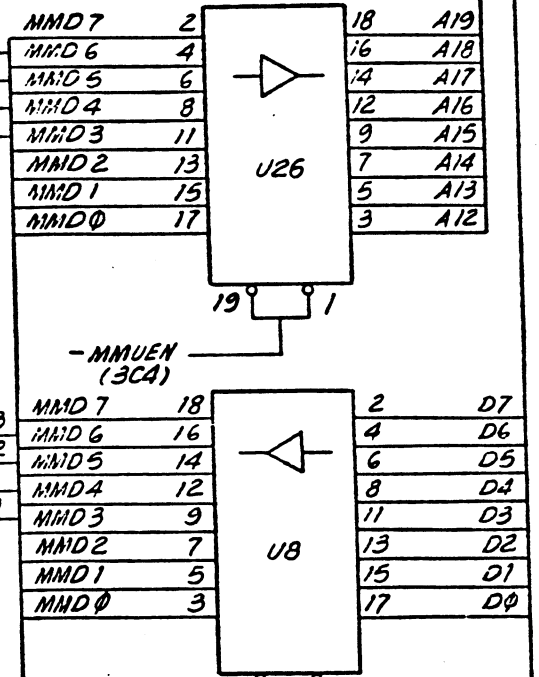
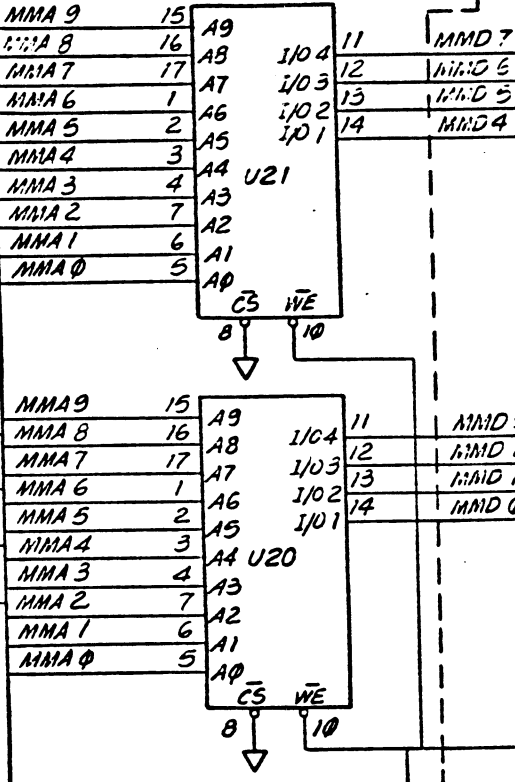
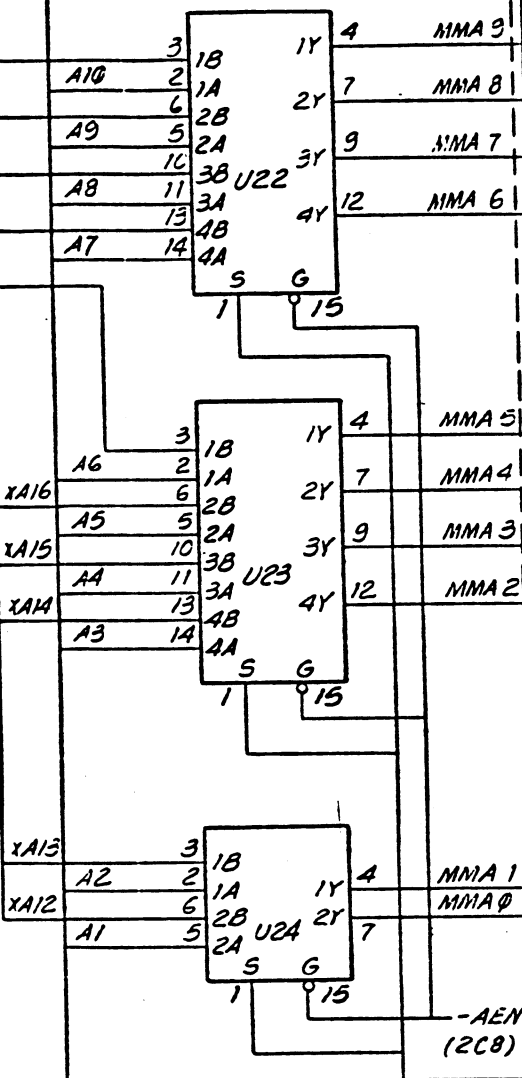


REV	ECO	DESCRIPTION	DATE	BY	CHK	APP
22		FOR 11/22/61	8/31/61	ET	L	CS

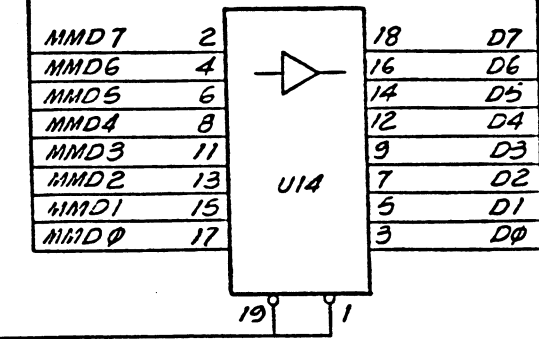
(2B7) MMA0-MMA3
RAM ADDRESS MUX

ADDRESS TRANSLATOR RAM

MM ADDRESS OUTPUT DRIVERS

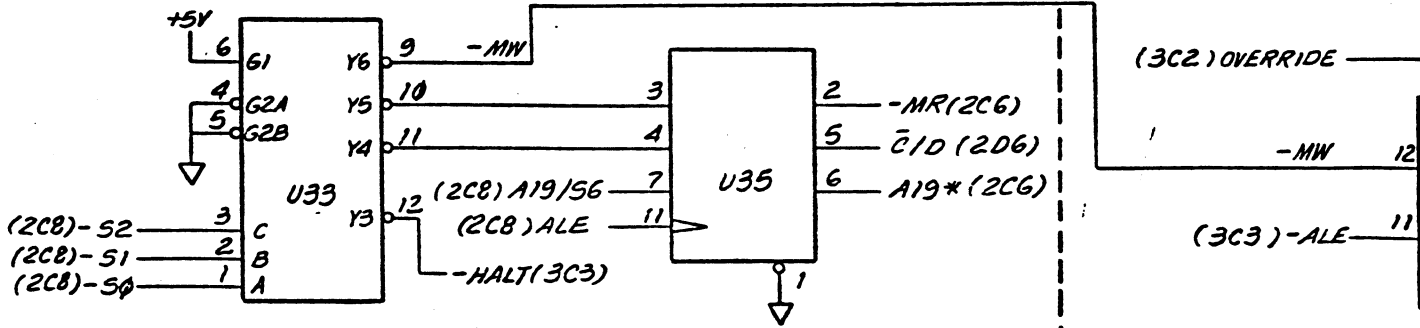
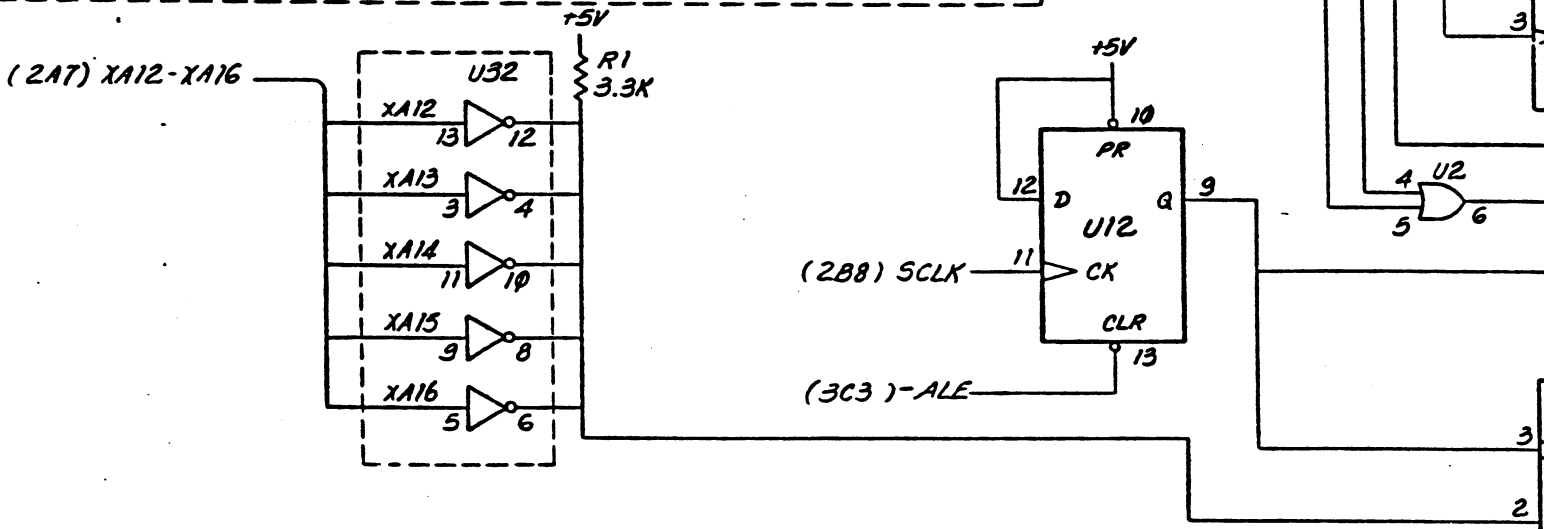
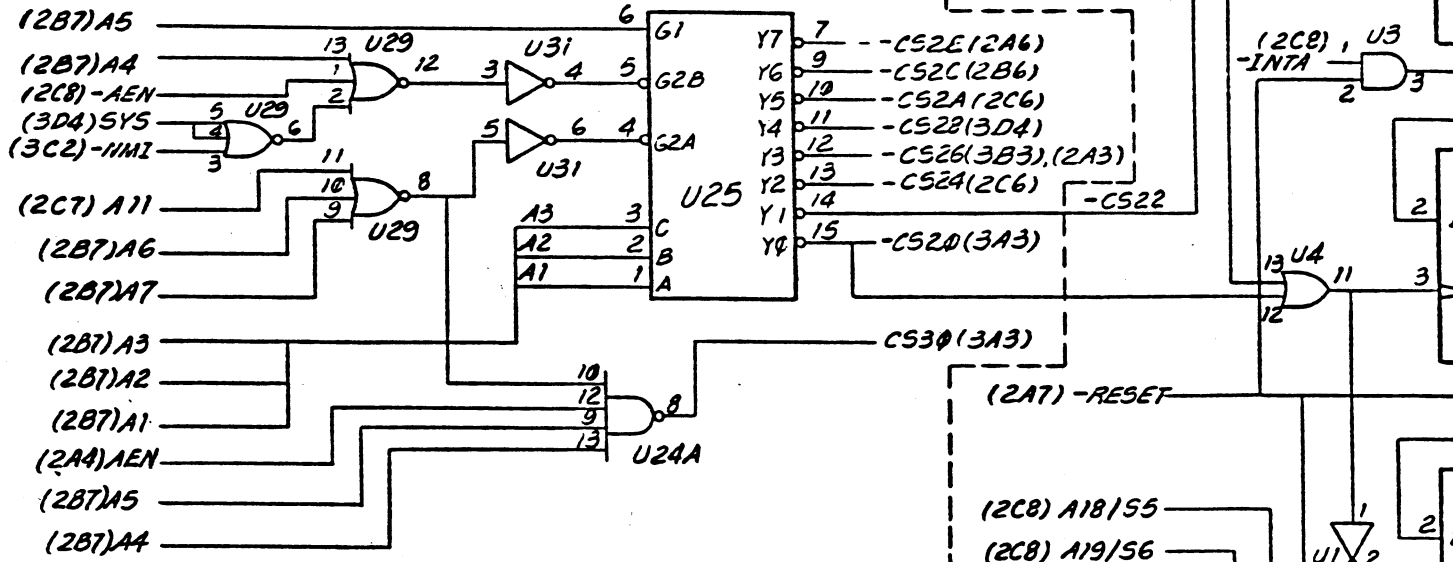


RAM DATA DRIVERS



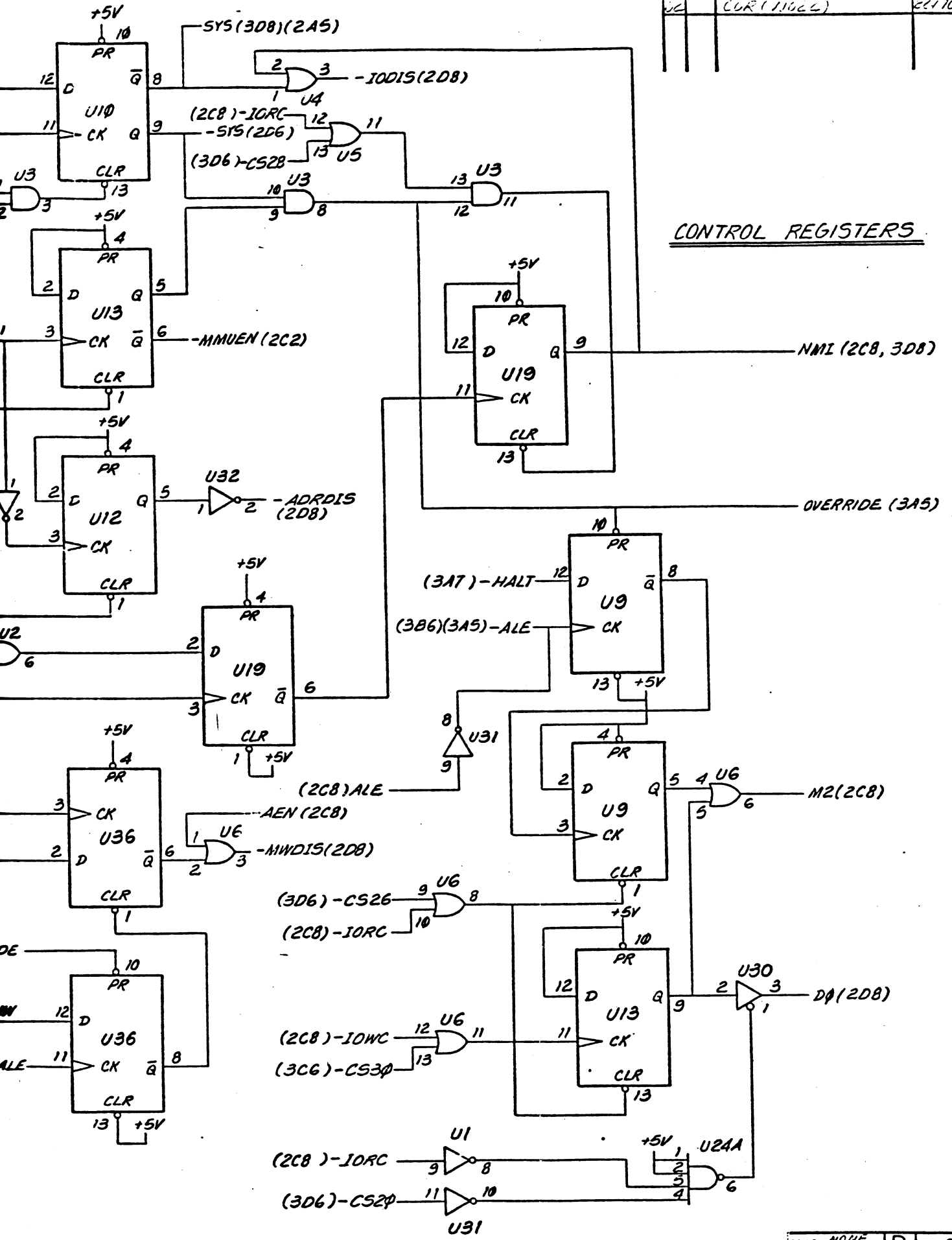
TRANSLATOR RAM ADDRESS DECODE

MMU REGISTER ADDRESS DECODER



BUS STATUS DECODER

REV	ECO	DESCRIPTION	DATE	BY	CHKD	APP
01		CLR (11022)	8/21/67	ET		



CONTROL REGISTERS