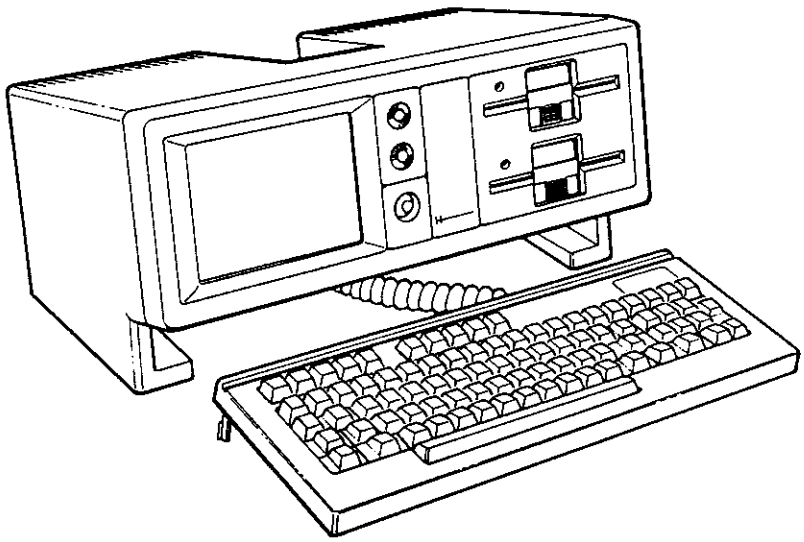
Hyperion

MAINTENANCE MANUAL



Part Number: 650000-000
BYTEC MANAGEMENT CORP

Federal Communications Commission Compliance

The Hyperion is subject to Federal Communications Commission (FCC) rules. The Hyperion has been tested and found to comply with the limits of Class B computing devices in accordance with the specifications in Subpart J of Part 15 of FCC rules. The Hyperion has Canadian Standards Association (CSA) approval, and conforms to the Government of Canada Telecommunications Interconnection Requirements (CS-03).

UL#86H2
CSA LR33921-6
FCC Ident. CTJ7YM3000
FCC Regist. CTJ7YM-704333-DT-E

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NOTE: MISSING PAGE #'S WERE BLANK IN ORIGINAL

UPGRADES/FIELD CHANGES SINCE 1983 NOT AVAILABLE

Warranty

The Dynalogic Info-Tech Corporation warrants this Dynalogic Personal Computer Product to be in good working order for a period of one year from the date of purchase from DYNALOGIC or an Authorized Dynalogic Computer Dealer. Should this product fail to be in good working order at any time during this one year warranty period, DYNALOGIC will, at its option, repair or replace this product at no additional charge except as set forth below. Repair parts and replacement Products will be furnished on an exchange basis and will be either reconditioned or new. All replaced parts and products become the property of DYNALOGIC. This limited warranty does not include service to repair damage to the Product resulting from accident, disaster, misuse, abuse, or non-Dynalogic modification of the Product.

Disclaimer

The information in this manual has been carefully prepared and checked for completeness and accuracy. There is, however, always the possibility of omission or error. In such event, Bytec cannot assume liability for any damages resulting from the use of this manual.

Warning

Circuit boards damaged by attempting IC replacement shall result in reduction or cancellation of return credits or voidance of the warranty.

Trademarks

HYPERION is a trademark of Hyperion Division of Bytec.
MS-DOS is a trademark of Microsoft Corporation.
IN:TOUCH is a trademark of Hyperion Division of Bytec.

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Addendum Sheet

Date: September 12, 1983

The Following Changes Are Required in The Manual

To Chapter 8:

The Disk Drives were modified to improve the reliability on the high tracks. The errors were noticable when running the disk diagnostics and the majority of errors occur on tracks 35 to 39. Resistors R15 and R16 were changed from 51.1 ohms to 91 ohms, 5%, 1/2 watt.

If the Disk Drive has these resistors installed the following changes are required to the Write Current Adjustment procedure:

A) Return to Track 0.

B) Install a scratch diskette halfway into the drive.

C) Connect the Volt Meter leads across R34.

D) The reading should be 350mv +/- 3mv, if this is not correct, adjust potentiometer R35 and secure with locktite.

Addendum Sheet

Date: September 7, 1983

The Following Changes Are Required in The Manual

To Chapter 3:

The diagnostic routines can be accessed by the Soft Keys (F1 to F10).

For Master Diagnostic Diskette, Part Number 740003-000 the first Soft Key line is:

LASTLN CHRSET LOWRES HIGHRS MORE ATTRIB CRTRAM RAMTST DSKTST HELP

Pressing F5 (MORE) will change the Soft Key line to:

TEST DOS PARALL SERIAL DIR/P SPEAKR MODEM DTMF CRTTST HELP

For Master Diagnostic Diskette, Part Number 740020-000 the Soft Key line is:

LASTLN SERIAL CRTTST DOS SPEAKR CRTRAM RAMTST DSKTST HELP

Page 3-16: The diagnostic program "LINEARITY" is not on the Soft Key line.

Page 3-22: By using the Soft Key F9 (CRTTST) the program will be loaded without having to load "BASICA" first.

To Chapter 8:

The programs for adjusting the CRT without using "BASICA" are not on the Soft Key line. If the programs do not remain on the screen, if may be necessary to use "CTRL + S" to lock the display on the screen.

Addendum Sheet

Date: November 10, 1983

The Following Changes Are Required in The Manual

General

The Maintenance Manual does not clearly state which Diagnostic Diskette to use with each revision of Hyperion. The Master Diagnostic Diskette Rev 01 is to be used with Revision 5 Hyperions, the Master Diagnostic Diskette is for use with Revision 4 Hyperions.

To Chapter 3:

The Attributes section of the CRT TEST does not have Reverse Video as shown in the manual (Fig 3-8 and Fig 3-11). The SOFT KEY LINE is reverse video so if this line is present, the reverse video works. The line which contains SUPERSCRIPT and SUBSCRIPT has the word "BOTH" super and subscripted, not "CONTAINS" superscripted and "BOTH subscripted as shown. Because Superscript moves up one line and Subscript moves down two lines, "BOTH" is down only one line.

On page 3-11, the Voltage levels for V1 are shown as +5.25 for both Max and Min. The correct values are +5.25 for Max, +4.75 for Min.

1.0 Introduction

The Hyperion portable computer is a powerful 16-bit microcomputer with full graphics and optional built in telecommunications capability. Most of the advanced circuitry is contained on two densely populated multi-layer printed circuit boards, which makes the Hyperion one of the smallest and easiest computers to repair.

This manual is intended to assist in isolating problems to the sub-assembly level, then to provide factory approved removal and replacement techniques. The Diagnostic Diskettes are used with the Fault Analysis Charts (FACs) in Chapter 3, to provide rapid fault isolation. The two diskettes contain the same programs, however, they are used with different revisions of computer. Refer to Chapter 3 for details of which diskette to use with each revision. The removal and replacement techniques will assist in correcting problems and provide for testing to verify fault correction (Chapter 4).

A Bytec Hyperion Maintenance Course is available to authorized dealer technicians. This course provides detailed technical information and hands-on repair experience. Anyone attempting repair of the Hyperion without benefit of the course is encouraged to seek technical assistance from the nearest authorized dealer.

Throughout this manual various types of precautionary information is included:

Warning A WARNING indicates that procedures detailed could cause personal injury or serious equipment damage if suitable precautions are not taken.

Caution A CAUTION indicates that minor damage may result if suitable precautions or normal work practices are not taken.

Note A NOTE indicates steps to be taken to make the particular procedure easier to carry out.

2.0 Hyperion Block Diagrams

Complete System (Fig. 2-1)

The System Block Diagram illustrates the relationship between the System Board and the Keyboard, Disk Drives, Speaker, Fan, Display and I/O Board, Display Unit, and Modem Board.

System Board (Fig. 2-2)

The System Board contains the DRAM, System Clock, CPU, EPROM, and the DMA and Floppy Disk Controller. The Boot Strap Program and Hyperion-On-Self-Test (HOST) Programs are stored on the system EPROM.

Display and I/O Board (Fig. 2-3)

The Display and I/O Board contains the Real Time Clock, outputs and inputs to the CRT, Modem and Parallel/Serial interface.. The CRT enhancement circuitry for alpha/graphics plus the Video Driver are located on this board. The optional Modem Board plugs into the Display and I/O Board in piggy-back fashion.

Modem Board (Fig. 2-4)

The Modem Board provides the auto-dial, auto answer, telephone line interface and a 300 baud Modem. The programmable speaker volume control is also located on this board.

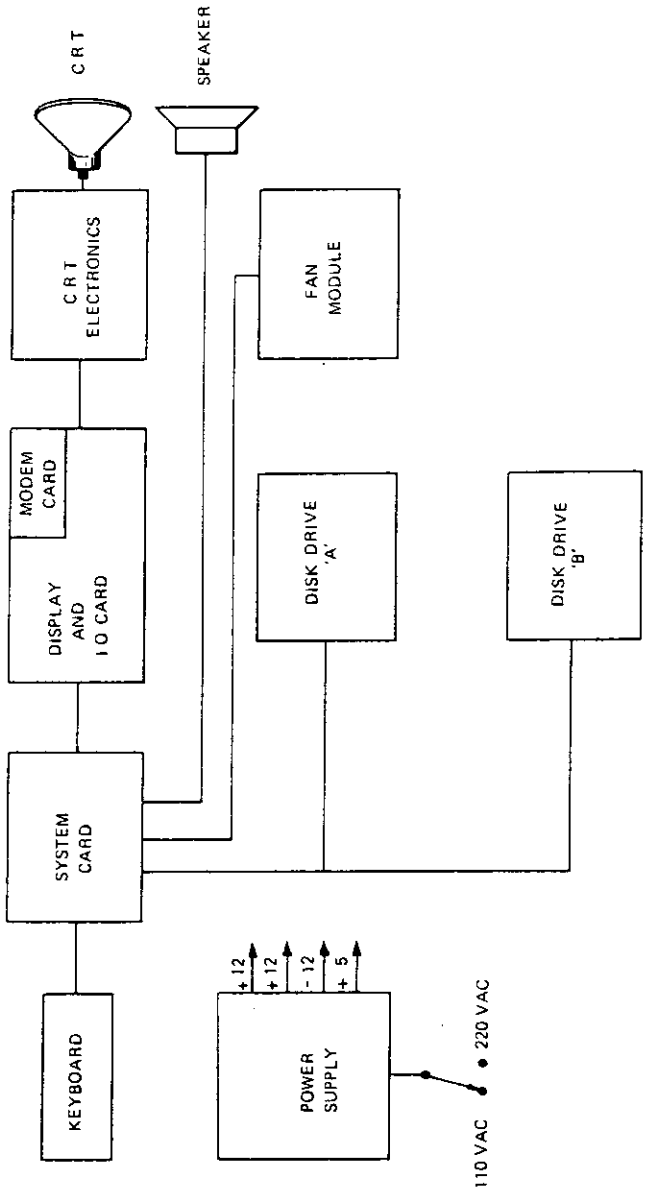


Fig. 2-1 – Hyperion Block Diagram

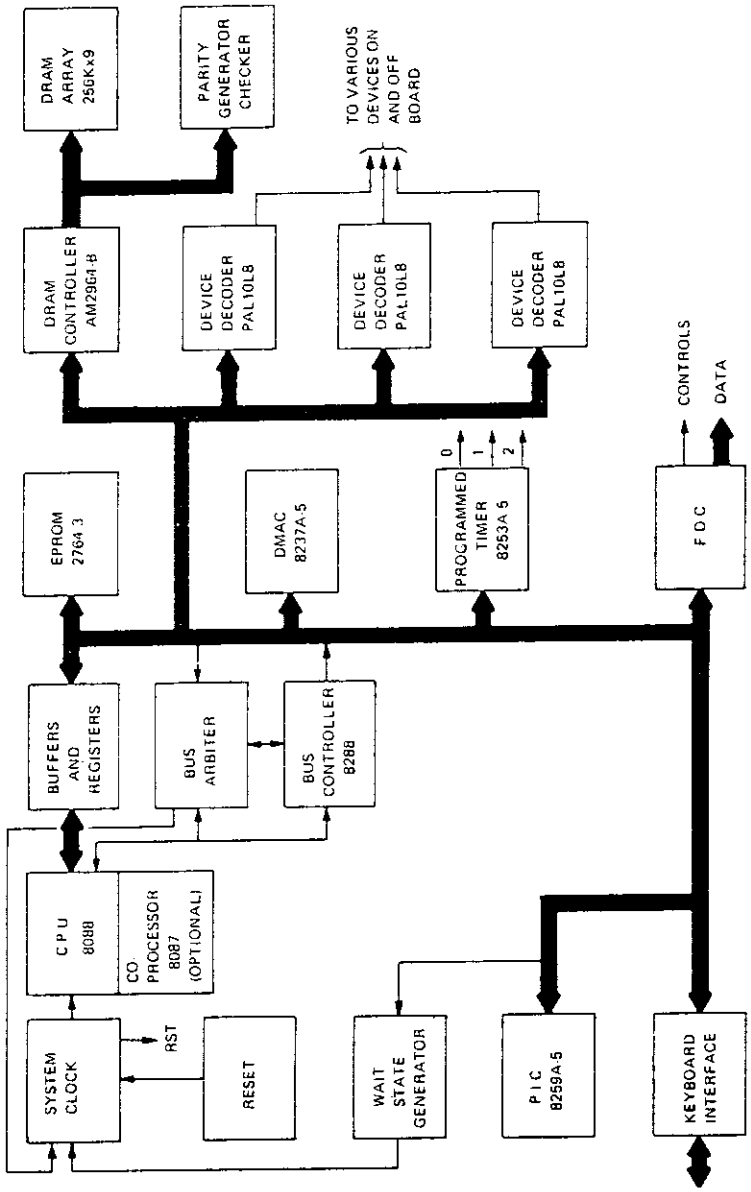


Fig. 2-2 – System Board Block Diagram

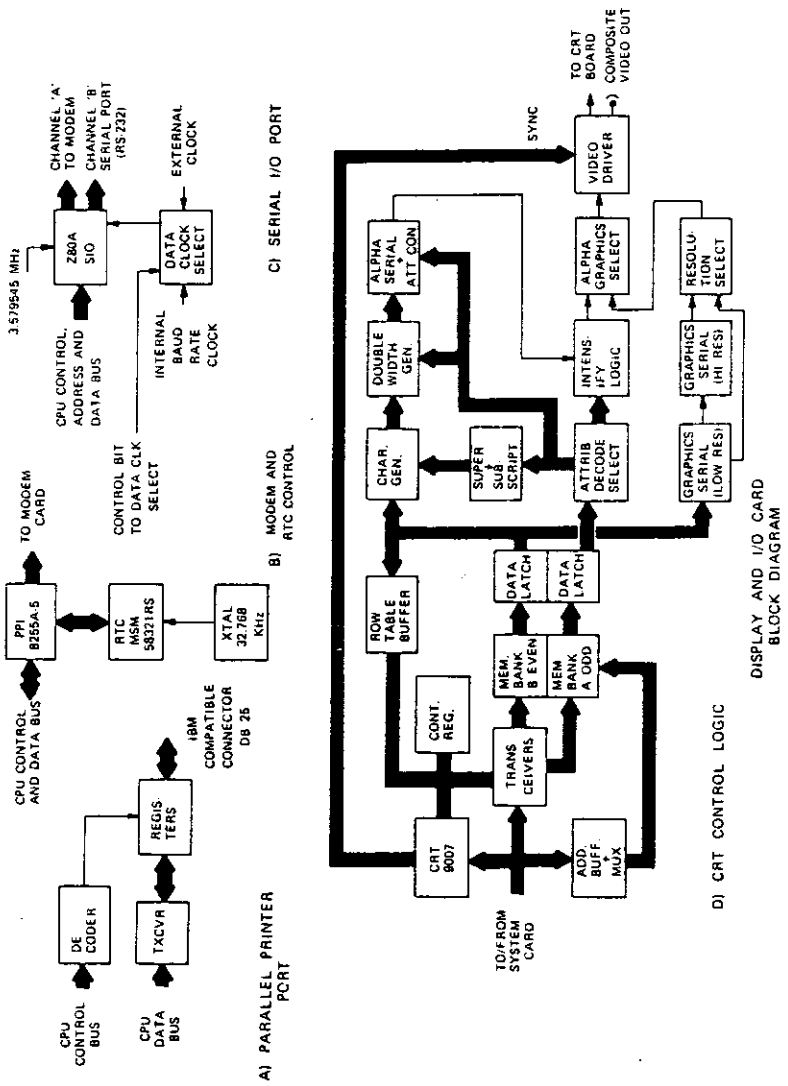


Fig. 2-3 – Display & I/O Board Block Diagram

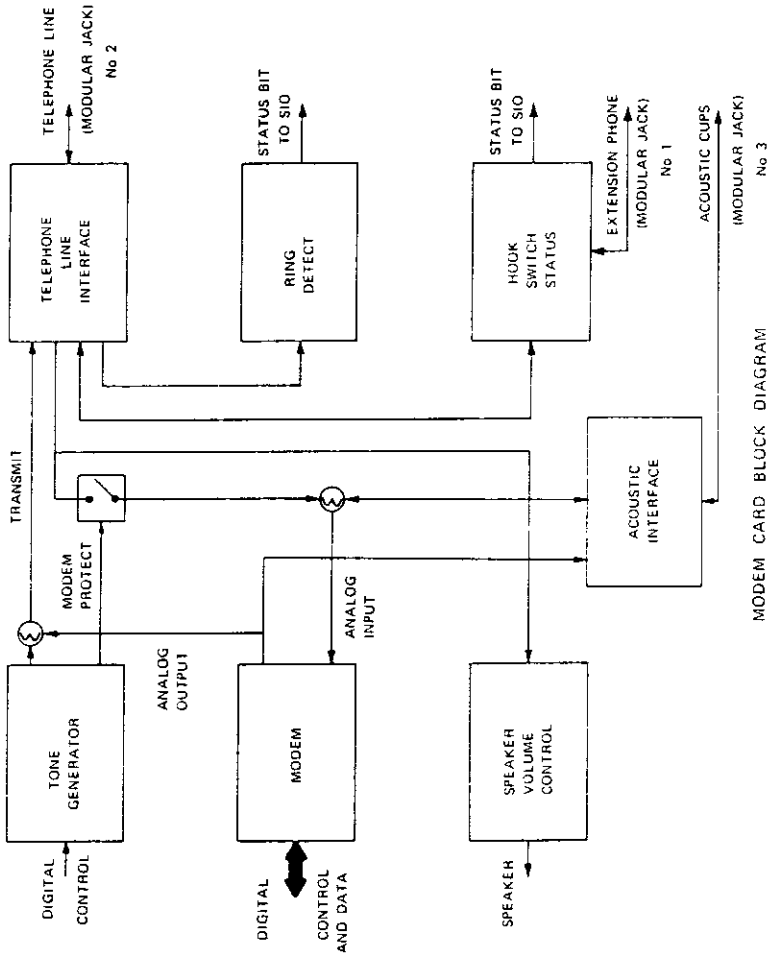


Fig. 2-4 – Modem Board Block Diagram

3.0 Fault Analysis Charts (FAC's)

How To Use This Chapter

1) Always begin with the START FAC.

2) The START FAC will refer you to one of the other FAC's numbered from 2 to 10.

3) The sub-assembly FAC will guide you through mechanical, electrical and diagnostic tests which will help isolate the failed sub-assembly.

4) The removal/replacement section will guide you to repair completion.

Start

This is the entry point for all fault isolation. The equipment you need for fault analysis is:

a) Wrap around plug kit

b) Hyperion Diagnostic Diskette

c) Standard hand tools

The hand tools should consist of:
Diagional cutters
Needle nose pliers
Phillips screw driver
Socket wrench or nut-driver set
Right angle dental pick

d) Standard spares kit

1) Before applying power, check the AC line cord and keyboard cable for damage

2) Connect the AC line cord to a known good AC outlet and turn the system ON.

3) Under normal conditions the AMBER ON button will light when power is applied.

Does The Power Light Come On?

No – Go to Power FAC 2.0. If the power is good, replace ON switch light bulb.

Yes – Next page.

Normal Power-Up

When a properly working Hyperion is powered ON and a Diagnostic Diskette is inserted, the following responses are normal:

1) 10-15 second warm-up period

2) Diagnostic program boot-up

3) The following will appear on the display:

```
Hyperion (TM) Dynalogic Info-Tech Corporation

Beta Test 09 Dec 82

MS-DOS version 1.25
Copyright 1981,82 Microsoft, INC

Current date is Mon 4-04-83
A:
```

Note The information displayed on the screen may not be identical to above, depending on the version of diagnostic diskette. The above is only a typical screen format.

If the diskette does not load properly, try to load from the other Disk Drive. If this works run the Disk FAC to confirm Disk Drive failure.

Does The Hyperion Power-Up Properly?

Yes – Refer to Running Specific Diagnostic Section in this chapter to choose the diagnostic program to run.

No – Next page

Hyperion-On-Self-Test (HOST)

When a malfunctioning Hyperion is powered up, the system may fail its start-up diagnostics. These diagnostics test only some major sub-assemblies. The system will not boot if it fails these diagnostics.

The error messages are:

Error Message	Probable Cause
Memory Fault	CRT RAM, System RAM or EPROM The area at fault is determine from the address reported. The DRAM is located from 00000 to 3FFFF. The CRT RAM is located from B0000 to BFFFF. The EPROM is located from F8000 to FFFFF.
Parity Fault	System RAM
Keyboard Fault	Keyboard/System Board
Disk Fault	Disk Drive/System Board

Keyboard fault codes are:

1) "ABFF" indicates a problem in RAM or ROM.
2) "ABXX" where "XX" is the key number of the stuck key.
3) "FF" indicates a keyboard is not connected.

Is There A HOST Error Message?

Yes – The system is hung in this state. You will have to rely on DC electrical testing and sub-assembly replacement to isolate the fault. If you cannot isolate the problem—Seek technical assistance.

No – Connect an external monitor to isolate a possible CRT failure, refer to FAC 3.0. If the CRT is GOOD continue to next page. NOTE: It may be necessary to adjust the vertical and horizontal sync of the monitor to match the Hyperion.

Non-Functioning Computer

When a system fails to boot-up, the following observations can be made:

1) Diskette will not load.

2) CRT will be blank.

3) Continual reset has no effect.

4) AMBER ON light is illuminated.

Note The system is non-operational. Refer to Power FAC 2.0 for voltage checks; if the voltages are good, proceed with sub-assembly replacement to determine fault.

Running Specific Diagnostics

Review the problem symptoms and conduct a physical examination for obvious faults that would relate to the following subassemblies:

1)	Power Supply	FAC-2.0
2)	CRT and its controls	FAC-3.0
3)	Disk Drives	FAC-4.0
4)	System Memory	FAC-5.0
5)	CRT Memory	FAC-6.0
6)	Serial I/O	FAC-7.0
7)	Parallel I/O	FAC-8.0
8)	Speaker	FAC-9.0
9)	Modem	FAC-10.0

Does the Symptom Relate to any of the Above Assemblies?

Yes – Use the appropriate FAC and diagnostic program to confirm problem isolation and repair. Carry out repairs and re-test.

No – Next page.

Voltage Check

You have entered this FAC because you suspect a fault in the Power Supply or the power distribution system. You have already checked the AC line cord and are certain that the AC wall plug is good.

The Power Supply used in the Hyperion is a switching type which requires a load on the output to produce the correct voltage. The DC voltage levels must be checked while the Power Supply is sufficiently loaded down.

The following loads are required on the output voltage lines.

Voltage	Load (OHMS)	Pin Numbers	Voltage Max	Min
Common		1,11,12,13		
V1	1.1	10,9,8,	+5.25	+5.25
V2	25	2	+12.6	+11.4
V3	25	7,6,5,	+12.6	+11.4
V4	100	4	−12.6	−11.4

If there is a short on a board, a clicking noise can be heard from the power supply.

Are The Right Voltages Measured?

No – If all of the voltages are missing, check the fuse and if it is GOOD, replace the Power Supply. If some of the voltages are missing or incorrect, replace the Power Supply.

Yes – Next page.

Power Harness Check

It is still suspect that a power problem is possible. You are now going to check the power harness.

1) Turn the AC power off.

2) Remove each connector from the sub-assemblies.

3) Measure the resistance to check the continuity of the harness.

Do The Cables Have Continuity?

No – Replace/repair the harness.

Yes – You have now eliminated the Power Supply and harness as a possible fault. Return to START FAC if problem still persists.

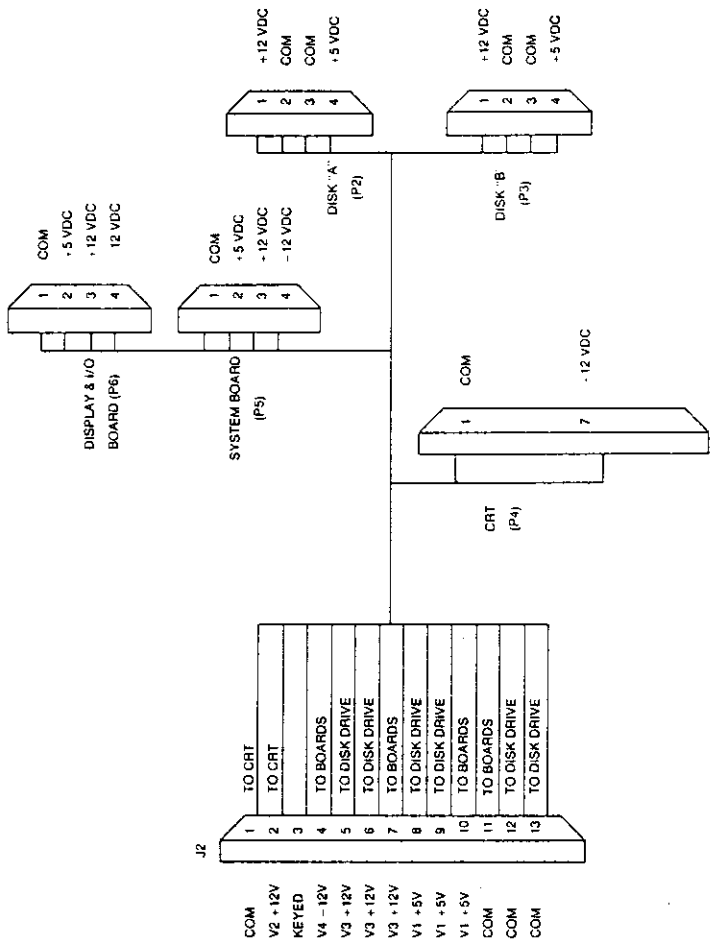


Fig. 3-1 – Power Harness Voltages

CRT Diagnostics

You have entered this FAC after doing the Start FAC and are now trying to isolate the cause of a malfunctioning screen.

1) When a Hyperion boots up it is normal to observe the standard diagnostic information as follows:

```
Hyperion (TM) Dynalogic Info-Tech Corporation

Beta test 09 Dec 82

MS-DOS version 1.25
Copyright 1981,82 Microsoft, INC.

Current date is Mon. 4-04-83
A:
```

2) If there is an obvious distortion or error in the screen information, connect an external monitor via the external video jack and compare the screen information.

3) If the CRT requires adjustment refer to Chapter 8.

4) There are two versions of CRT diagnostics for the Hyperion. One version will work on all boards with serial numbers up to 2500. The other version uses BASICA so it will only work on those Boards with serial numbers 501 and up. Both versions will be detailed, the one which does not require BASICA will be first.

Does The Correct Image Appear on the External Monitor?

No – Replace the Display and I/O Board.

Yes – Replace the CRT assembly and re-run the diagnostics.

CRT Tests Which Do Not Require BASICA

Linearity Test

This diagnostic is intended to test the focus, centering, tilt or curvature of the display.

Select diagnostic "LINEARITY", the following will appear on the screen.

Fig. 3-2 – CRT Display Quality

Is the Display: Dim? Too Wide? Too narrow? Too short? Too small? Wavey? Not centered? Out of focus?

Yes – Adjust the CRT and re-run the diagnostics.

No – Next page.

Character Generator Test

This diagnostic test is designed to test the character generator located on the Display & I/O Board.

Select diagnostic "CHARSET".

The program sets up the following display:

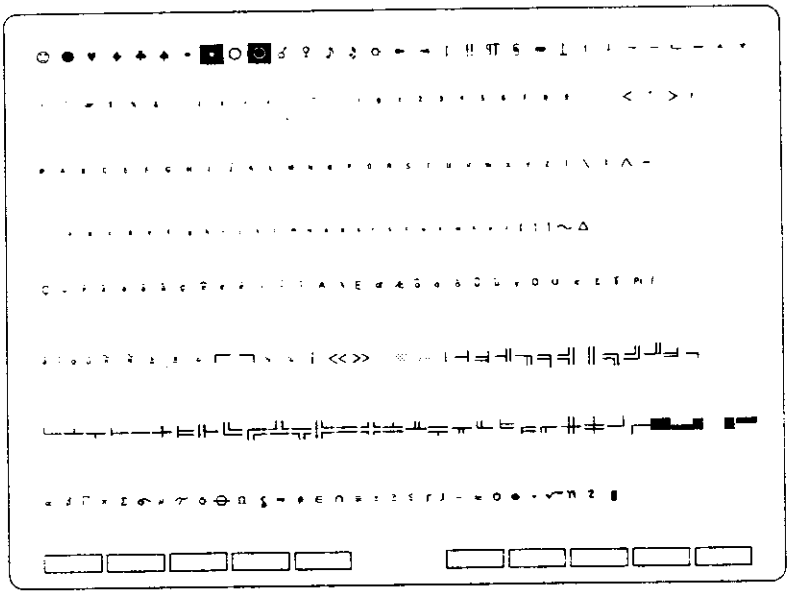


Fig. 3-3 – Character Set Diagnostics

Check that each character is complete and in the same position as above.

Did Character Generator Test Pass?

No – Replace the Display and I/O Board and re-run diagnostics.

Yes – Next page.

Display Attributes

This diagnostic checks the display attributes.

Select diagnostic "ATTRIBUTES", and check that the display is as below.

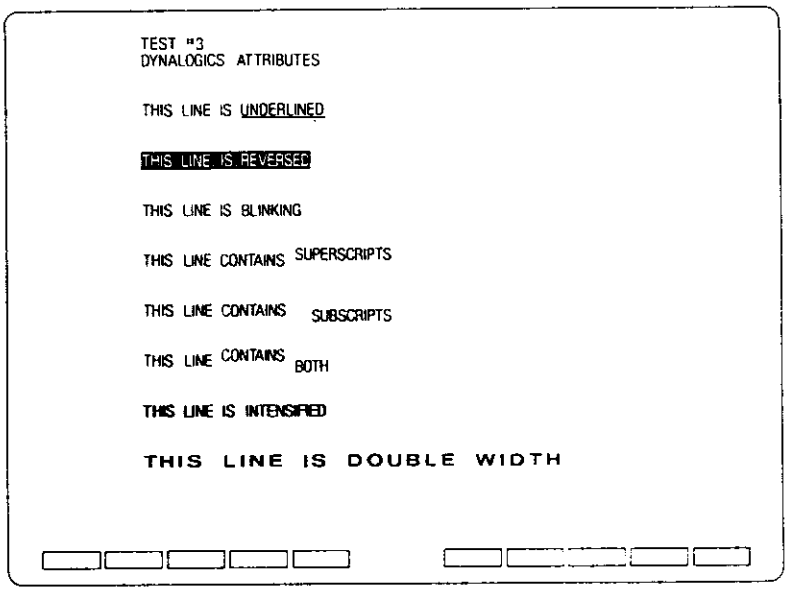


Fig. 3-4 – Attributes Diagnostics

Did The Display Attributes Pass?

No – Replace the Display & I/O Board.

Yes – Next Page.

Display Graphics

This diagnostic checks the Low Resolution graphics.

Select diagnostic "LOWRES".

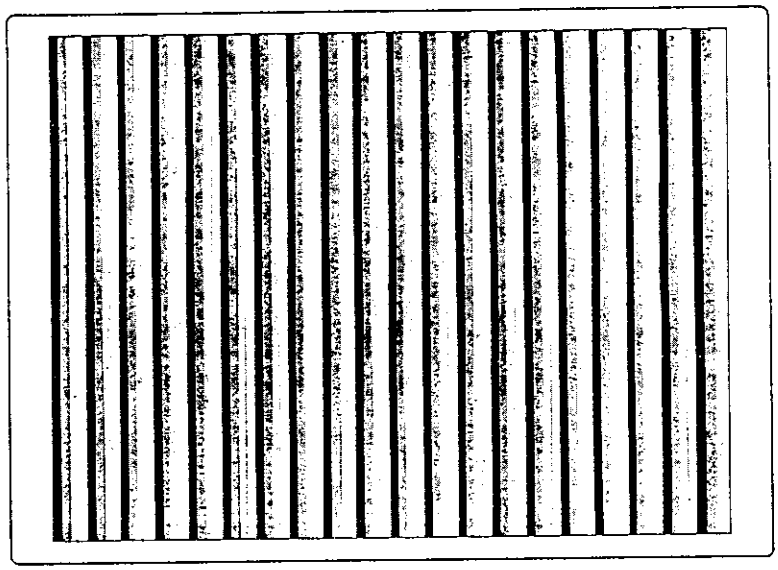


Fig. 3-5 – Low Resolution Diagnostics

Did Low Resolution Graphics Test Pass?

No – Replace the Display & I/O Board.

Yes – Next page.

This diagnostic tests the High Resolution Graphics.

Select diagnostic "HIGHRES".

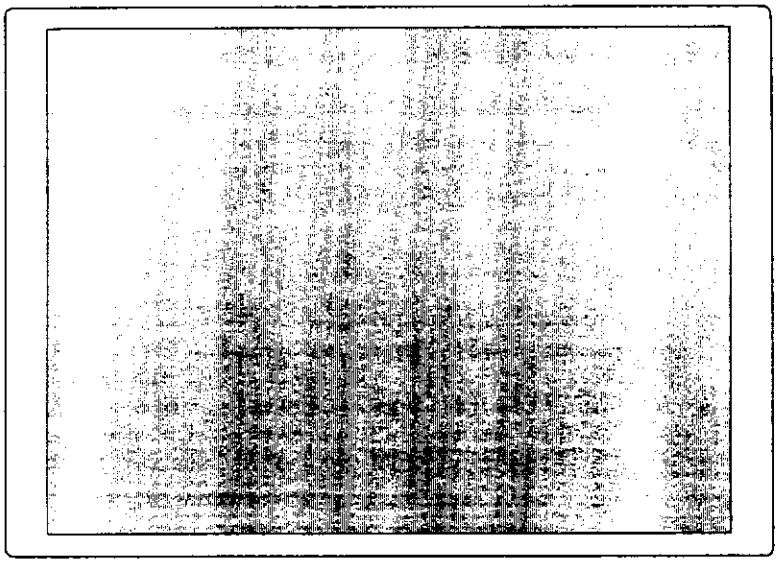


Fig. 3-6 – High Resolution Diagnostics

Did High Resolution Graphics Test Pass?

No – Replace the Display & I/O Board.

Yes – If the Hyperion has passed all of the CRT diagnostics and there is still a CRT problem, seek technical assistance.

CRT Test Which Require BASICA

This is a group of tests linked together which provide patterns for CRT alignment as well as the Character Set, Attributes, Low and High resolution graphics. The test is executed by:

1) Type: BASICA and Rtn. The screen will display the following:

```
Dynalogic Hyperion (TM)
BASICA version 1.00B
(C) Copyright Microsoft 1982
59866 Bytes Free
OK
```

2) Type: Run"CRTTST. The screen will display the following.

```
Hyperion CRT/Display Test (820035-000-02)

60Hz. CRT TEST PATTERN- CRT alignment
70Hz. CRT TEST PATTERN- CRT alignment
CHARACTER SET- Verify integrity of Character Generator
ATTRIBUTES DISPLAY- Verify all Attribute functions
LOW RESOLUTION GRAPHICS- Verify the four levels
HIGH RESOLUTION GRAPHICS- Check the quality of the
display


To change the display use the following: To move to the next
display type, the 'CURSOR RIGHT' key
To move to the previous display, type the 'CURSOR LEFT'
key
To exit to DOS type the 'E' key
```

3) The 60Hz and 70Hz test patterns are used for adjusting the CRT. Refer to Chapter 8 for the procedure.

4) The other four tests are similar to those previously explained.

Character Generator Test

This diagnostic is designed to test the character generator located on the Display & I/O Board.

The program sets up the following display:

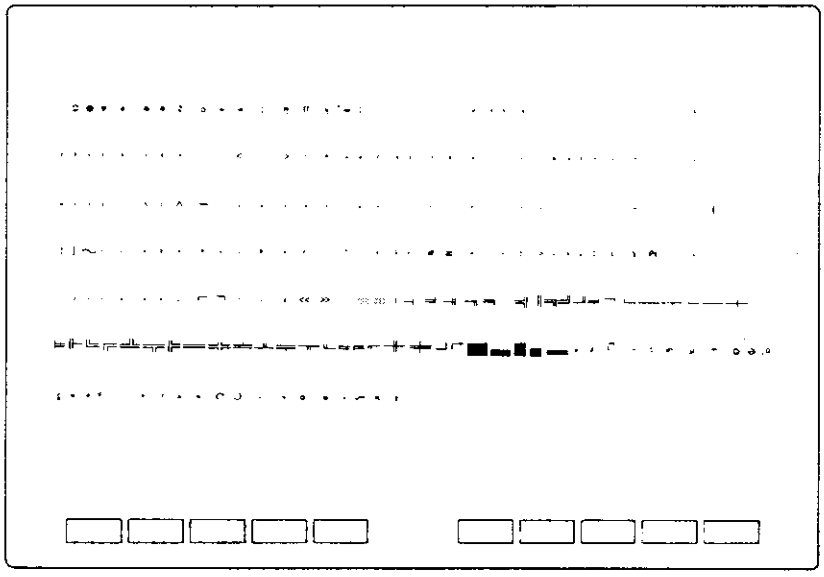


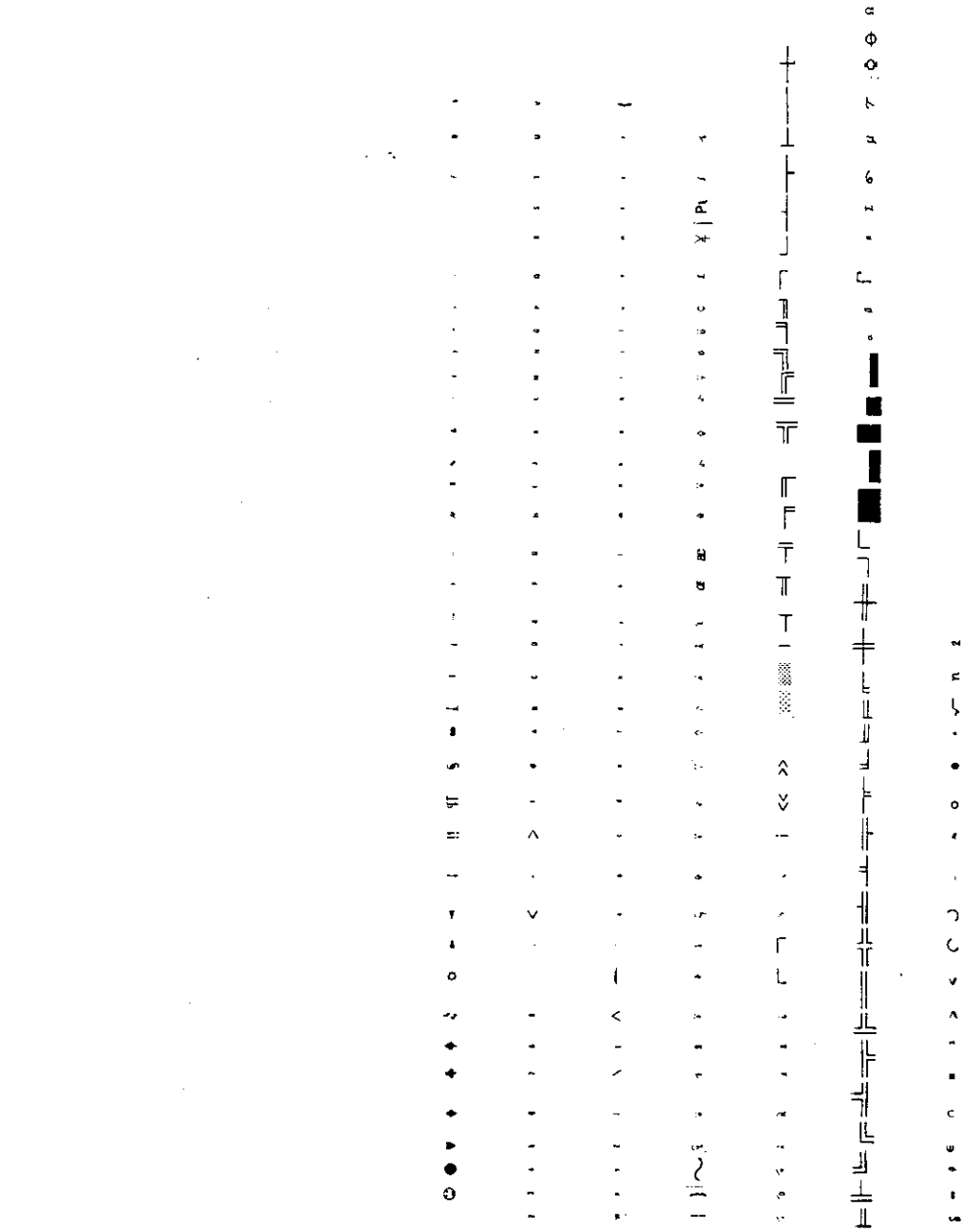
Fig. 3-7 – Character Set Diagnostics REV01

Check that each character is complete and in the same position as above.

Did Character Generator Test Pass?

No – Replace the Display & I/O Board and re-run diagnostics.

Yes – Next page.



Display Attributes

This diagnostic checks the display attributes.

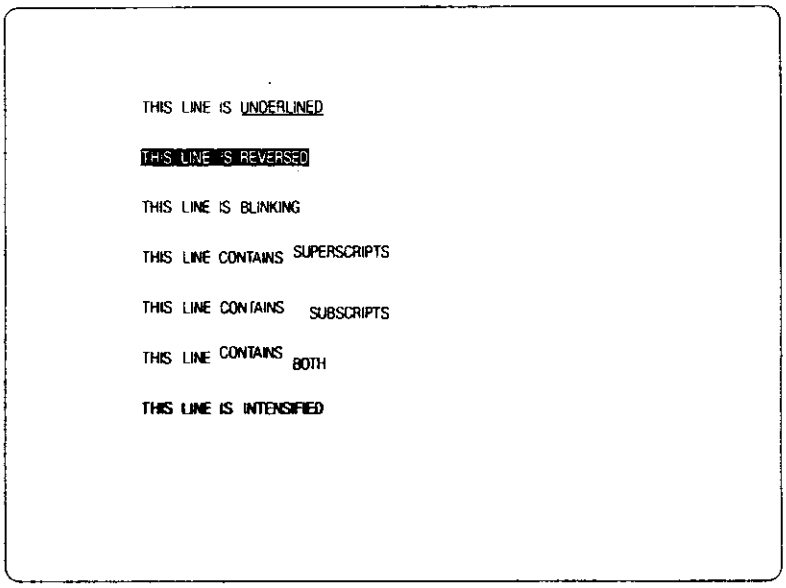


Fig. 3-8 – Attributes Diagnostics REV01

Did Display Attributes Test Pass?

No – Replace the Display & I/O Board.

Yes – Next page.

Display Graphics

This diagnostic checks the low resolution graphics.

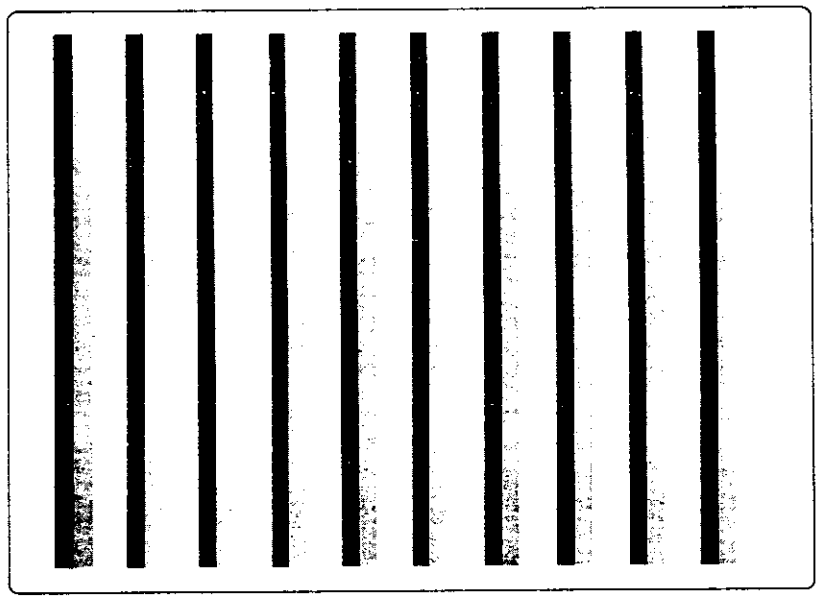


Fig. 3-9 – Low Resolution Diagnostics REV01

Did Low Resolution Graphics Test Pass?

No – Replace the Display & I/O Board.

Yes – Next page.

This diagnostic tests the high resolution graphics.

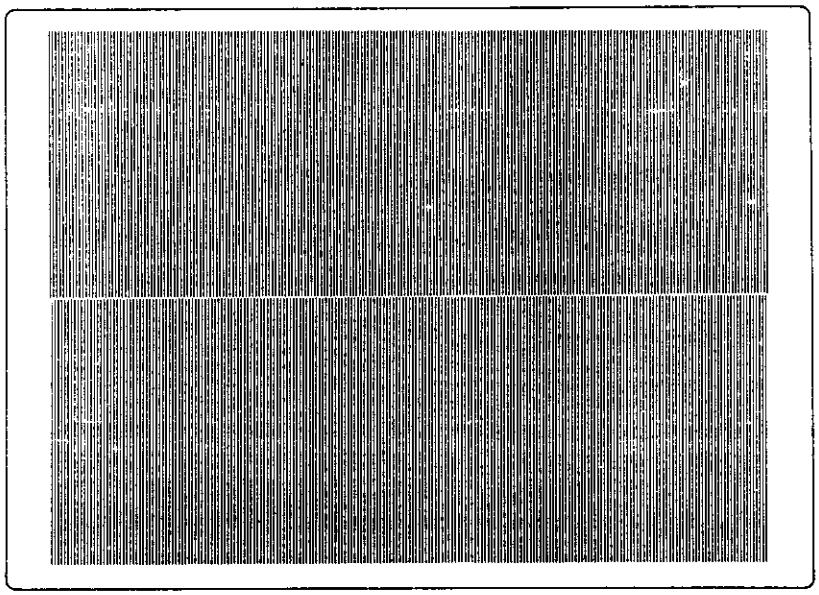


Fig. 3-10 – High Resolution Diagnostics REV01

Did High Resolution Graphics Test Pass?

No – Replace the Display & I/O Board.

Yes – Next page.

40 Character Mode

This diagnostic checks the display attributes in 40 character mode. This diagnostic test is on Diagnostic Diskette REV01 only.

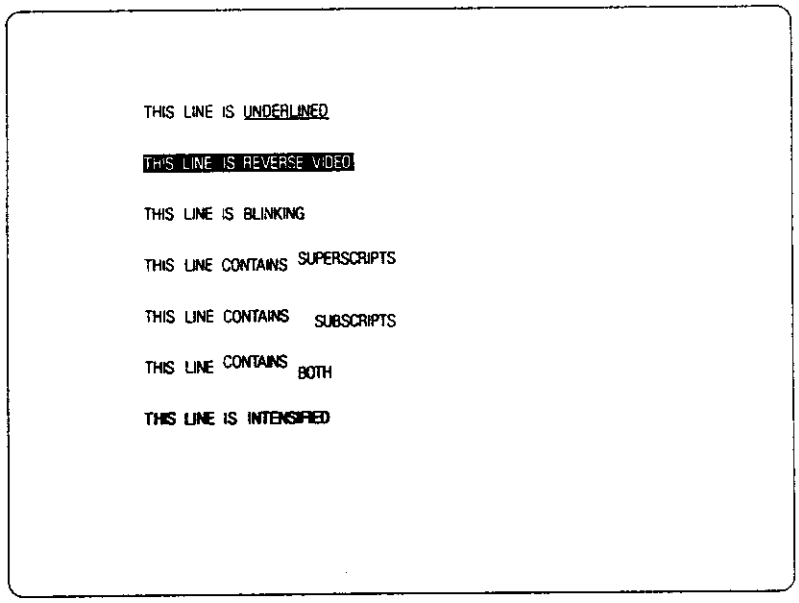


Fig. 3-11 – Attributes Diagnostics 40 Character Mode REV01

Did 40 Character Mode Pass?

No – Replace the Display & I/O Board.

Yes – If the Hyperion has passed all of the CRT diagnostics and there is still a CRT problem, seek technical assistance.

Disk Test

You have entered this FAC because of a HOST error message, a failure to load, or suspected random read/write errors.

1) Under HOST error conditions you cannot even load your diagnostics.

2) If there is no HOST error continue to next page.

3) Ensure the diskette is good.

4) Insert diskette into other drive and re-boot.

5) Inspect all wiring harnesses and power cables. Refer to Power FAC as required.

Note Random read/write errors will occur on Drive "B" if the fan is not operational.

The Disk Drive head cleaning kit should only be used when errors occur running Disk Test. It should not be used on a regular basis as rapid head wear may result.

Does the Error Continue?

Yes – Replace the System Board or Disk Drive that was faulty.

No – Next page.

Reliability Test

The reliability test is designed to isolate read/write errors.

The types of errors normally associated with the Drives are, Hard, Soft and Seek.

Soft errors are usually caused by:

1) Airborne contaminants that pass between the read/write heads and the disk. These contaminants are usually removed by the cartridge self-cleaning wiper.

2) Random electrical noise which usually lasts for a few microseconds.

3) Small defects in the written data and/or track not detected during the write operation.

4) Worn or defective media, known good media must be used when running this test.

Soft errors are normally recovered by rewriting or rereading the diskette on the next revolution.

If unsuccessful after 10 tries at writing/reading the data, the error is classified as Hard.

Seek errors result when the stepping rate exceeds 5msec.

A "small" number of soft errors are acceptable since they are automatically recovered by the Floppy Disk Controller (FDC), and will not affect normal system operation. A "large" number of soft errors may indicate problems in the hardware which may worsen with time and are not acceptable. Hard errors may indicate defective diskette media, dirty or worn read/write heads, or a fault in the drive or FDC electronics.

When using Disk Test, error information is displayed on the screen when detected. In addition, a summary of the number of accumulated errors are displayed after each pass. Soft error reporting indicates the type of error, drive, cylinder, head and sector number. Also, the number of failed retries is displayed. Errors which repeatedly occur at the same place on the diskette may indicate "bad spots" on the diskette.

Select diagnostic "DISKTEST"

The following will be displayed:

```
Welcome to Hyperion DISKTEST (820030-000-03)

Test Reliability, Interchangeability, Read Master Diskette, Write
Master Diskette or Exit, your choice? (R,I,M,W,E,) "_".
```

Select option "R" and disktest will prompt:

```
Insert scratch diskette in drives to be tested. Ready to proceed?
(Y/N) "_"
```

Select option "Y" to start testing or option "N" to exit back to MS-DOS.

Single Drive Hyperions may be tested by entering the choice (P), which will allow the user to configure Disktest to suit the Hyperion under test.

Select option "P" and disktest will prompt:

Choose one of the following:
0 = Exit program
1 = Write Master Diskette
2 = Read Master Diskette
3 = Reliability Test
4 = Interchange Test

Your Choice

Select option "3" and the screen will display:

How many Drives in system	Enter "1"
Double sided Drives (Y or N)	Enter "Y"
Data Word (in Hex)	Enter "6DB6"
How many passes (Decimal)	Enter "100"
How many random Read/Writes (dec)	Enter "100"
How many interdrive transferes	Enter "0"

Insert scratch diakette in Drive(s) to be tested
Ready to proceed? (Y/N) "_"

Does The Random Error Continue?

Yes – Replace the appropriate Drive or System Board as directed by the error message. If there are a large number of errors on both drives, the problem may be with the System Board.

No – Run the test multiple times to confirm a good system. If the system does not fail it is GOOD.

Interchangeability Test

This test is run if there is a suspected compatibility problem between the Drives. This test cannot be used on single drive Hyperions.

Select Disktest, then the option "I". Disktest will prompt:

```
Insert scratch diskettes in Drives A B.
Ready to proceed? (Y/N) "_".
```

By selecting option "Y" the diskettes will be formatted and written with data. When completed the program will prompt:

```
Now interchange diskettes between A & B.
Ready to proceed? (Y/N) "_".
```

By selecting option "Y" the diskettes will be verified. Following verification you have the option of continuing or terminating testing.

Is There an Error Message?

Yes – Replace the Drive which failed.

No – Next Page.

Read/Write Master

If there is a suspected compatibility problem between Hyperions, select Disktest, then option "W". Disktest will prompt:

```
Drive # (A or B)? "__".
Insert diskette in drive.
Ready to proceed? (Y/N) "__".
```

By answering "Y" the diskette will be formatted, filled with data and verified before returning to the initial menu.

This "master" can now be read on a known GOOD Hyperion by loading the diagnostic diskette, selecting Disktest, then option "M". Disktest will prompt:

```
Drive # (A or B)? "__".
How many passes? (decimal) "__".
Insert master diskette in drive.
Ready to proceed? (Y/N) "__".
```

By answering "Y" the diskette will be verified until the selected pass count is reached. The program will then return to the initial menu. This master should be read from both drives. To further test the Hyperion, a master should be produced on a known GOOD machine and read on the Hyperion which is suspect. Read/Write Master can be used to test a single drive Hyperion.

Is There an Error Message?

Yes – Replace the Drive which failed.

No – Drives pass compatibility test.

DRAM Diagnostics

This FAC has been entered due to a HOST error message or an error message during use. A random error can occur periodically and is difficult to isolate. The best means of checking the computer reliability is to run the RAM test multiple times.

When RAMTEST is running, the system must be powered down, then up, to re-boot as this test overwrites all MS-DOS commands stored im memory.

RAMTEST uses several different test patterns run in sucession to test the 256K of DRAM. Each pattern is designed to detect a particular hardware fault. The DRAM is divided into four segments of 64K each and is tested one segment at a time.

BYTE TWO PASS
This does a write then a read up the segment under test with the following patterns, 00H, FFH, 55H and AAH, checking for open and stuck bits.

CHECKERBOARD
55H and AAH are written in alternate bytes then verified. A write pass and verification pass with the complimentary checkerboard AAH/55H is then done.

WALKING ADDRESS
This uses a pattern derived from every other memory location. The eight MSB of the address of the location being tested are written into that location, the eight LSB are written into the following byte. The contents are then verified. This test detects row and column address shorts.

STAIRCASE
This uses a pattern derived from a counter initialized to 0H. 0H is written into the first location and the counter incremented. When the counter reaches FFH, it wraps back to 0H, and the count is continued until the write pass is complete. This test detects shorts between rows.

RIPPLE
All locations are cleared, verified, then filled one at a time with FFH and verified again. With FFH in all addresses, 0H is written one at a time and verified. This test detects shorts between any two bytes.

SLOW TWO PASS
This is a repetition of the BYTE TWO PASS with the interval between writing and verification increased to 1 second to check for slow leakage problems between bit cells.

ROTATING BYTE
A location is written with 01H, verified, the value is shifted left and verified. This continues until the value is 08H. The test then moves to the next location. This tests for shorts between each bit in each byte.

Error Reporting

Error messages consist of the name of the test that detected the error, address of the error, data that was read and the data that should have been read. Appended to the error messsage is the Exclusive OR of the error. An example of an error message is:

BYTE TWO PASS ERROR AT 1000:768F DATA WAS 57 NOT 55 XOR=02

This is interpreted as an error at location 768F in the second bank. Converting 02 hex to binary gives 00000010 meaning that data bit 1 is in error.

Select diagnostic "RAMTEST" to start testing.

Are There Error Messages?

Yes – Replace the System Board.

No – Passing this test confirms RAM reliability.

CRT Ram Diagnostics

CRTRAM uses the same test patterns as RAMTEST to check the 20K of Video Ram located on the Display & I/O Board.

Select diagnostic "CRTRAM" to start testing.

Are There Error Messages?

Yes – Replace the Display & I/O Board.

No – Passing the test confirms CRTRAM reliability.

Serial Port Test

The Hyperion diagnostic program for the Serial I/O Port is used in conjunction with the loop back plug shown below.

Data is sent out the serial port which is fed back in by the loop back plug. The data fed back is compared with the data sent out. Also looped back are Data Terminal Ready with Receiver Ready, and Clear to Send with Request to Send.

Select diagnostic "SERIAL" to start testing. The screen will display:

Testing at 300 BAUD: (Hit 0,3,4, or 9)

0 will exit the program
3 will test at 300 BAUD
4 will test at 4800 BAUD
9 will tets at 9600 BAUD

In REV01 serial diagnostics the BAUD rates are selected by:

E will exit the program
1 will test at 19.2K BAUD
3 will test at 300 BAUD
4 will test at 4800 BAUD
9 will test at 9600 BAUD

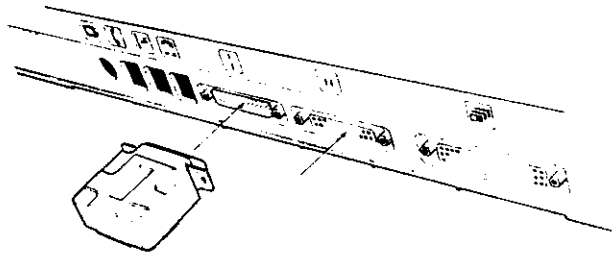


Fig. 3-12 – Serial Loop Back Plug

Did Serial Diagnostics Pass?

No – Replace the Display & I/O Board and re-run diagnostics.

Yes – Ensure that the printer the customer is using is GOOD. If the printer is GOOD, seek depot assistance.

Parallel Port Test

The Hyperion diagnostic program for the Parallel I/O Port is used in conjunction with the loop back plug shown below.

Select diagnostic "PARALLEL".

The screen will display: TEST D0-D7, PRESS G TO GO ON

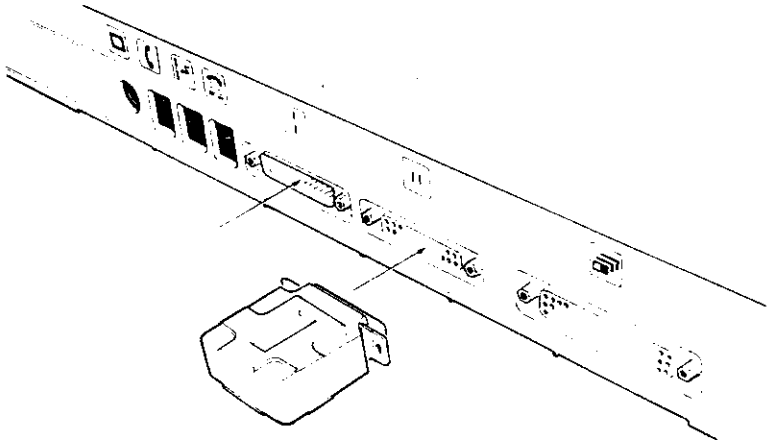


Fig. 3-13 – Parallel Port Loop Back Plug

An oscilloscope can be used to test the data lines, pins 2 to 9, on the parallel port. The test outputs a 50% signal.

If all data lines pass, the loop back plug can be installed on the port. By pressing "G" the status lines will be checked.

Did Parallel Diagnostics Pass?

No – Replace the Display & I/O Board and re-run diagnostics.

Yes – Ensure that the printer the customer is using is GOOD. If the printer is GOOD, seek depot assistance.

Speaker Test

You have entered this FAC because of sound problems. Select diagnostic "SPEAKER". The screen will display:

```
Hyperion System Card Timer Channel Speaker Test
(820033-000-01)

Press "N" = On, "F" = Off, "U" = Higher frequency "D" = Lower
frequency, "E" = Exit.
```

On the Diagnostic Diskette REV01, the 3 Speaker tests are combined, when the diagnostic is loaded the screen will display:

```
Please select one of the following tests

(1) SPKR  - System Card timer test
(2) MDMCHK  - Modem chip speaker test
(3) DTMFCHK  - DTMF generator chip speaker test


Your choice
```

Choose the number of the test to be run.

Caution DO NOT connect a signal generator to the Speaker wires to check the speaker function.

Does The Speaker Sound?

No – Check that the speaker wires are connected and that there are no shorts in the cable. Replace the Speaker and re-run diagnostics. If the test fails again replace the System Board.

Yes – There is no problem with the Speaker

Modem Test

This FAC is entered as part of a preventative maintenance procedure or because of problems using the Modem or Auto Dial/Answer feature. The Modem can be tested using the In:Touch program on the MS-DOS diskette.

Dialer Test

1) Connect the Hyperion as shown below. If possible connect a known GOOD Hyperion to another extension.

2) Insert the MS-DOS diskette and boot the system. When DOS has loaded, press soft key F6 (PHONE). Refer to the Hyperion User Guide to configure the Hyperion to match your telephone system. The cursor will be to the right of

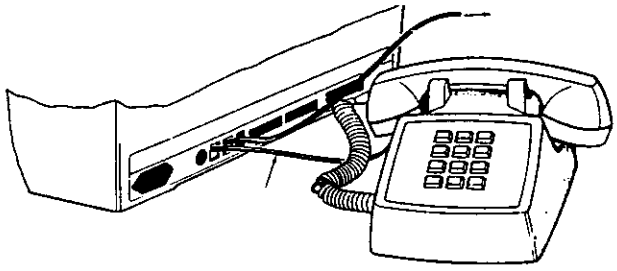


Fig. 3-14 – Modem Diagnostics

the Current #, you can enter a 7 digit local number or the number of the extension where the other Hyperion is connected. Press F5 (SPKR) soft key and the system will dial the number.

Does The Dialer Work?

No – 1) Check Speaker for correct operation.
2) Replace the Modem Board.
3) Replace the Display & I/O Board.

Yes – Continue to next page.

Dial the extension number the Hyperion under test is connected to using a known GOOD Hyperion or another phone.

The speaker can be checked for correct operation by running the test "MODEM".

The Tone Generator can be checked for correct operation by running the test "DTMF".

Did The Speaker Sound?

No – 1) Check Speaker for correct operation.
2) Replace the Modem Board.

Yes – Passing all tests in this section confirms correct Modem operation.

4.0 Removal/Replacement

4.1 General

This section details the removal and replacement of the major components of the Hyperion system. Before undertaking any removal or replacement procedures always ensure that you are aware of the safety precautions.

Note

Always

1) Disconnect all power sources and peripherals from the system before undertaking any removal or replacement procedures.

2) Work in a well lit area.

3) Use an anti-static work station.

4) Protect the system, especially the CRT face.

5) Use the proper tools.

6) Follow all safety instructions and hazard warnings found in this text or in the machine.

7) Remove all cables by the connectors, not by pulling on the cable itself.

Multilayer Boards

A multilayered printed circuit board is a series of individual circuit layers bonded to produce a thin monolithic assembly with external and internal connections to each level of circuitry determined by the system wiring diagram.

At the point of proposed interconnections, holes are drilled which pass through pads on the conductors of the inner layers which are larger than the drilled holes. The drilling exposes a rim of copper around the entire circumference of the hole. Interconnection between the different layers is accomplished by plating through the holes, connecting circuitry on the individual layers with each other and to the surface of the boards.

Cracking of the plating in the hole can occur during soldering because the thermal expansion of the insulating boards is considerably greater than that of the metal. The cracking occurs because the board and the eyelet expand due to the heat of soldering, and as the solder cools, the contraction of the board exceeds that of the eyelet which sets up stress sufficient in some cases to fracture the solder joints.

4.2 Keyboard Removal and Replacement

1) Invert the Hyperion on a proteced work surface. Disconnect (or connect) the modular connector at the rear of the Keyboard storage area.

Caution Do not pull or twist the retractable cable.

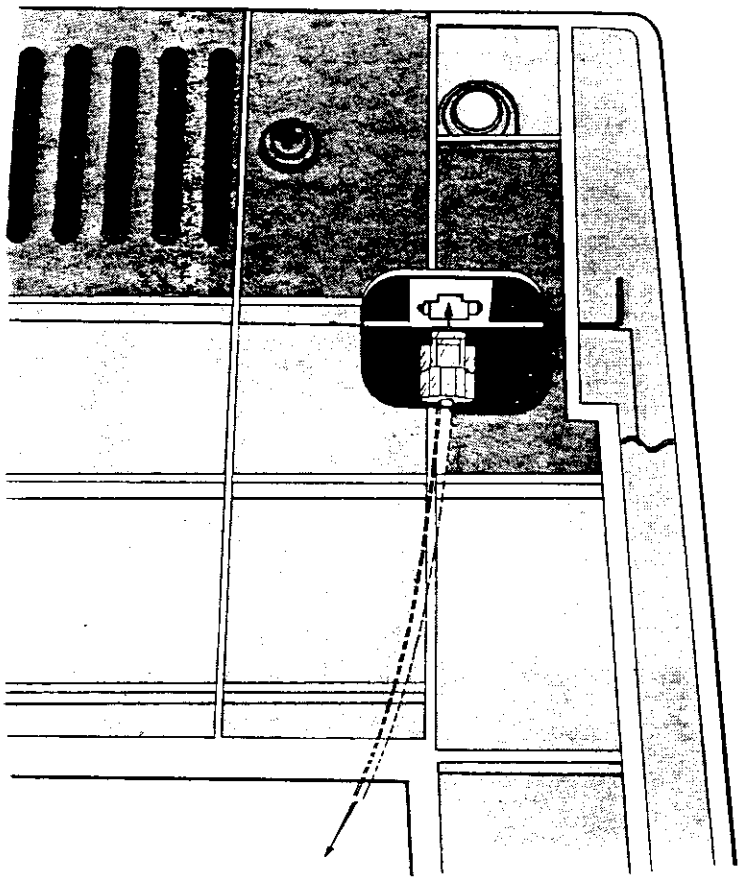


Fig. 4-1 – Keyboard Removal

4.3 Keyboard Cable or PCB

Removal

1) Disconnect the Keyboard.

2) Using a dental pick, remove the 6 spring clips securing the Keyboard top and bottom covers.

3) Seperate the covers and disconnect the cable from the Keyboard PCB.

4) Lift out the PCB if it is to be replaced.

Replacement

1) Connect the cable to the Keyboard PCB and assemble the top cover, Keyboard PCB and bottom cover.

2) Replace the 6 spring clips and secure them.

3) Reconnect the Keyboard to the system and check the operation.

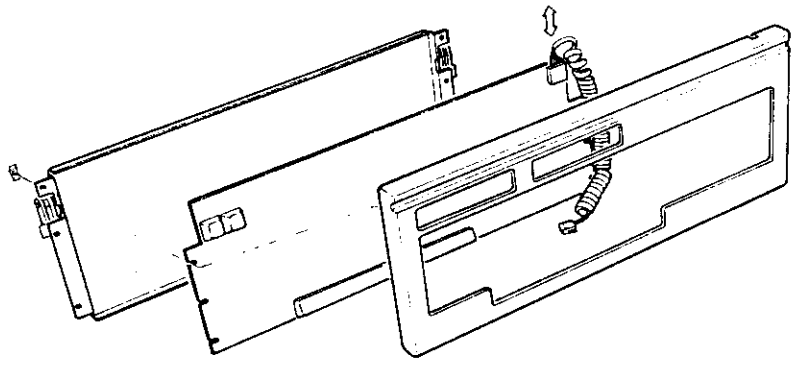


Fig. 4-2 – Keyboard PCB Removal

4.4 Housing

Removal

1) With the AC power, Peripherals and Keyboard disconnected, loosen/remove the two screws from the handle. On earlier housings the screws were not captive.

2) Remove the four screws from the base.

3) Lay the computer face down on a protected surface and slide the housing off the computer.

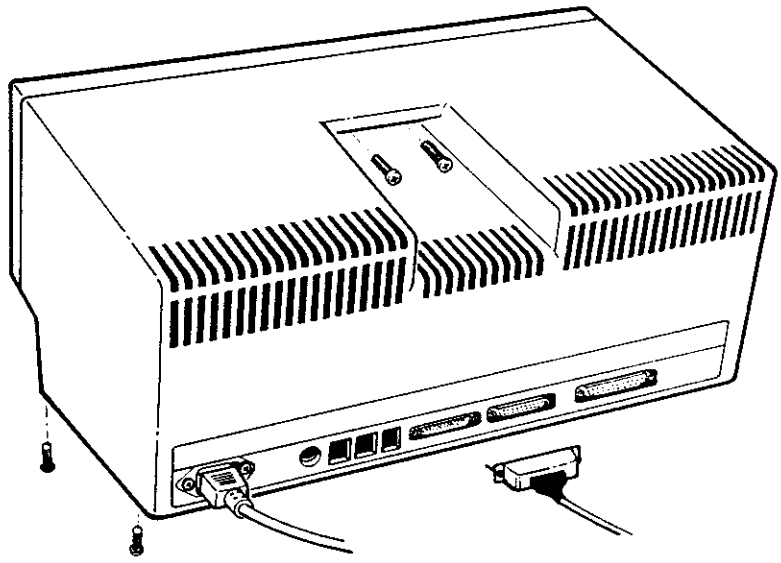


Fig. 4-3 – Housing Removal

Replacement

1) Lay the computer face down on a protected work surface. Carefully slide the Housing onto the chassis.

2) Replace the four screws in the base and tighten the two in the handle.

3) Reconnect the AC power, Peripherals and the Keyboard.

Note Following replacement of the Housing, the system should be tested for normal operation. Specific diagnostics may be prescribed in the following sections.

4.5 Front Bezel

Removal

1) With the main Housing removed, remove the Power Supply.

2) Remove the 6 screws that hold the bezel to the front of the chassis. The screws are located one at each corner and one in the center top and middle. On older machines the center screws are located top and bottom. Access to the screws is gained from the back of the bezel.

Replacement

1) Position the bezel and replace the 6 screws securing it to the front of the chassis, but do not tighten them.

2) Make sure that the Disk Drive doors open and close without binding. Adjust the Bezel as necessary and tighten the screws.

3) Replace the Power Supply, Housing, Keyboard and Peripherals.

4.6 Modem Board

Removal

1) With the Housing removed, remove the screws securing the Modem Board to the Display & I/O Board.

2) Carefully seperate the Modem Board from the Display and I/O Board connectors (top and bottom).

Replacement

1) Carefully align the plugs and sockets and mount the Modem Board on the Display & I/O Board.

2) Replace the screws securing the Modem Board to the Display & I/O Board.

3) Reconnect the Keyboard, Peripherals, and AC power.

4) Run the Modem diagnostics.

5) If sucessful, remove AC power, Peripherals and Keyboard.

6) Replace the Housing.

7) Replace the Keyboard, Peripherals and AC power.

8) Re-run the Modem diagnostics.

Warning The Modem is static sensitive and the board should not be removed and reinserted often.

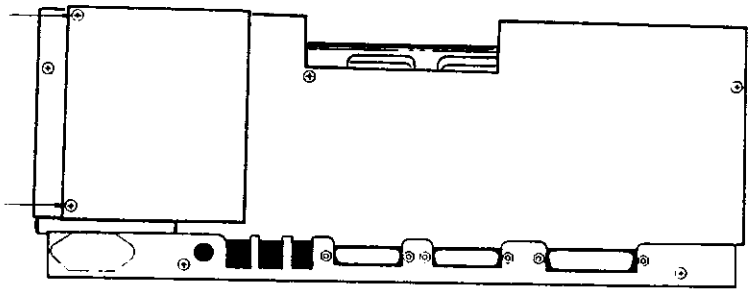


Fig. 4-4 – Modem Board Removal

4.7 System and Display & I/O Boards

Removal

Caution When the System and Display & I/O Boards are removed from the chassis, the chassis becomes "front heavy". The chassis must be supported at all times to prevent its tipping forward when the boards are removed.

1) With the Housing removed, disconnect the DC power cable and disk drive interface.

2) Remove the 3 Phillips head screws along the top and the 2 screws at the bottom.

3) Remove the 6 hexagon head nuts from the I/O connectors along the bottom edge of the Display & I/O Board. On the newer chassis these 6 nuts are part of the board assembly and do not have to be disconnected to remove the board assembly.

4) Lift out the board assembly and disconnect the video, fan and speaker cables.

5) Remove the two hexagon head nuts from the bottom corners of the Display & I/O Board.

6) Carefully seperate the boards at the connectors.

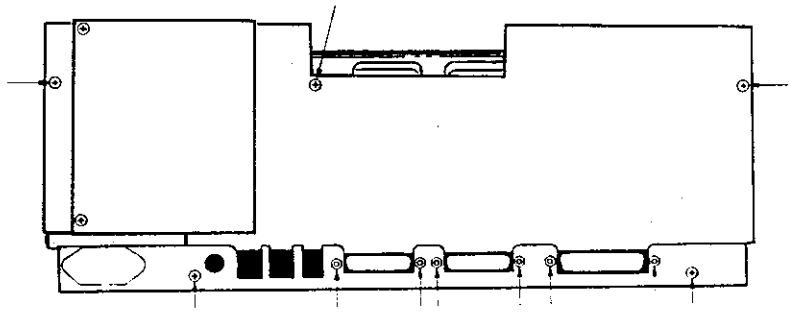


Fig. 4-5 – Board Assembly Removal

Replacement

Note If the System Board is to be changed, and the unit is configured as a single drive Hyperion, a jumper at position E3-1&2 must be installed, this jumper must be removed for a two drive Hyperion.

If the Display & I/O Board is to be replaced, remove the I/O connector chassis frame from the defective board and install on the replacement board.

1) Carefully align and seat the connectors of the Display & I/O and the System Boards.

2) Replace the two hexagon head nuts and spacers in the bottom of the Board assembly.

3) Position the boards in the computer and connect the speaker, video and fan cables. Route the video cable under the board assembly in the cut-out provided.

4) Replace the 6 hexagon head nuts beside the I/O connectors at the bottom of the boards if the chassis is the older version.

5) Replace the remaining spacers and screws securing the Boards.

6) Replace the DC power cable and disk drive interface.

7) Reconnect the Keyboard, Peripherals and AC power.

8) Run applicable diagnostics.

9) If sucessful, remove AC power, Peripherals and Keyboard.

10) Replace the Housing.

11) Replace the Keyboard, Peripherals, and AC power.

12) Re-run the diagnostics.

4.8 Disk Drive

Removal

Note To remove Drive "B", first remove Drive"A"

1) With the Housing removed, remove the Power Supply.

2) Remove the Front Bezel.

3) Remove the screen from the top of the Disk Drives. On newer chassis this screen cannot be removed.

4) If the screen cannot be removed, the Board assembly will have to be removed to gain access to the back of the drives permitting easy removal of the cables. DO NOT remove the cables by pulling on the wires.

5) Remove the screws from the left hand side of Drive "A".

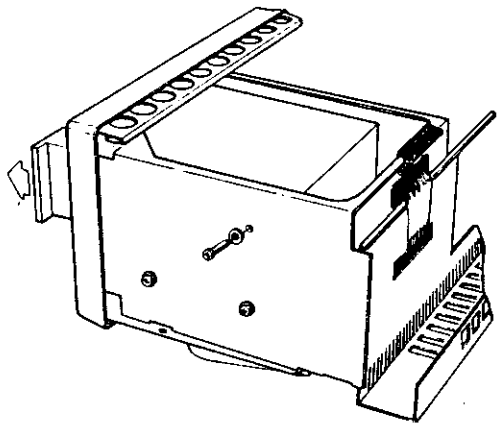


Fig. 4-6 – Disk Drive Removal

6) Remove the screws on the right hand side of Drive "A" and slide it partially out of the chassis.

7) Disconnect the ribbon cable and power harness when accessible and slide the Drive out of the chassis.

8) To remove Drive "B", repeat steps 5,6, and 7 for Drive "B".

Replacement

Note Drive "B" must be replaced before Drive "A". Drive select jumpers must be correctly positioned before drive replacement as follows.
Drive "A" = DS0
Drive "B" = DS1

The Drives are shipped with a cardboard diskette inserted. This should only be removed after the Drive is installed in the system but before turning on the computer.

If the Hyperion is configured as a single drive system, a jumper will have to be installed on the System Board at location E3-1&2. For a two drive system this jumper must be removed.

1) Slide the Drives partially into the chassis and connect the power harness and ribbon cables and slide fully home.

2) Replace the screws in the side of the Drives but do not tighten them.

3) Replace the Front Bezel and align the Drives to the slots in the bezel. Ensure that the Drive doors open easily and a diskette can be inserted and removed smoothly, then tighten the screws.

4) Replace the Power Supply and Board assembly.

5) Reconnect the Keyboard, Peripherals and restore the AC power.

6) Run Disk Diagnostic.

7) If sucessful, remove AC power, Peripherals and Keyboard.

8) Replace the screen on top of the Disk Drives, then the Housing.

9) Reconnect the Keyboard, Peripherals and AC power.

10) Re-run the diagnostics.

4.9 Power Supply

Removal

1) With the Housing removed, carefully pry the DC wire harness from the plug (J2).

2) Remove the two nuts at the base of the Power Supply frame.

3) Carefully lift the Power Supply out of the chassis and disconnect the AC input plug (J1) when it becomes accessible.

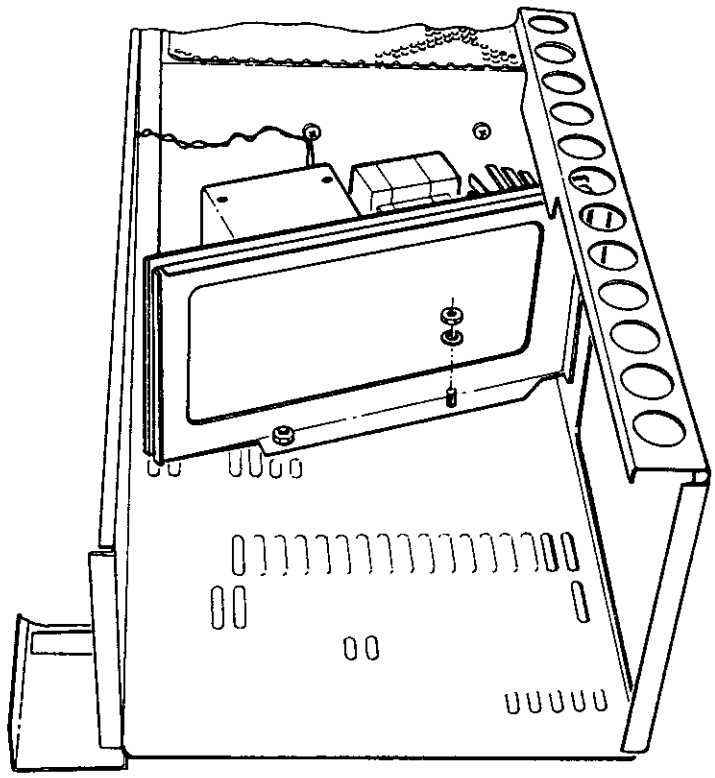


Fig 4-7 – Power Supply Removal

Replacement

1) Ensure that the jumper on J3 is set properly for the AC power in use.

2) Connect the AC power harness (J1) and position the Power Supply in the chassis.

3) Replace the two nuts at the base of the Power Supply.

4) Replace the DC power harness plug (J2).

5) Reconnect the Keyboard, Peripherals and restore AC power.

6) Test the system.

7) Remove the AC power, Peripherals and Keyboard.

8) Replace the Housing.

9) Reconnect the Keyboard, Peripherals and AC power and test the system.

4.10 CRT Assembly

Warning Before attempting any work on the CRT assembly, short the anode to the chassis as shown.

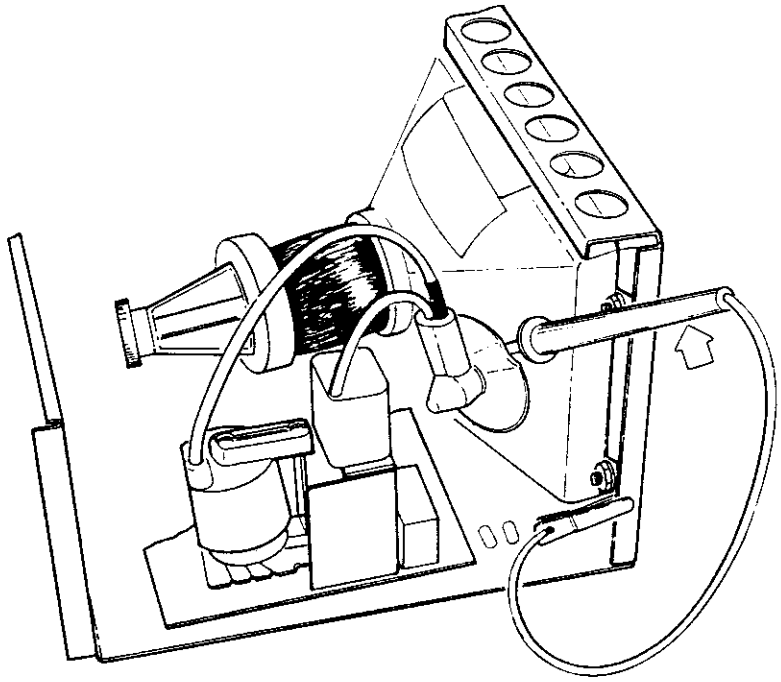


Fig. 4-8 – Discharging CRT Anode

Warning The CRT is very fragile, especially at the neck, and requires careful handling to prevent breakage. The implosion resulting from careless handling can cause serious injury. Always place a soft cloth on the work surface to prevent scratching of the tube face.

Removal

1) With the Housing removed, remove the System and Display & I/O Boards and the Power Supply.

2) Observing the saftey precautions, disconnect the CRT Board interface.

3) Remove the four screws from the CRT Board.

4) Remove the four nuts securing the CRT to the chassis and carefully lift out the tube and board assembly.

Replacement

1) Carefully replace the CRT assembly in the chassis. Ensure that the springs are between the CRT flange and the chassis. Also make sure that the long spring is positioned under the tube and connects over the top of the bottom flanges.

2) Replace and tighten the nuts around the flange.

3) Connect the CRT Board interface.

4) Replace the screws in the CRT Board.

5) Replace the Power Supply, System and Display & I/O Boards.

6) Reconnect the Keyboard, Peripherals and AC power.

7) Run diagnostics and adjust the CRT as required, (refer to Chapter 8 for alignment procedures).

8) Replace the Housing.

9) Reconnect the Keyboard, Peripherals, and restore AC power.

10) Re-run the diagnostics.

4.11 Speaker

Removal

1) With the Housing removed, unsolder the Speaker leads at the speaker.

2) Remove the screws/nut securing the Speaker to the chassis and remove the Speaker.

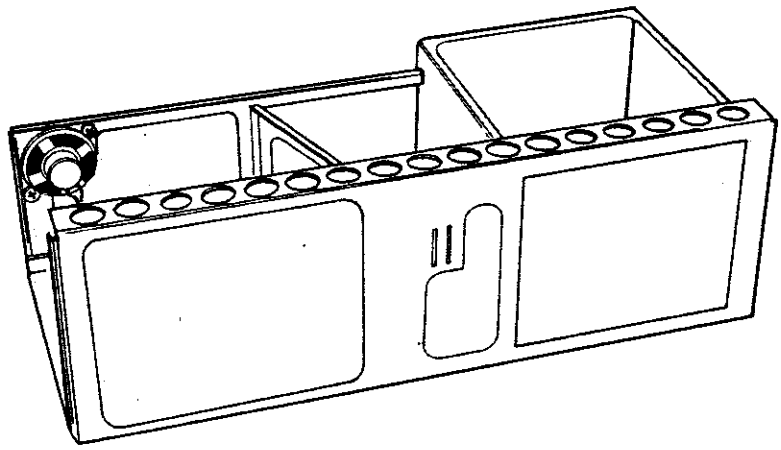


Fig. 4-9 – Speaker Removal

Replacement

1) Position and secure the speaker to the chassis.

2) Resolder the Speaker leads.

3) Reconnect the Keyboard, Peripherals, and restore AC power.

4) Run the Speaker diagnostics.

5) If sucessful, remove AC power, Keyboard, and Peripherals.

6) Replace the Housing.

7) Reconnect the Keyboard, Peripherals and restore AC power.

8) Re-run the diagnostics.

4.12 Fan

Removal

1) With the Housing removed, remove the Power Supply.

2) Disconnect the Fan power plug.

3) Remove the nuts securing the Fan to the chassis and lift out the Fan.

Replacement

1) Position the Fan in the chassis.

2) Replace the nuts securing the Fan to the chassis.

3) Reconnect the Fan power plug.

4) Replace the Power Supply.

5) Restore AC power and ensure that the Fan runs.

6) Remove AC power.

7) Replace the Housing.

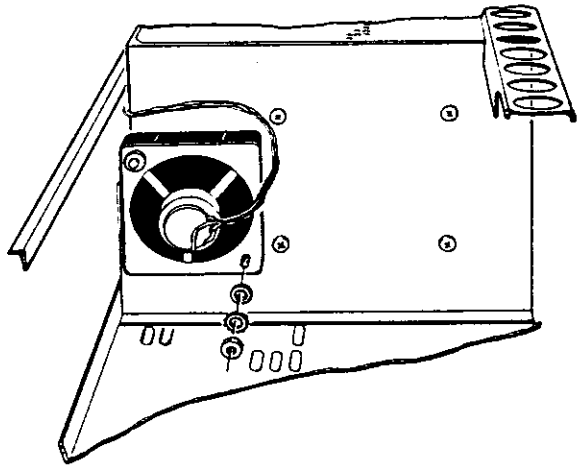
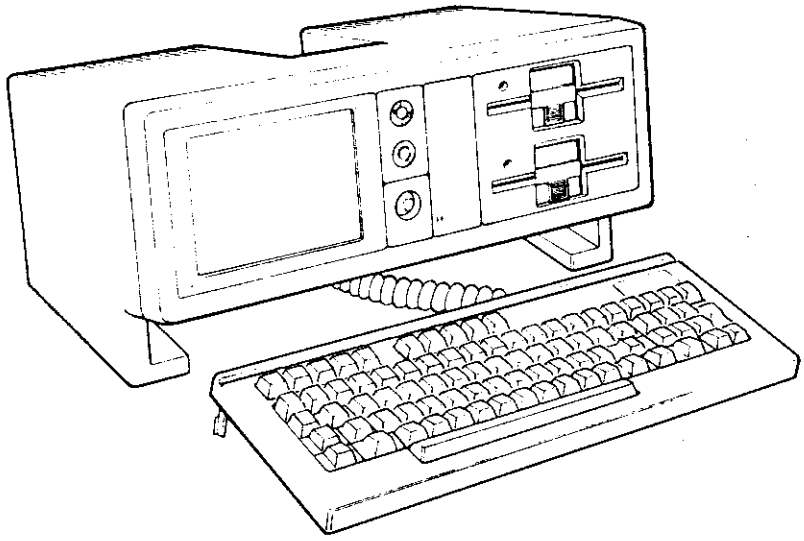


Fig. 4-10 – Fan Removal

5.0 Parts List

5.1 How to Use This Parts List



1) Locate the assembly containing the part.

2) Turn to the section for that assembly and visually identify the part.

3) Refer to the accompanying list to find the description, quantity and Hyperion part number.

5.2 Hyperion Assembly (External)

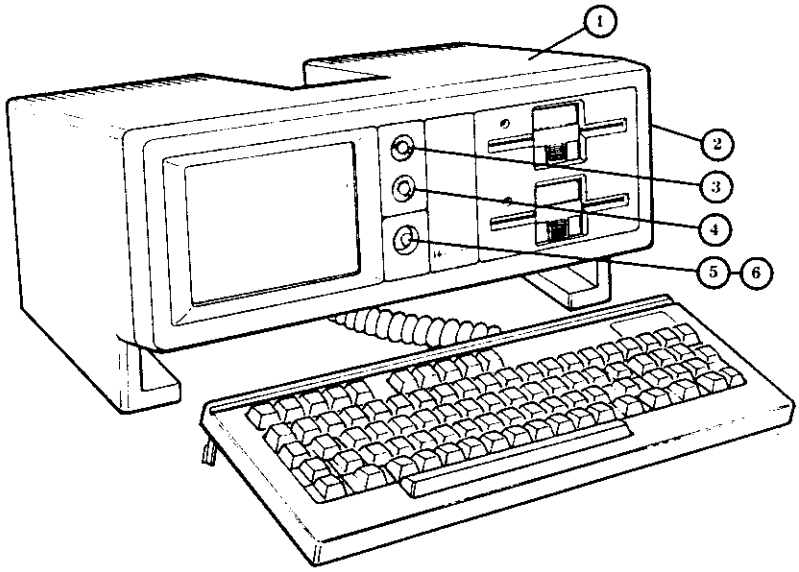


Fig. 5-1 – Hyperion Assembly External

Figure Index Number	Part Number	Description
1	200000-000	HOUSING, MAIN
2	200006-000	BEZEL, FRONT
3	200008-000	KNOB, BRIGHTNESS
4	200007-000	KNOB, CONTRAST
5	900846-000	SWITCH PB LIGHTED
6	900849-000	LAMP BI-PIN T1

5.3 Hyperion Assembly (Internal)

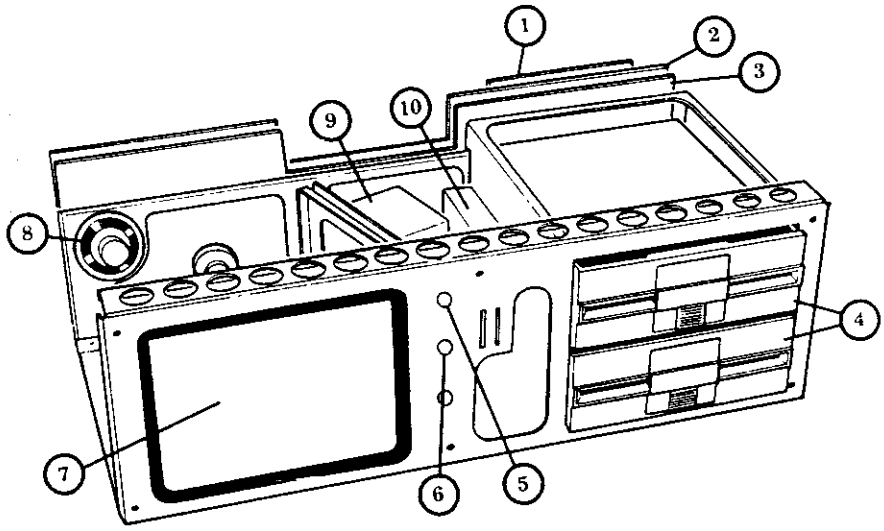


Fig. 5-2 – Hyperion Assembly Internal

Figure Index Number	Part Number	Description
1	100012-000	PCB, MODEM BOARD A8
2	100005-000	PCB, DISPLAY AND I/O BOARD A7
3	100004-000	PCB, SYSTEM BOARD A6
4	520003-001	DISK DRIVE, FLOPPY, QTY 2
5	520007-000	POT SINGLE TURN, LOGARITHMIC
6	520008-000	POT SINGLE TURN LINEAR
7	520000-001	CRT ASSY, COMPLETE
8	900789-000	SPEAKER, MINI, 480-5000HZ 0.3W
9	520002-001	POWER SUPPLY
10	900809-000	FAN 12V 200mA 2.4W

5.4 Keyboard Assembly

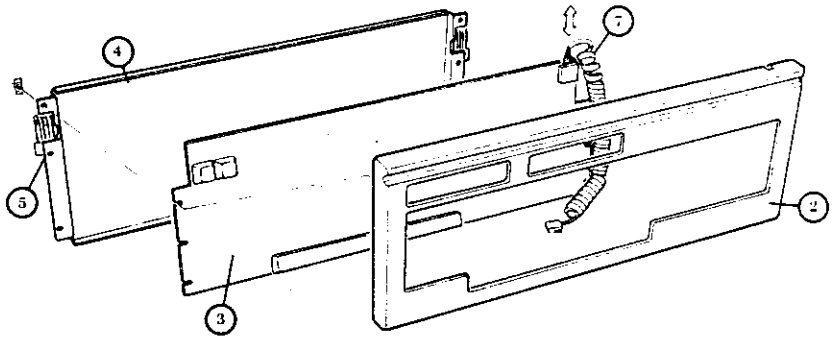


Fig 5-3 – Keyboard Assembly

Figure Index Number	Part Number	Description
1	100003-000	KEYBOARD ASSEMBLY
2	200009-000	ENCLOSURE, KEYBOARD
3	520001-001	KEYBOARD
4	200010-000	BASE, KEYBOARD
5	200011-000	FOOT, KEYBOARD L.H.S.
	200011-001	FOOT, KEYBOARD R.H.S.
6	200012-000	SPRING, FOOT L.H.S.
	200012-001	SPRING, FOOT R.H.S.
7	520009-000	CABLE ASSEMBLY, KEYBOARD

6.0 Preventative Maintenance

The purpose of preventative maintenance is to locate and correct potential problems before they occur and to ensure reliable system operation.

Preventative maintenance should be performed on a regular basis and, depending on use, should be at 6 month to 1 year intervals.

1) Check for visible damage. Pay particular attention to the Keyboard for damaged keys.

2) Clean inside the Keyboard.

3) Remove the Housing of the computer and check that the board and cable connections are secure. Check that socketed components are properly seated.

4) Check voltage levels at the Boards, Drives and CRT and that the Fan is operational.

5) Load and run all diagnostics. Replace or repair components as required.

6) Re-assemble the machine, clean the Housing and CRT face.

7) Re-test the system.

7.0 Packing and Shipping

General

Packaging for shipping should confirm as nearly as possible to the origional packaging when items are received from the depot or factory. Devices which are static sensitive must be wrapped directly in conductive wrapping before being placed in shipping cartons.

Printed circuit boards should be protected against component and pin connector damage before being placed in the conductive wrapping.

Large and fragile parts require special care in packaging. Add support and extra packing material to prevent crushing or shifting in transit.

Boxes and cartons must be labeled to indicate the fragility of their contents.

CRT

Note Observe safety precautions

1) The CRTs are shipped in their own box and are securely fastened to a cardboard tray. CRTs must always be stored and shipped securly fastened to these trays to prevent damage.

2) Before closing the cover of the box make sure that the box is full of packing to prevent the CRT from moving.

Drives

1) Drives are shipped in special foam boxes and are also shipped with a cardboard diskette inserted to prevent the heads from touching or banging during shipping. Always ship Drives in the foam boxes and with the cardboard diskette inserted.

8.0 Adjustments

Disk Drives

CRT

8.1 Tools and Test Equipment

The Drives have been manufactured and assembled with precision and to tight tolerances. As a result, field service or repair of the drives is not recommended unless the user has the following tools, test and calibration equipment.

1) 5-1/4 inch Floppy Disk Drive Exerciser.

2) Dual Trace Oscilloscope, Tektronix 465 or equivalent with matched 10:1 probes.

3) Digital Voltmeter.

4) Taptite Driver #4, Torx Part Number TX-09.

5) Taptite Driver #6, Torx Part Number TX-15.

6) Torque Wrench.

7) Alignment Diskette, (DYSAN part number 800180).

Note The Track positions specified in this procedure are for Dysan alignment diskettes. Other manufacturers may use different tracks.

8.2 Alignment and Adjustments

Equipment Set-up

Note Any alignment should be performed in an environment of 50% humidity and at a temperature of 70 F +/− 5. The media being used to align drives must be in this environment for at least 24hrs prior to alignment.

Configure the Drive Exerciser for:

5 inch Drive.
40 Tracks.
Double density.
2 Heads.
Single Sector.

Set-up the oscilloscope for:

Channel 1	AC
Channel 2	AC Inverted
Vert. Mode	+ ADD
Sec/div	20 msec
Trigger	Normal/external
Volts/div	0.1 (using 10x probes).

Oscilloscope connection test points (Ref Fig. 8-1)

Channel 1	TP5 (L2) on Control Board
Channel 2	TP6 (L3) on Control Board
Grounds	+ve side of C26
Trigger	TP3 (R38) on Control Board
Ground	−ve side of C12

Sequence of alignments and adjustments:

Motor Speed Adjustment
Track 00
Index Alignment
Radial Alignment
Read/Write Current
Write Current Adjustment

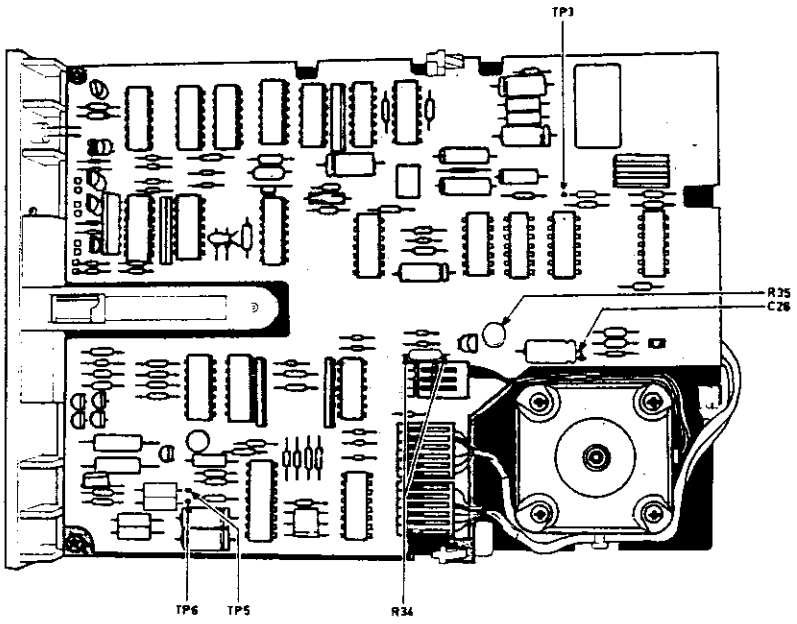


Fig. 8-1 – Disk Drive Test Points

Motor Speed Adjustment

1) Connect the power and control cables from the exerciser to the drive.

2) Connect the motor PCB ground to the lug on the chassis.

3) Change Channel 1 and 2 to 0.1 Volts/Div.

4) Insert alignment diskette.

5) Return the Head to Track 0, then step to Track 1.

6) Observe that the index pulse is 200 msec +/− 2 msec. The dark lines on the Drive Motor spindle should appear motionless if viewed with an ultraviolet light.

7) Adjust R30 on the Motor Control Board if necessary and secure with locktite.

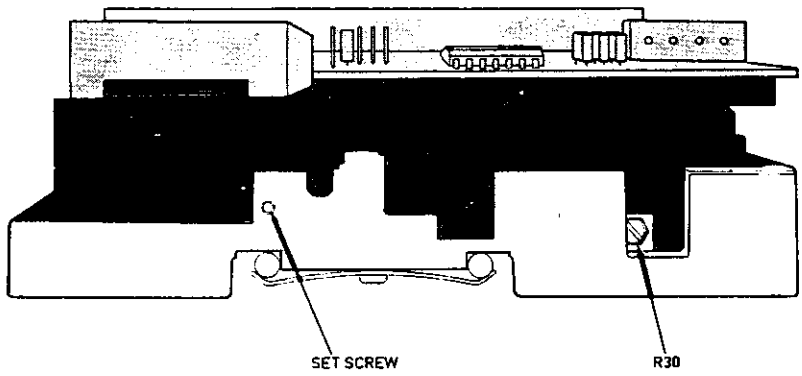


Fig. 8-2 – Motor Speed Adjustment Resistor

Track 00 Adjustment

Connect the oscilloscope to:

Channel 1	A8, Pin14
External Trigger	B11, Pin12

Set the oscilloscope for:

Vert. Mode	Ch1/Alt
Time/Div	1 msec
Volts/Div	2 Volts
Trigger	Normal, External/AC

Set the exerciser for:

Step Rate	3 msec

Auto seek between Tracks 0 and 3

1) Start the Drive and exerciser.

2) The signal should be as shown below. If not perform the following adjustment.

3) Loosen the Track 00 screw accessible thru the small hole near J-1.

4) Adjust the Track 00 sensor for a signal of 5.25 +/− 0.25 msec.

5) Check the Radial Alignment.

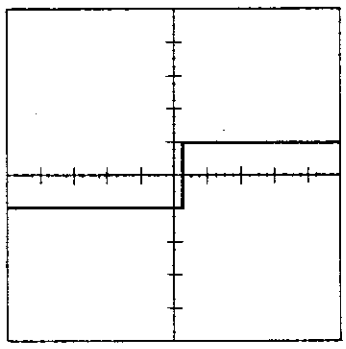


Fig. 8-3 – Track 00 Waveform

Index Alignment

Change the oscilloscope to:

Vert. Mode	Both/Add
Time/div	50usec
Volts/div	0.1 volt
Channel 1&2	Inverted
Positive Slope Trigger	

1) Insert alignment diskette.

2) Step to Track 1.

3) The display on the oscilloscope should be 200usec +/- 50usec.

4) If the display is not as above, loosen the Load Arm screws, move the Load Arm all the way towards the Bezel, (be careful not to pinch the write protect or index wires), slowly move the Load Arm towards the rear of the Drive, when the leading edge of the pulse is at 200usec, tighten the screws to 6 inch-lbs.

5) Check the signal on Head 1. If the Heads are not aligned with each other, the signal may not be on 200usec. If this is the case, adjust the Load Arm so that the signal is off on each Head by the same amount.

6) Step to Track 34.

7) Check the Index on both Heads and adjust if necessary. If the Load Arm is adjusted, repeat the check at Track 1.

8) Check the Head Azimuth. Set the Time/div to 1 msec. The tolerance is +/- 18 minutes of angle. If the Azimuth is out of tolerance, replace the Head.

9) Return to Track 0.

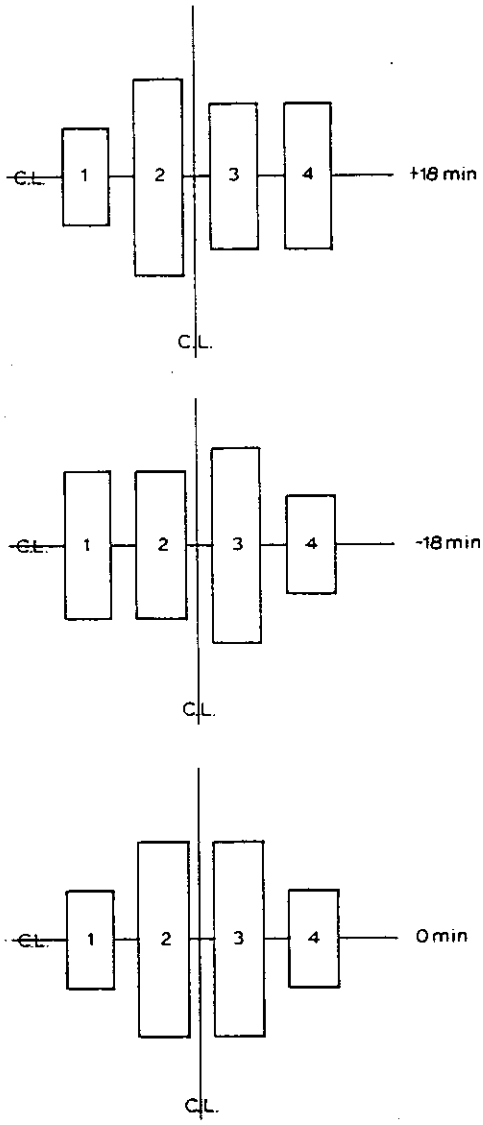


Fig. 8-4 – Head Azimuth Waveforms

Radial Alignment

1) Insert alignment diskette.

2) Step to Track 0 then out to Track 16.

3) The display on the screen should be similar to that shown below.

4) Turn the Volts/div to 20mv and adjust the lobs for equal amplitude. To adjust, loosen the two Stepper Motor alignment screws 1/4 turn and move the alignment set screw forward or reverse to obtain the correct cat-eye position. Tighten the alignment plate screws and ensure that the position did not change.

5) Return the Head to Track 0, then out to Track 16 and check that the cat-eye is within 15% of each other.

6) Step from Track 16 to Track 39 and return to Track 16, the cat-eye should be within 15% of each other.

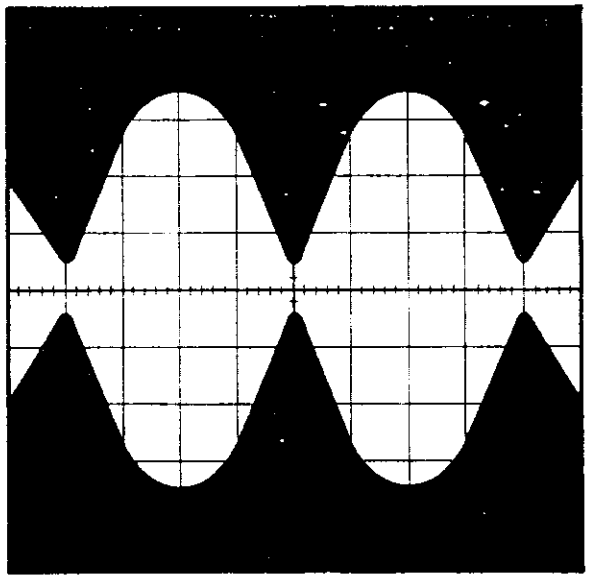


Fig. 8-5 – Radial Alignment Waveform

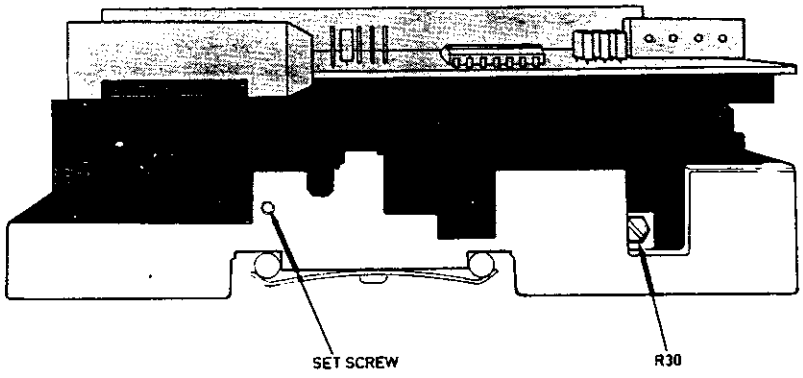


Fig 8-6 – Radial Alignment Adjusting Set Screw

Read/Write Amplitude

1) Insert a scratch diskette and return to Track 0.

2) Perform an erase.

3) Write data and check the signal on the oscilloscope is 550mv +/− 50mv.

4) Step to Track 39.

5) Perform an erase.

6) Write data and check the signal on the oscilloscope is 230mv +/− 50mv.

7) Perform the Write Current Adjustment if necessary.

Write Current Adjustment

1) Return to Track 0.

2) Install a scratch diskette halfway into the drive.

3) Connect the Volt Meter leads across R34.

4) The reading should be 400mv +/− 3mv, if this is not correct, adjust potentiometer R35 and secure with locktite.

8.3 Troubleshooting Guide

A. Track 0 not adjustable:

Track 0 switch defective
Logic Board defective

B. Motor Speed not adjustable:

Loose connector at J3
Defective Motor Control Board
Loose connector at Drive Motor
Defective Index LED or Detector
Defective Logic Board
Clutch not engaged properly

C. Cat-eye not adjustable or fails position test:

Loose set screw on pulley
Eject mechanism defective
Damaged Heads
Damaged Guide Rails
Load Arm not adjusted properly
Head riding on Load Arm
Head wire too tight at Stepper Motor

D. Index not adjustable:

Damaged Heads
Eject mechanism bad
Connector not seated or making poor contact
Defective Logic Board

E. Write current not adjustable:

Defective Logic Board

8.4 CRT Alignments and Adjustments

The CRT can be adjusted while it is in the Hyperion, however, care must be taken to protect against electrical shock, (remove watches and rings). The only tools required for adjusting the CRT are a non-metal tuning wand, diagnostic diskette and the CRT overlay. DO NOT USE A METAL SCREWDRIVER. For best results allow the CRT to warm up for one minute before adjusting.

Note Before making any adjustments, check that the yoke is tight against the CRT.

Always lock the pots with locktite or equivalent when the adjustments are completed. If an excess amount of locktite is used it may run down inside the pot causing it to seize.

There are two alignment procedures to use, one requires BASICA which will only run on systems with boards having serial numbers 501 and up. The other procedure will run on all machines with boards having serial numbers up to 2500.

The following adjustments can be performed:

1) Brightness (R94)
2) Vertical Size (R27, for both 70 ands 60 Hz).
3) Vertical SizeA (R46, for 60 Hz only).
4) Vertical Linearity (R49).
5) Horizontal Size (L52).
6) Horizontal Linearity (L51).
7) Raster Centering (Ring magnets).
8) Horizontal Centering (R53).
9) Dynamic Focus (R110).
10) Focus (R95).
11) Geometrical Distortion (Yoke magnets).

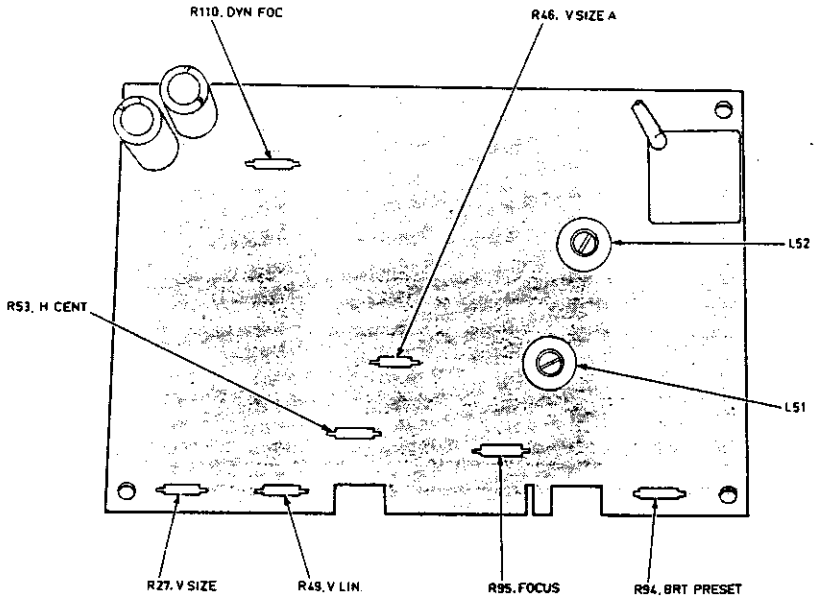


Fig 8-7 – CRT Board Adjustment Locations

Procedure to Align the CRT Without BASICA

Brightness

1) Load diagnostic diskette, enter BRIGHTNESS and Rtn.

2) Turn Brightness Preset (R94) to minimum.

3) Turn the Brightness Control on the Hyperion to the maximum position.

4) Increase Brightness Preset until the raster is visible.

5) Re-adjust the Hyperion brightness control for comfortable viewing.

Note If the brightness level is set too high, the screen phosphor may burn.

Raster Size

1) Enter SQUARE70 and Rtn. The square should measure 4.8 x 3.75 +/− 0.12 inches. Place the CRT overlay on the screen and adjust Vertical Size (R27) and Horizontal Size (L52) until the Square fits within the two squares of the overlay. The two ring magnets may have to be adjusted, moving the raster within the overlay.

2) Enter SQUARE60 and Rtn. The square should be the same size. If the dimensions are not the same, adjust Vertical SizeA (R46) and Horizontal Size (L52).

3) Repeat Step 1 and adjust as required.

Linearity

1) Enter LINEARITY and Rtn. If the characters are larger/-smaller at the top than the bottom, adjust Vertical Linearity (R49). If the characters are wider or overlapping on either side, adjust Horizontal Linearity (L51).

2) Check Raster Size and adjust as necessary.

3) Enter BRIGHTNESS and Rtn. Check that the top and bottom bands are the same size, adjust Vertical Linearity (R49) as required.

Centering

1) Enter BRIGHTNESS and Rtn.

2) Using the two ring magnets on the neck of the tube, center the raster on the screen.

3) Center the video on the screen horizontally with Horizontal Centering (R53).

Focus

1) Turn Brightness to maximum.

2) Adjust the Focus control (R95) for best centre and corner focus.

3) Return to normal brightness.

Dynamic Focus

1) Adjust the Dynamic Focus (R110) on the collector of Q110 to 80 +/− 10 volts peak to peak.

Geometrical Distortion

1) Remove the magnets from the posts on the yoke and clean off excess silicon.

2) Enter SQUARE60 and Rtn.

3) The magnets on the top three posts are used to push the display down, while the bottom four posts push the display up. Rotating the magnets allow for fine adjustment.

4) When the adjustments are complete, apply silicon to hold the magnets to the posts.

5) Check Raster size and adjust as necessary.

Procedure to Align CRT Using BASICA

1) Load diagnostic diskette and type BASICA and Rtn.

2) The screen will display the version of Basic followed by "OK".

3) Type RUN"CRTTST and Rtn. The program will load and a menu of 6 test patterns will be displayed. The first two are used for CRT alignment. They are accessed by the "Cursor Right" key, using the "Cursor Left" key allows the program to go back to the previous display.

4) The 60 Hz CRT Test Pattern is used for adjusting:

   Brightness: Brightness Preset (R94).
   Raster Size: Vertical SizeA (R46) and Horizontal Size (L52). The CRT overlay is used in the same manner as with the other procedure.
   Linearity: Vertical Linearity (R49) and Horizontal Linearity (L51).
   Centering: Ring magnets
   Focus: (R95).
   Geometrical Distortion: Yoke magnets.

5) The 70 Hz CRT Tets Pattern is used for adjusting:

   Raster Size: Vertical Size (R27) and Horizontal Size (L52) and to check the adjustments made with the 60 Hz pattern.

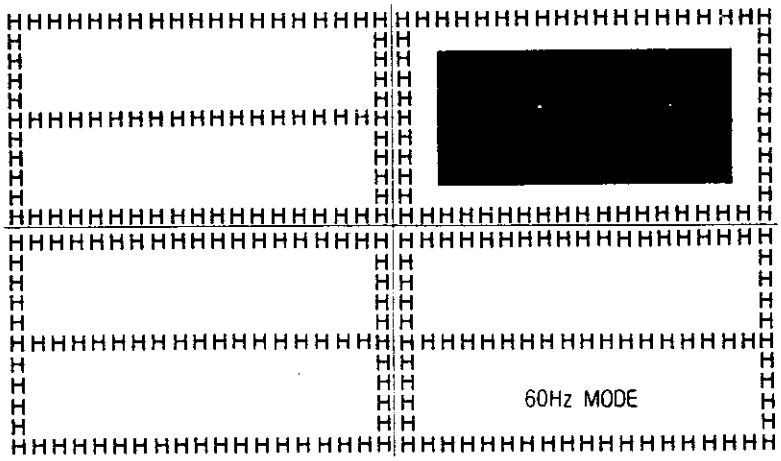


Fig. 8-8 – 60 HZ CRT Test Pattern

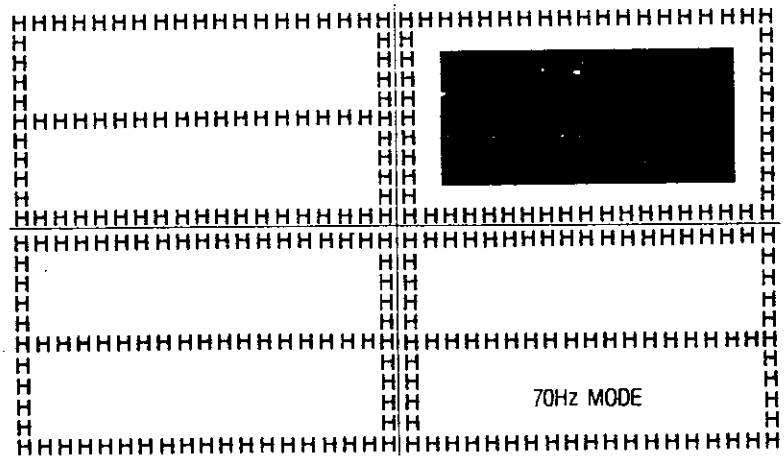


Fig. 8-9 – 70 HZ CRT Test Pattern

9.0 Specifications

Electrical

- 120/240 volts AC +12%, −25%, 45 to 65 Hz operation selectable via internal jumper.
  Power consumption 90 watts maximum.

Mechanical

- Size 18.3 inches (46.4 cm) wide, 11.3 inches (28.8 cm) deep, 8.8 inches (22.3 cm) high.
  Weight 21 lbs (9.6 kg).

Environmental

- Humidity Operating 20% to 80%
  Storage 5% to 98% (no condensation)
- Temperature Operating 10 to 50 deg. C (40 to 122 deg. F).
  Storage −34 to 65 deg. C (−30 to 149 deg. F).
  Max Wet Bulb 29 deg. C (85 deg. F).
- Altitude Operating 10,000 feet.
  Non-operating 40,000 feet.

HYPERION

MAINTENANCE MANUAL

Part Number: 650003-000
BYTEC-COMTERM INC.

Contents

List of Illustrations

Schematic Diagrams

1.0 Introduction

The Hyperion portable computer is a powerful 16-bit microcomputer with full graphics and optional built-in telecommunications capability. Most of the advanced circuitry is contained on two multi-layer printed circuit boards.

This manual is intended to provide detailed information to assist in repairing the Hyperion sub-assemblies to the chip level. Refer to the Maintenance Manual (Part Number 100031-000-01) for detailed diagnostic and removal/replacement procedures.

Throughout this manual various types of precautionary information is included:

Warning A WARNING indicates that procedures detailed could cause personal injury or serious equipment damage if suitable precautions are not taken.

Caution A CAUTION indicates that minor damage may result if suitable precautions or normal work practices are not followed.

Note A NOTE indicates steps to be taken to make the particular procedure easier to carry out.

Before undertaking any removal or replacement procedures always ensure that you are aware of the safety precautions.

Note

Always

1) Disconnect all power sources and peripherals from the system before undertaking any removal or replacement procedures.
2) Work in a well lit area.
3) Use an anti-static work station.
4) Protect the system, especially the CRT face.
5) Use the proper tools.
6) Follow all safety instructions and hazard warnings found in this text or in the machine.

7) Remove all cables by the connectors, not by pulling on the cable itself.

8) The boards, especially the Modem, are static sensitive and must be handled with care.

Multilayer Boards

A multilayered printed circuit board is a series of individual circuit layers bonded to produce a thin monolithic assembly with external and internal connections to each level of circuitry determined by the system wiring diagram.

At the point of proposed interconnections, holes are drilled which pass through pads on the conductors of the inner layers which are larger than the drilled holes. The drilling exposes a rim of copper around the entire circumference of the hole. Interconnection between the different layers is accomplished by plating through the holes, connecting circuitry on the individual layers with each other and to the surface of the boards.

Caution Cracking of the plating in the hole can occur during soldering because the thermal expansion of the insulating boards is considerably greater than that of the metal. The cracking occurs because the board and the eyelet expand due to the heat of soldering, and as the solder cools, the contraction of the board exceeds that of the eyelet which sets up stress sufficient in some cases to fracture the solder joints.

Soldering Techniques for Multilayered Boards

Heat Requirements

The maximum temperature used for soldering on multilayered boards is 480F (248C), slightly higher temperatures may be necessary for chip removal. The solder tip used should be high mass with fast heat recovery time.

Warning The copper pads on the boards may be lifted up by excessive heat or pulling.

Chip Removal

1) Cut the chip legs as close to the chip as possible and remove the chip.

2) Remove each leg by heating individually and lifting from the hole.

3) Use a vacuum type solder sucker to remove the solder from the holes. DO NOT USE SOLDER WICK as this requires high heat input.

Chip Replacement

1) Correctly orient and insert the chip.

2) Start soldering the pins at the center of the chip and work towards the ends.

3) Touch the solder to the leg, bring the solder iron into contact with the solder. When the solder has melted and flowed around the joint, remove the solder iron then the solder.

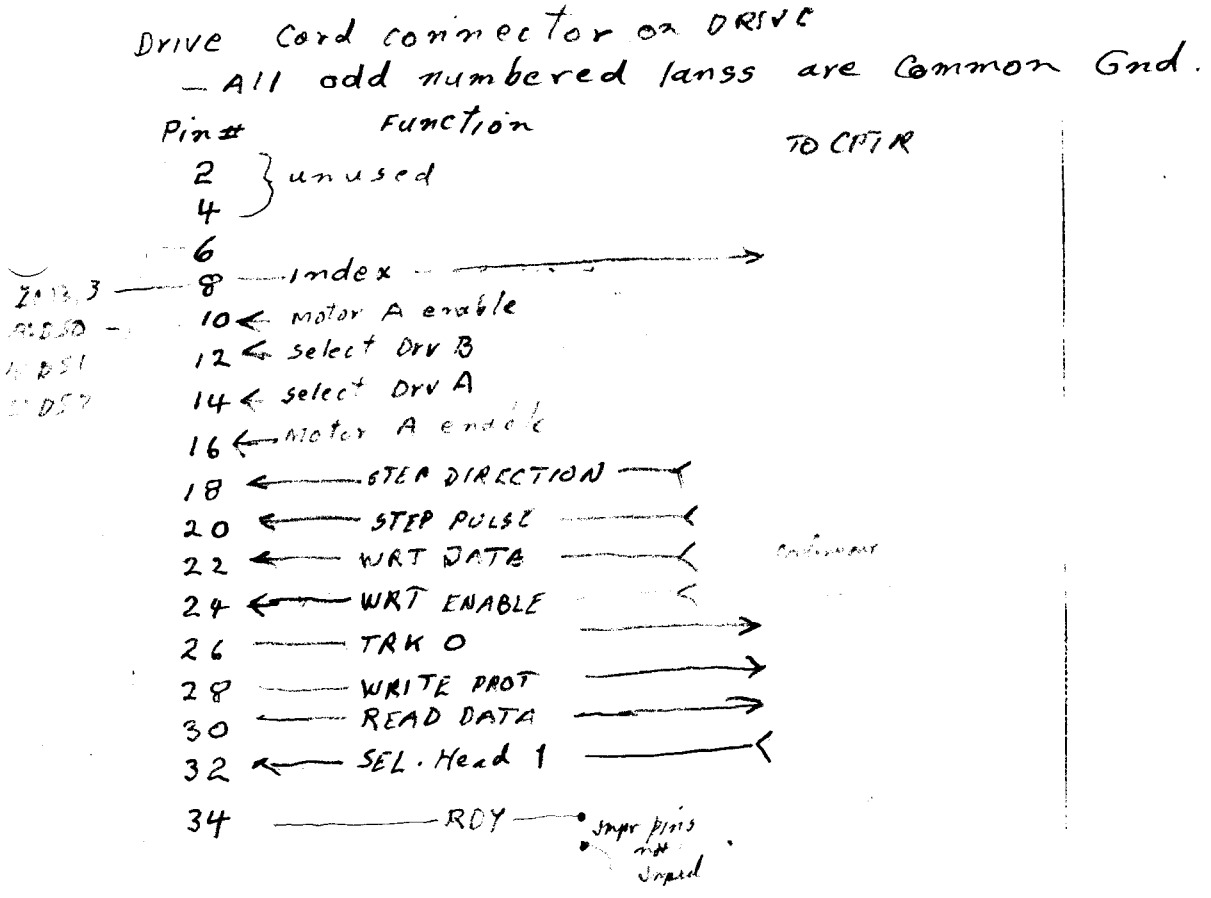
Cleaning

1) After soldering, the area must be cleaned to remove all traces of flux. The flux contains activated resins to aid the cleaning action of the flux and improve solderability. These flux resins can be corrosive and conductive.

Solder

1) The recommended solder to use is commercially available 63-37 Rosin cored solder.

2.0 Disk Drive Removal and Replacement Procedures



2.1 Tools and Test Equipment

The drives have been manufactured and assembled with precision and to tight tolerances. As a result, field service or repair of the drives is not recommended unless the user has the following tools, test and calibration equipment.

1) 5-1/4 inch Floppy Disk Drive Exerciser.

2) Dual Trace Oscilloscope, Tektronix 465 or equivalent with matched 10:1 probes.

3) Digital Voltmeter.

4) Taptite Driver #4, TORX part number TX-09.

5) Taptite Driver #6, TORX part number TX-15.

6) Torque Wrench.

7) Alignment Diskette, (DYSAN part number 800180).

Note The track positions specified in this procedure are for Dysan alignment diskettes. Other manufacturers may use different tracks.

2.2 Removal/Replacement

Control Board

1) Remove all power and control cables.

2) Disconnect P3A, P4, P5, P6 from the Control Board.

3) Using the Taptite Driver #4, remove the two screws from the front of the drive. Remove the Control Board.

4) Replacement is in the reverse order. When replacing the two screws use a torque wrench set to 4 inch-lbs.

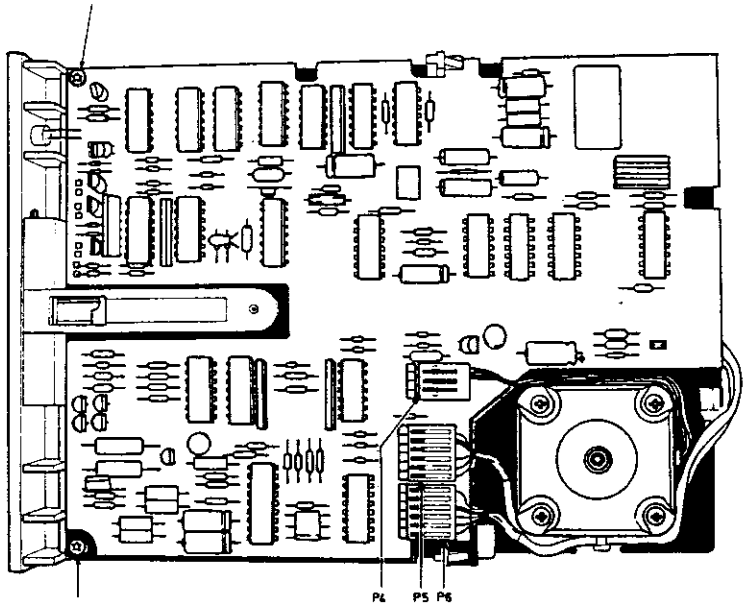


Fig. 2-1 – Control Board Removal

Motor Board

1) Remove all power and control cables.

2) Disconnect P8 at the Motor and P3B on the Control Board.

3) Disconnect the ground lugs at the rear of the Drive.

4) Using the Taptite Driver #4, remove the screws at the center and edge of the Board.

5) Replacement is in the reverse order. The Mylar washer must be installed between the Motor Board and the Drive chassis or the Motor Board will be damaged. When replacing the screws use a torque wrench set to 4 inch-lbs.

6) Perform the Motor Speed Adjustment procedure.

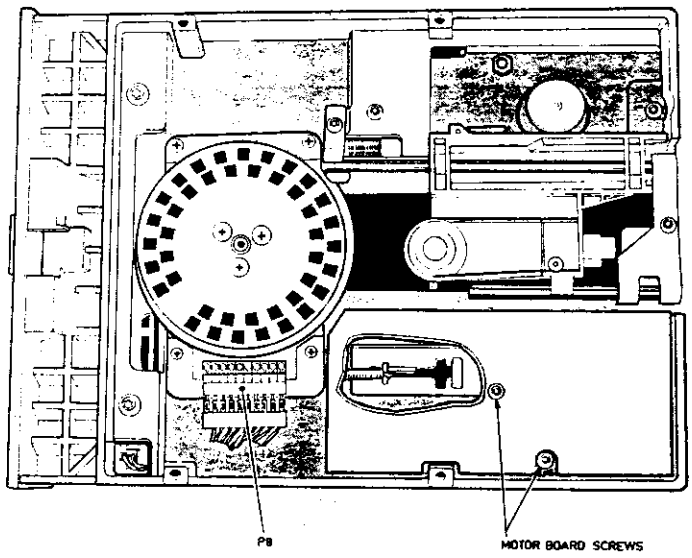


Fig. 2-2 – Motor Board Removal

Front Bezel/Clutch Assembly

1) Close the front door.

2) Remove the Control Board.

3) Disconnect the plug which connects to the write protect phototransistor sensor on the bottom (P3H).

4) Disconnect the plug which connects to the write protect sensor at the top (P3G).

5) Using the Taptite Driver #6, remove the two screws holding the Front Bezel/Clutch Assembly to the chassis.

6) Reassemble in the reverse order. Make sure the Clutch is properly seated in the Motor Assembly and the Index Pins are installed in the slots FF and GG located in the chassis. When replacing the screws use a torque wrench set to 6 inch-lbs. After assembly, open the door and check that the clutch disengages from the Motor Assembly.

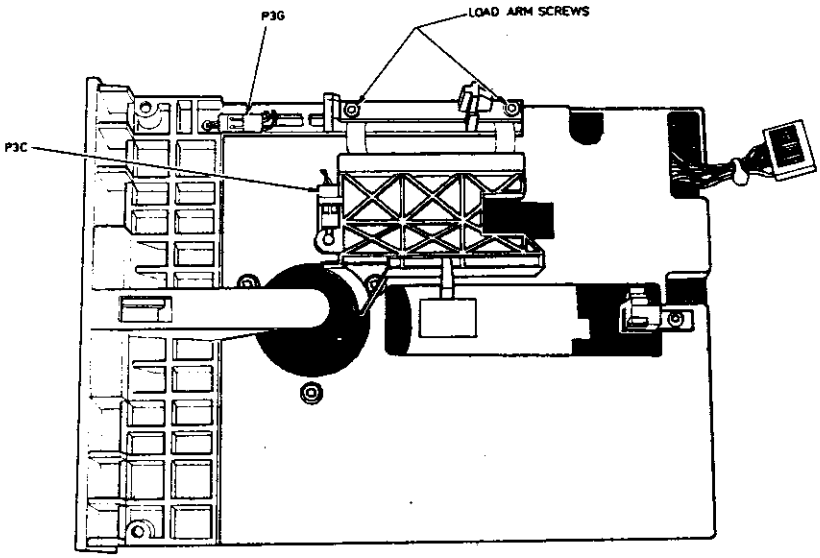


Fig. 2-3 – Location of Write Protect Sensor

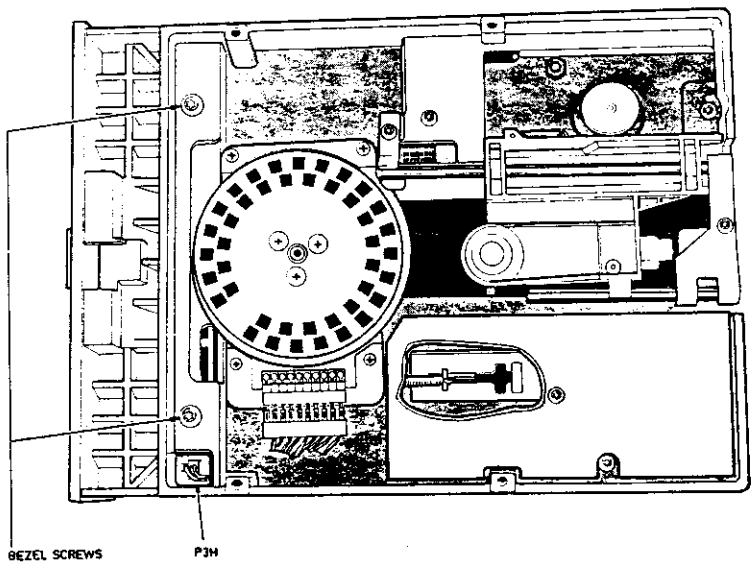


Fig. 2-4 – Location of Write Protect LED and Front Bezel Screws

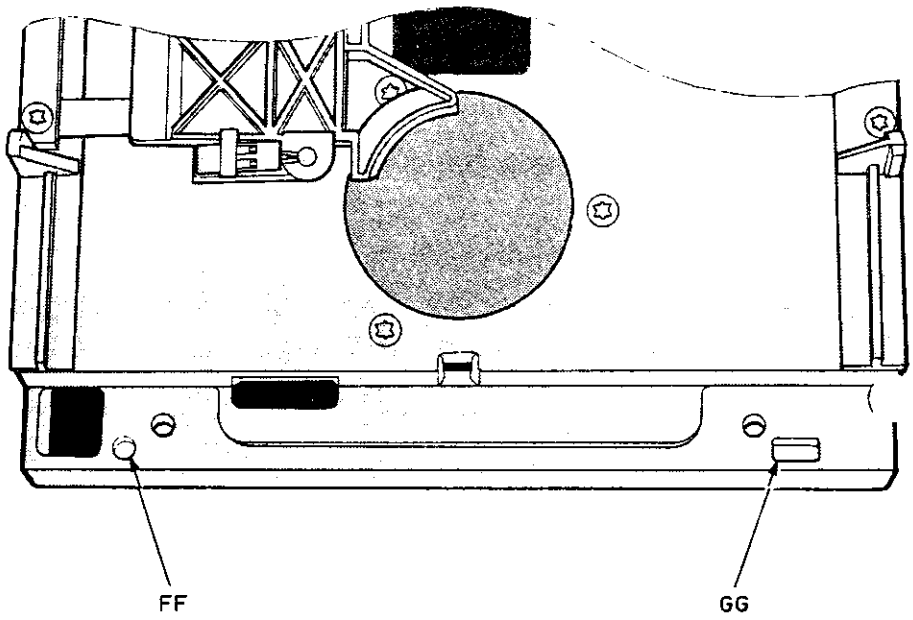


Fig. 2-5 – Front Bezel Locating Slots

Write Control Phototransistor Replacement

1) Remove the Front Bezel/Clutch Assembly.

2) The Phototransistor is press fit and need only be pulled out. Note the orientation of the flat on the Phototransistor so it can be replaced in the same orientation.

3) Clip or bend the leads to the same length as the one being replaced and install.

4) Align the new Phototransistor so that the flat is towards the nearest side of the bezel.

5) Replace the Front Bezel/Clutch Assembly.

Write Control LED Replacement

1) Remove the Front Bezel/Clutch Assembly.

2) Remove the old LED which is pressed in. Note the orientation of the flat on the LED.

3) Clip or bend the leads to the same length as the one being replaced and install.

4) Install the new LED so the flat is towards the front.

5) Replace the Front Bezel/Clutch Assembly.

Ejector and Ejector Spring Replacement

1) Remove the Control and Motor Drive Board.

2) Remove the spring from the Ejector.

3) Note the orientation of the Ejector, slide it to the rear until it can be removed through the slot. When the Ejector is removed, the Heads are free to touch, a clean piece of media should be inserted between thet Heads. When the Ejector is removed, be careful that the Heads do not bang together.

4) Install the new Ejector in the reverse manner. It may be necessary to lift the Load Arm to slide the Ejector in.

5) Install the spring. If the spring is to be replaced, it is necessary to remove the bonding agent which holds the front of the spring to the chassis. The bonding agent is not needed for replacement, simply hook the chassis side of the spring to the pin on which the bonding agent was attached.

6) Replace the Motor Drive and Control Board.

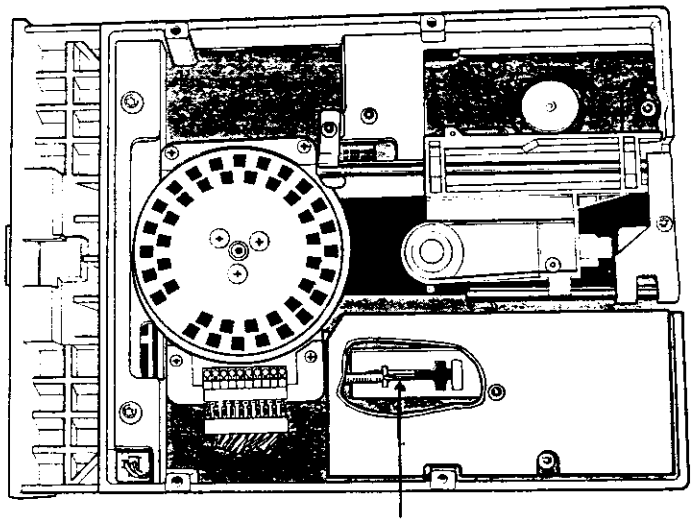


Fig. 2-6 – Ejector and Ejector Spring Removal

Load Arm/Media Guide Assembly

1) Close the front door.

2) Remove the Control Board.

3) Unplug connector P3C which connects to the Index phototransistor.

4) Using the Taptite Driver #4, remove the two screws and washers holding the Load Arm/Media Guide to the Chassis. When the Guide is removed, the Heads are free to touch, place a clean piece of media between the Heads. Be careful not to let the Heads bang together.

5) Replace in the reverse order. Use a torque wrench set to 4 inch-lbs.

6) Perform the Index Alignment procedure.

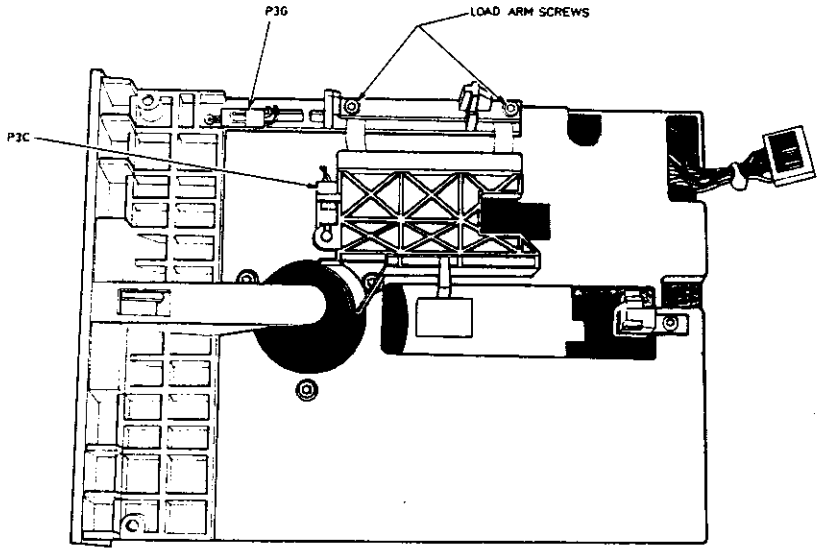


Fig. 2-7 – Load Arm Removal

Index Phototransistor

1) Remove the Load Arm/Media Guide Assembly.

2) Remove the Index Phototransistor which is press fit. Note the orientation of the flat on the phototransistor so it can be replaced in the same orientation.

3) Clip the leads to the same length as the one being replaced and install.

4) Replace the Load Arm/Media Guide Assembly.

5) Perform the Index Alignment procedure.

Track 00 Switch Replacement

1) Remove the Control and Motor Drive Board.

2) Unplug connectors P3E and P3F from the Track 00 switch.

3) Using the Taptite Driver #4, remove the screw securing the Track 00 bracket to the chassis.

4) Using the Taptite Driver #4, loosen the two screws securing the Switch to the bracket. Note the orientation of the Switch. It is important that the white dot be visible when mounted in the bracket and positioned to the bottom of the drive.

5) Reassemble in the reverse order, tighten the two screws in step 4 to a torque of 4 inch-lbs.

6) Perform the Track 00 alignment procedure.

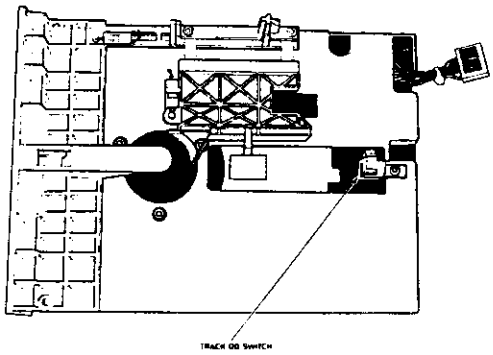


Fig. 2-8 – Track 00 Switch Removal

Head Replacement

1) Remove the Control Board.

2) Cut and remove the cable ties securing the wires from the Head to the Stepper Motor.

3) Disconnect the spring from the Head frame.

4) Remove the screw securing the stepper band to the stepper motor.

5) Remove the screw securing the stepper band to the Head frame.

6) Using the Taptite Driver #4, remove the rear screw securing the Guide Rails to the Chassis, loosen the front screw and remove the Rails.

7) Place a clean piece of media between the Heads.

8) Carefully remove the Head Assembly from the drive and remove the spring.

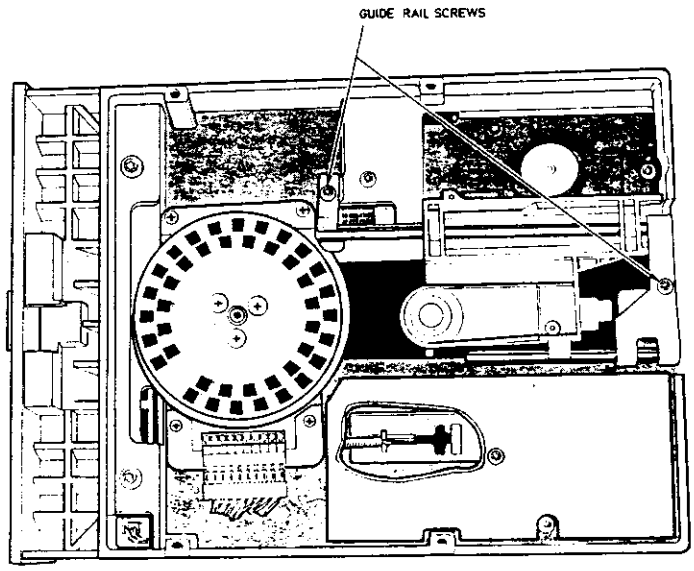


Fig. 2-9 – Head Removal

9) Install the new Head Assembly in the reverse order, be careful not to let the Heads bang together. Check that the Head Load Arm is between the Heads. When replacing the cable ties, ensure that the Head Assembly is free to move to the innermost track without binding.

10) Tighten the two screws securing the Guide Rails to 4 inch-lbs.

11) Perform the following alignment procedures:
    A) Head load force
    B) Track 00
    C) Radial Alignment

Head Load Force Adjustment

1) Remove the Control Board.

2) Insert a diskette part way to engage the eject mechanism.

3) Remove the diskette, insert a small piece of media between the Heads and close the door.

4) Position the Drive on its side and attach a Gram Gauge to the Head, be careful not to damage the spring on the Head. Carefully pull the Gram Gauge (at 90 degrees to the Head) until the media falls out.

5) The force required to separate the Heads should be 20 +/-2 Grams. If necessary adjust the set screw on the Head, in or out, to obtain the required pressure. Secure the set screw with locktite.

Stepper Motor Replacement

1) Disconnect J4 from the Control Board and cut the cable ties from the Stepper Motor.

2) Remove the spring securing the stepper band to the Head Frame.

3) Remove the screw securing the stepper band to the Stepper Motor.

4) Using the Taptite Driver #4, remove the two screws securing the Stepper Motor mounting plate to the chassis.

5) Replacement is in the reverse order.

6) Tighten the screws to 4 inch-lbs.

7) Perform the Radial Alignment procedure.

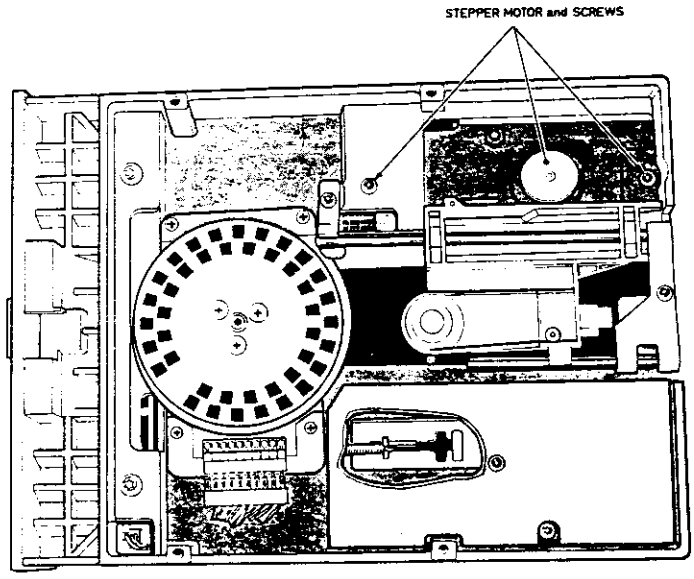


Fig. 2-10 – Stepper Motor Removal

2.3 Alignment and Adjustments

Equipment Set-up

Note Any alignment should be performed in an environment of 50% humidity and at a temperature of 70° F +/-5. The media being used to align drives must be in this environment for at least 24hrs prior to alignment.

Configure the Drive Exerciser for:

5 inch Drive.
40 Tracks.
Double density.
2 Heads.
Single Sector.

Set-up the oscilloscope for:

Channel 1	AC
Channel 2	AC Inverted
Vert. Mode	+ ADD
Sec/div	20 msec
Trigger	Normal/external
Volts/div	0.1 mV (using 10x probes).

Oscilloscope connection test points (Ref Fig. 2-11)

Channel 1	TP5 (L2) on Control Board
Channel 2	TP6 (L3) on Control Board
Grounds	+ ve side of C26
Trigger	TP3 (R38) on Control Board
Ground	-ve side of C12

Sequence of alignments and adjustments:

Motor Speed Adjustment
Track 00
Index Alignment
Radial Alignment
Read/Write Current
Write Current Adjustment

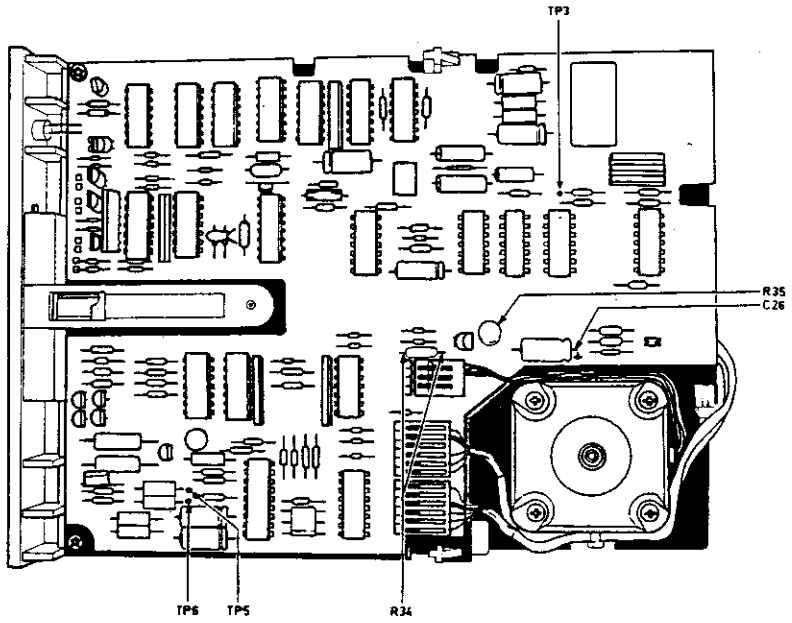


Fig. 2-11 – Disk Drive Test Points

Motor Speed Adjustment

1) Connect the power and control cables from the exerciser to the drive.

2) Connect the motor PCB ground to the lug on the Drive chassis.

3) Change Channel 1 and 2 to 0.1 Volts/Div.

4) Insert the alignment diskette.

5) Return the Head to Track 0, then step to Track 1.

6) Observe that the index pulse is 200 msec +/- 2 msec. The dark lines on the Drive Motor spindle should appear motionless if viewed with an ultraviolet light.

7) Adjust R30 on the Motor Control Board if necessary and secure with locktite.

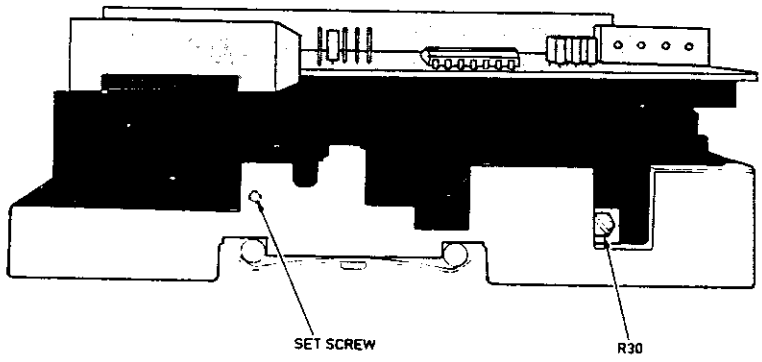


Fig. 2-12 – Motor Speed Adjustment Resistor

Track 00 Adjustment

Connect the oscilloscope to:

Channel 1	A8, Pin14
External Trigger	B11, Pin12

Set the oscilloscope for:

Time/Div	1 msec
Volts/Div	2 Volts
Trigger	Normal, External/AC

Set the exerciser for:

Step Rate	3 msec
Auto seek between Tracks 0 and 3	

1) Start the Drive and exerciser.

2) The signal should be as shown below. If not perform the following adjustment.

3) Loosen the Track 00 screw accessible thru the small hole near J-1.

4) Adjust the Track 00 sensor for a signal of 5.25 +/- 0.25 msec.

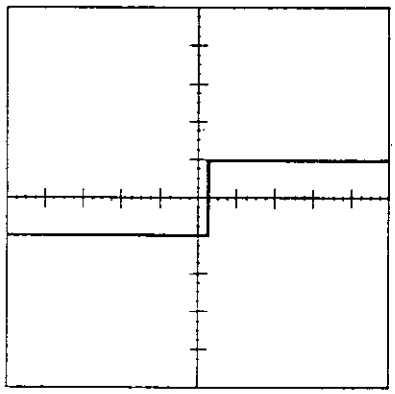


Fig. 2-13 – Track 00 Waveform

Index Alignment

Change the oscilloscope to:

Time/div	50usec
Volts/div	0.1 volt
Channel 1&2	Inverted
Positive Trigger	

1) Insert the alignment diskette.

2) Step to Track 1.

3) The display on the oscilloscope should be 200usec +/- 50usec.

4) If the display is not as above, loosen the Load Arm screws, move the Load Arm all the way towards the Bezel, (be careful not to pinch the write protect or index wires), slowly move the Load Arm towards the rear of the Drive, when the leading edge of the pulse is at 200usec, tighten the screws to 6 inch-lbs.

5) Check the signal on Head 1. If the Heads are not aligned with each other, the signal may not be on 200usec. If this is the case, adjust the Load Arm so that the signal is off on each Head by the same amount.

6) Step to Track 34.

7) Check the Index on both Heads and adjust if necessary. If the Load Arm is adjusted, repeat the check at Track 1.

8) Check the Head Azimuth. Set the Time/div to 1 msec. The tolerance is +/- 18 minutes of angle. If the Azimuth is out of tolerance, replace the Head.

9) Return to Track 0.

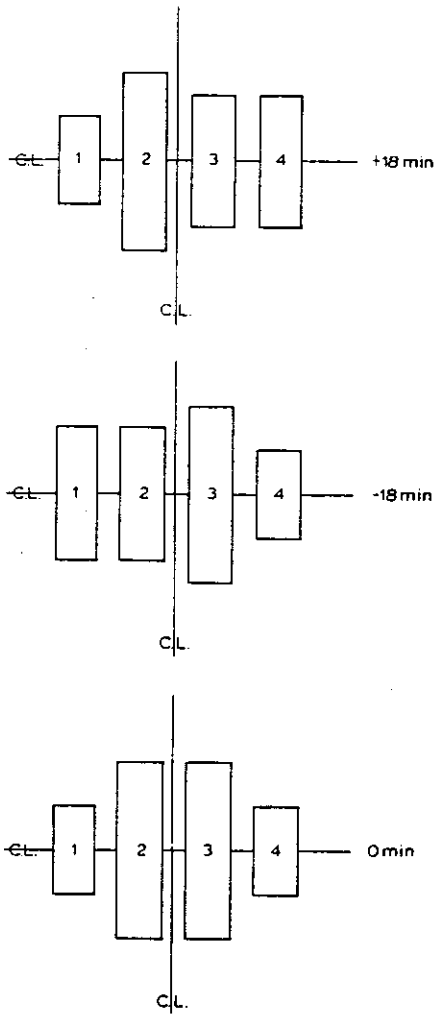


Fig. 2-14 – Head Azimuth Waveforms

Radial Alignment

1) Insert the alignment diskette.

2) Step to Track 0 then out to Track 16.

3) The display on the screen should be similar to that shown below.

4) Turn the Volts/div to 20mv and adjust the lobes for equal amplitude. To adjust, loosen the two Stepper Motor alignment screws 1/4 turn and move the alignment set screw forward or reverse to obtain the correct cat-eye position. Tighten the alignment plate screws and ensure that the position did not change.

5) Return the Head to Track 0, then out to Track 16 and check that the cat-eye is within 15% of each other.

6) Step from Track 16 to Track 39 and return to Track 16, the cat-eye should be within 15% of each other.

7) Repeat the alignment procedure on Head 1.

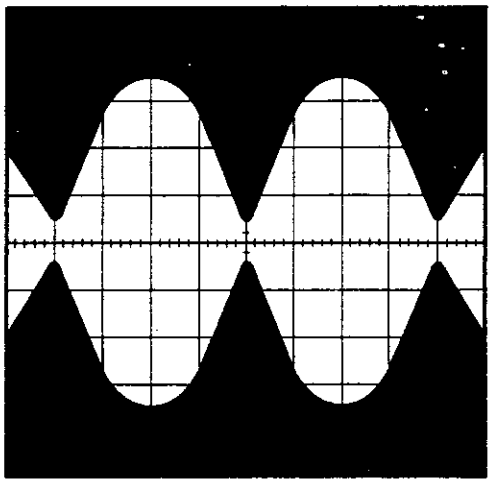


Fig. 2-15 – Radial Alignment Waveform

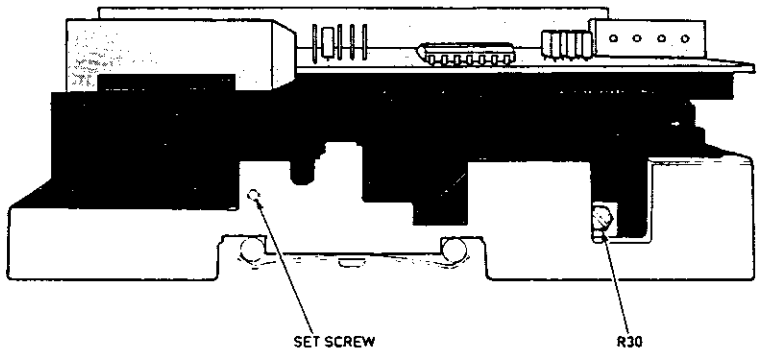


Fig. 2-16 – Radial Alignment Adjustment Set Screw

Read/Write Amplitude

1) Insert a scratch diskette and return to Track 0.

2) Perform an erase.

3) Write data and check the signal on the oscilloscope is 550mv +/-50mv.

4) Step to Track 39.

5) Perform an erase.

6) Write data and check the signal on the oscilloscope is 230mv +/-50mv.

7) Perform the Write Current Adjustment if necessary.

Write Current Adjustment

1) Return to Track 0.

2) Install a scratch diskette halfway into the drive.

3) Connect the Volt Meter leads across R34.

4) The reading should be 400mv +/- 3mv, if this is not correct, adjust potentiometer R35 and secure with locktite.

The Disk Drives were modified to improve reliability on the high tracks. The errors were noticeable when running the disk diagnostics and the majority of errors occur on Tracks 35 to 39. Resistors R15 and R16 were changed from 51.1 ohms to 91 ohms, 5% 1/2 watt.

If the Disk Drive has these resistors installed, the following changes are required to the Write Current Adjustment.

1) Return to Track 0.

2) Install a scratch diskette halfway into the drive.

3) Connect the Volt Meter leads across R34.

4) The reading should be 350mv +/- 3mv, if this is not correct, adjust potentiometer R35 and secure with locktite.

2.4 Troubleshooting Guide

A. Track 0 not adjustable:

Track 0 switch defective
Logic Board defective

B. Motor Speed not adjustable:

Loose connector at J3
Defective Motor Control Board
Loose connector at Drive Motor
Defective Index LED or Detector
Defective Logic Board
Clutch not engaged properly

C. Cat-eye not adjustable or fails position test:

Loose set screw on pulley
Eject mechanism defective
Damaged Heads
Damaged Guide Rails
Load Arm not adjusted properly
Head riding on Load Arm
Head wire too tight at Stepper Motor

D. Index not adjustable:

Damaged Heads
Eject mechanism bad
Connector not seated or making poor contact
Defective Logic Board

E. Write current not adjustable:

Defective Logic Board

3.0 Hyperion Board Level Troubleshooting

3.1 General

This section details a method of troubleshooting the Hyperion Revision 4 and Revision 5 boards when the problem has not been isolated by the diagnostics, or to check a particular area of the boards isolated by the diagnostics.

The method to follow when troubleshooting is to check:

1) The power supply voltages.
2) That all connections and chips are properly seated.
3) That all ECO wires are firmly attached.
4) For shorts and blown components on the Boards.
5) Clocks and signals to/from the various chips.

3.2 System Board

Symptom	Check
1) Computer does not power up	Power supply output voltages. Voltage levels at boards, CRT and drives.
2) Computer powers up but does not boot	Diskette is good, try booting from other drive. All chips are properly seated. All ECO wires are connected. Replace EPROM (U48). Main clock (14MHZ/0.07usec) at U83-17 (X1), and U83-12 (OSC). Follow the signal through the Board. The clock can also be checked on the Display & I/O Board. CPU clock (4.77MHZ/0.21usec) at U83-8 (MCLK). Follow the signal through the Board. The clock can also be checked on the Display & I/O Board. Reset signal (70usec) at U83-10. Follow the signal through the Board. The reset signal can also be checked on the Display & I/O Board.
3) Loss of information	Refresh timer (80KHZ/14usec) at U94-10 for Revision 4 Hyperions and at U100-11 for Revision 5 Hyperions. DREQ0 at U31-6 and U47-19 going high, RFSH at U55-25 and RASI at U55-3 are low.

4) Hard error	Use a new diskette. Check all connections to drives. Run disktest to isolate the problem to a drive or the system board. If the hard error is found on both drives the system board is the probable cause. Replace the System Board and re-run disktest. FDC clock (8MHZ/0.125usec) at U27-8. Replace the FDC (U50). Replace the Data Separator (U91). Check the Drive alignments.
5) Unable to access a peripheral	All cables and connections to the peripheral tight and that the peripheral is operational. PIC (U43) interrupt lines (IR0-7). PIC interrupt to the CPU (U43-17). Interrupt acknowledge from the Bus Controller (U18-14) to the PIC. Refresh circuitry.
6) Parity errors	Parity Generator/Checker. Output of U29-9 (Parity Error).
7) CRT does not echo Keyboard	Replace Keyboard. Serial data from Keyboard (U89-2). Keyboard interrupt from Keyboard at the PIC (U43-19). CRT section of the Display & I/O Board.

3.3 Display & I/O Board

Symptom	Check
1) General checks	Board crystal at U12-8 (12.46MHZ/0.08usec). DOTCLK (12MHZ/0.08usec) at U13-5 or (6MHZ/0.16usec) at U13-4. External BAUD clock at U7-9 (1.55MHZ/0.64usec). RTC at U11-14 (32.76KHZ/30.5usec). External Master clock at J2-20 (4.77MHZ/0.21usec). External oscillator at J2-38 (14.32MHZ/0.07usec). DTMF clock at U70-20 (3.57MHZ/0.28sec). DC1-8 at U62-12-19.
2) Loss of Video	The connector to the CRT board tight. Connect an external monitor to the Composite Video Jack to check for signal. Diodes D1 and D3 and resistors R17 and R19, U66-3&5, and U21-1.
3) Loss of Sync	VSYNC (60HZ/16.6msec) at U66-16 and U75-12. HSYNC (15.8KHZ/63usec) at U66-18 and U75-13.
4) Loss of Attributes	DC1 at U1-3&11.
A) Super/Sub Script	FAT3 at U1-2. FAT4 at U1-12. Output of U1-5&9. SL0-3 from U75. Output of adder U2.

B) Double Width	FAT 6&7 at U10-9&11. Replace U10.
C) Intensify	FAT 5 at U37-2. DC4 at U37-3&11. Output of U37-9. DC8 at U49-11. Output of U49-9.
D) Underline	FAT 0 at U21-20. Replace U21.
E) Reverse video	FAT 1 at U21-21. Replace U21.
F) Blink character	FAT 2 at U21-24. Replace U21.
5) Displays wrong character	Replace keyboard. Replace Character Generator (U3). System Board keyboard circuitry.
6) Missing Grey scales in Low Resolution mode	Voltage levels at J1-2. They should be 0V, 1.6V, 2V, 2.2V. Diodes D1&3, Resistors R17&19. Output of U66-3,5,7&9. Output of U31-13 and U15-13. Output of U35-4&7. Output of U29-4&7.

3.4 Modem Board

Symptom	Check
1) General checks	DTMF clock at U1-7 (3.58MHZ/0.28usec). Modem clock at U2-8 (4.03MHZ/0.25usec).
2) Modem non-operational	Replace Modem board to isolate problem to the Modem board. Replace U2.
3) Will not dial	Row and column inputs to U1. Tone output at U1-16. DTMF clock at U1-7. Output of U4-8. Output of U9-7.
4) No speaker volume control	Amplifier U5 inputs 6,12 and 13. If one of these inputs is high, the output of the corresponding section of the amplifier should be higher than its input.

3.5 Debug Usage

Debug is a programming tool used to alter the contents of registers, or to access a specific location in memory. For a complete description of debug commands and their execution refer to the Programmers Guide.

The following debug commands will be used for troubleshooting.

COMMAND	FUNCTION
D(range)	Display the contents of the region of memory specified by the (range).
F(range)(list)	Fill the addresses in the (range) with the values in the (list).
I(value)	Input and display one byte from the port specified by (value).
O(value)(byte)	Output the (byte) specified to the output port specified by (value).
Q	Terminates debug and returns control of the system to the MS-DOS commands.

After all commands, a carriage return is used to start executing the command.

Examples of Debug

1) Mode selection not working — Mode selection is achieved through software using the control register at address A0000, this is an eight bit register.

Control Register Bits								Hex Function	
CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0		
1	1	1	0	0	0	0	0	E0	Normal Cursor
1	0	1	0	0	0	0	0	A0	Underline Blinking
0	1	1	0	0	0	0	0	60	Invisible Cursor
1	1	1	1	0	0	0	0	F0	6MHz DOTCLK
1	1	1	0	1	0	0	0	E8	Hyperion Attributes
1	1	1	0	0	1	0	0	E4	High Resolution
1	1	1	0	0	1	1	0	E6	Low Resolution
1	1	0	0	0	0	0	0	C0	70Hz Scan Rate
1	1	1	0	0	0	0	1	E1	Row Table Mode

Using the above table and DEBUG, certain sections of the Display & I/O Board can be checked.

Debug is entered by the command, Debug (Rtn). When the prompt (>) appears the commands can be entered.

A) To test the 70Hz scan rate, type the following:

>FA000:0 L 1 C0 (Rtn) — The characters on the CRT will have increased in size by 10%.

B) To test Cursor functions, type the following:

>FA000:0 L 1 60 (Rtn) — The cursor should be invisible.

C) To test the Low resolution graphics, type the following:

>FA000:0 L 1 E6 (Rtn) — The display will change from alphanumerics to graphics (320 x 250).

D) To test the PPI (U4).

The PPI is located at address 140-143, with the Control Register at 143. The other three locations are the ports.

To check HS1, one of the control lines for the Modem Board, type the following:

>0143 80 (Rtn)	This command makes Port C all outputs, by entering the command >0142 10 (Rtn) the relay on the Modem Board is energized. The relay is de-energized by the command >0142 00 (Rtn).

E) To test areas of Memory.

To check a location in sector 0 at 03FF for its ability to be written to and read back, type the following:

>F03FF:0 L 2 55 AA (Rtn)	This command would write 55 AA to the first and second location consecutively.

To check the written locations for their ability to be read back properly, type the following:

>D03FF:0 L 2 (Rtn)	This command will dump out the contents for the specified two areas, the results should be 55 AA, if they are not then there is a problem with that area of Memory and the chip should be replaced.

Note The above test would only be used to verify an error detected by the RAMTEST diagnostic.

4.0 Parts List

4.1 How to Use This Parts List

1) Locate the Engineering reference of the defective part from the Board silk screen.

2) Refer to the notes in the accompanying list to determine which revision level of parts list to use. Engineering references may not be the same with each revision of the board.

3) Refer to the accompanying list to find the description and the Hyperion part number.

System Board

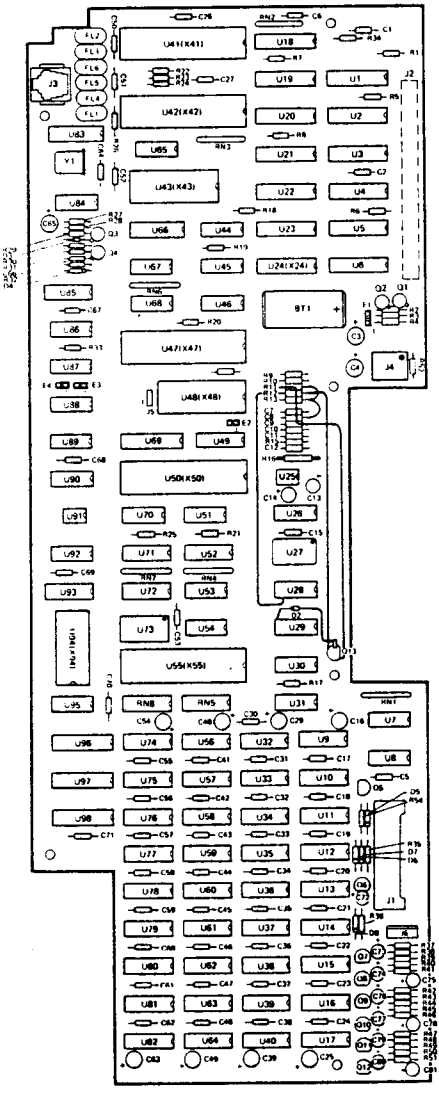


Fig. 4-1 – System Board Layout

4.4 PWA System Board A6 Parts List Revision Level: 12

Note This parts list is to be used for those System Boards from Revision 10 to 12.

Item	Reference	Part Number	Description
1	U1-U5	900045-000	IC 74LS244 OCTAL BUFFER
2	U6	900046-000	IC 74LS245 OCTAL BUS TRANCEIVER
3	U7	900010-000	IC 74LS14 HEX SCHMITT INVERTER
4	U8	900003-002	IC 74S04 HEX INVERTER
5	U9-U17	900815-000	IC 2164A-20 65536 BIT DRAM
6	U18	900073-000	IC 8288 BUS CONTROLLER
7	U19-U21	900054-000	IC 74LS373 OCTAL D LATCH
8	U22-U24	900087-000	IC PAL10L8
9	U25	900078-000	IC LM386 AUDIO POWER AMP
10	U26	900007-001	IC 74LS08 QUAD AND GATE
11	U27	900810-000	OSC HYBRID CLOCK MX050-2-8.00MHZ
12	U28,U29	900018-001	IC 74LS74A DUAL D FLIP-FLOP
13	U30	900023-000	IC 74LS125A QUAD BUFFER
14	U31	900018-001	IC 74LS74A DUAL D FLIP-FLOP
15	U32-U40	900815-000	IC 2164A-20 65536 BIT DRAM
16	U41	900066-000	IC 8088 8BIT HMOS MICROPROCESSOR
16A	X41	900331-000	SOCKET IC 40 PIN
17	U42	******-***	NOT USED
17A	X42	900331-000	SOCKET IC 40 PIN
18	U43	900070-000	IC 8259A-5 PIC
18A	X43	900816-000	SOCKET IC 28 PIN
19	U44	900000-003	IC 74ALS00 QUAD NAND GATE
20	U45	900018-002	IC 74ALS74 DUAL D FLIP-FLOP
21	U46	900014-001	IC 74LS32 QUAD OR GATE
22	U47	900067-000	IC 8237A-5 DMA CONTROLLER
22A	X47	900331-000	SOCKET IC 40 PIN
23	U48	900062-000	IC 2764A-3 8Kx8 EPROM
23A	X48	900816-000	SOCKET IC 28 PIN
24	U49	900059-000	IC 74LS670 4x4 REGISTER
25	U50	900071-000	IC 8272 FDC
25A	X50	900331-000	SOCKET IC 40 PIN
26	U51	900018-001	IC 74LS74A DUAL D FLIP-FLOP
27	U52	900043-001	IC 74LS195 4BIT PIPO SHIFT REG.
28	U53	900000-002	IC 74LS00 QUAD NAND GATE
29	U54	900007-001	IC 74LS08 QUAD AND GATE
30	U55	900074-000	IC AM2964B DRAM CONTROLLER
30A	X55	900331-000	SOCKET IC 40 PIN
31	U56-U64	900815-000	IC 2164A-20 65536 BIT DRAM
32	U65	900013-001	IC 74LS30 NAND GATE
33	U66	900046-000	IC 74LS245 OCTAL BUS TRANCEIVER
34	U67	900018-001	IC 74LS74A DUAL D FLIP-FLOP
35	U68	900010-000	IC 74LS14 HEX SCHMITT INVERTER
36	U69	900054-000	IC 74LS373 OCTAL D LATCH
37	U70	900018-001	IC 74LS74A DUAL D FLIP-FLOP
38	U71	900033-000	IC 74LS161A 4BIT BINARY COUNTER
39	U72	900039-000	IC 74LS175 QUAD D FLIP-FLOP

40	U73	900170-000	SEMI RCLL-13-11 DIG DELAY MODULE
41	U74-U82	900815-000	IC 2164A-20 65536 BIT DRAM
42	U83	900072-000	IC 8284A CLOCK GENERATOR
43	U84	900023-000	IC 74LS125A QUAD BUFFER
44	U85	900039-000	IC 74LS175 QUAD D FLIP-FLOP
45	U86	900007-001	IC 74LS08 QUAD AND GATE
46	U87	900003-003	IC 74LS04 HEX INVERTER
47	U88	900023-000	IC 74LS125A QUAD BUFFER
48	U89	900010-000	IC 74LS14 HEX SCHMITT INVERTER
49	U90	900003-003	IC 74LS04 HEX INVERTER
50	U91	900076-000	IC FDC9216B FDDS
51	U92	900001-001	IC 74LS02 QUAD NOR GATE
52	U93	900039-000	IC 74LS175 QUAD D FLIP-FLOP
53	U94	900068-000	IC 8253A-5 PROG. INTERVAL TIMER
53A	X94	900330-000	SOCKET IC 24 PIN
54	U95	900049-000	IC 74LS280 PARITY GENERATOR
55	U96	900051-000	IC 74LS322A 8BIT SHIFT REGISTER
56	U97.U98	900045-000	IC 74LS244 OCTAL BUFFER
57	U99	900018-001	IC 74LS74A DUAL D FLIP-FLOP
58	U100	900057-001	IC 74LS393 DUAL 4BIT COUNTER
59	D1,D2	******-***	NOT USED
60	D3	900147-000	SEMI 1N4148 SIGNAL DIODE
61	D4	900837-000	SEMI 1N748A DIODE ZENER 3.9V 5%
62	D5	900147-000	SEMI 1N4148 SIGNAL DIODE
63	D6	900838-000	SEMI IN4735A DIODE ZENER 6.2V 1W
64	D7	900147-000	SEMI 1N4148 SIGNAL DIODE
65	D8	900840-000	SEMI 1N4001 DIODE
66	Q1	900172-001	SEMI 2N2222A TRANSISTOR
67	Q2	900175-000	SEMI 2N2907 TRANSISTOR
68	Q3,Q4	900172-001	SEMI 2N2222A TRANSISTOR
69	Q5	******-***	NOT USED
70	Q6	900175-000	SEMI 2N2907 TRANSISTOR
71	Q7	900844-000	SEMI BC308C TRANSISTOR PNP
72	Q8	900172-001	SEMI 2N2222A TRANSISTOR
73	Q9	900844-000	SEMI BC308C TRANSISTOR PNP
74	Q10	900172-001	SEMI 2N2222A TRANSISTOR
75	Q11	900844-000	SEMI BC308C TRANSISTOR PNP
76	Q12	900172-001	SEMI 2N2222A TRANSISTOR
77	Q13	******-***	NOT USED
78	R1	900183-001	RES FIXED COMP 5% 1/4W 33 OHMS
79	R2	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
80	R3	900190-022	RES CARBON FILM 5% 1/4W 51K OHMS
81	R4	900190-013	RES CARBON FILM 5% 1/4W 820 OHMS
82	R5-R8	900183-001	RES FIXED COMP 5% 1/4W 33 OHMS
83	R9,R10	900190-021	RES CARBON FILM 5% 1/4W 47K OHMS
84	R11	900190-015	RES CARBON FILM 5% 1/4W 1K OHMS
85	R12	******-***	NOT USED
86	R13	900190-032	RES CARBON FILM 5% 1/4W 6.2K OHM.
87	R14	900190-004	RES CARBON FILM 5% 1/4W 100 OHMS
88	R15	900190-000	RES CARBON FILM 5% 1/4W 10 OHMS
89	R16	900191-002	RES CARBON FILM 5% 1/2W 33 OHMS
90	R17	900190-008	RES CARBON FILM 5% 1/4W 200 OHMS
91	R18-R26	900183-001	RES FIXED COMP 5% 1/4W 33 OHMS

92	R27	900190-008	RES CARBON FILM 5% 1/4W 200 OHMS
93	R28	900190-027	RES CARBON FILM 5% 1/4W 2.7K OHMS
94	R29	900190-022	RES CARBON FILM 5% 1/4W 51K OHMS
95	R30	900190-016	RES CARBON FILM 5% 1/4W 2K OHMS
96	R31,R32	900190-005	RES CARBON FILM 5% 1/4W 110 OHMS
97	R33,R34	900183-001	RES FIXED COMP 5% 1/4W 33 OHMS
98	R35	******-***	NOT USED
99	R36	900190-007	RES CARBON FILM 5% 1/4W 150 OHMS
100	R37	900190-048	RES CARBON FILM 5% 1/4W 680 OHMS
101	R38	900190-049	RES CARBON FILM 5% 1/4W 100K OHMS
102	R39	900190-021	RES CARBON FILM 5% 1/4W 47K OHMS
103	R40	900190-050	RES CARBON FILM 5% 1/4W 16K OHMS
104	R41	900190-037	RES CARBON FILM 5% 1/4W 22K OHMS
105	R42	900190-048	RES CARBON FILM 5% 1/4W 680 OHMS
106	R43	900190-049	RES CARBON FILM 5% 1/4W 100K OHMS
107	R44	900190-051	RES CARBON FILM 5% 1/4W 39K OHMS
108	R45	900190-050	RES CARBON FILM 5% 1/4W 16K OHMS
109	R46	900190-037	RES CARBON FILM 5% 1/4W 22K OHMS
110	R47	900190-048	RES CARBON FILM 5% 1/4W 680 OHMS
111	R48	900190-049	RES CARBON FILM 5% 1/4W 100K OHMS
112	R49	900190-038	RES CARBON FILM 5% 1/4W 33K OHMS
113	R50	900190-050	RES CARBON FILM 5% 1/4W 16K OHMS
114	R51	900190-037	RES CARBON FILM 5% 1/4W 22K OHMS
115	R52	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
116	R53,R54	******-***	NOT USED
117	R55,R56	900190-001	RES FIXED COMP 5% 1/4W 33 OHMS
118	R57,R58	900190-031	RES CARBON FILM 5% 1/4W 3.3K OHMS
119	RN1-RN4	900796-000	RES SIP 8PIN 7RES 0.2W 2% 3.3K OHMS
120	RN5	900200-000	RES DIP 16PIN 8RES 1/4W 33 O HMS
121	RN6,RN7	900796-000	RES SIP 8PIN 7RES 0.2W 2% 3.3K OHMS
122	RN8	900200-000	RES DIP 16PIN 8RES 1/4W 33 OHMS
123	C1,C2	900811-002	CAP CERAMIC 20% 100V 0.1uF
124	C3	900213-002	CAP TANTALUM 10% 6.3V 33uF
125	C4	900214-000	CAP TANTALUM 10% 16V 33uF
126	C5,C6	900811-002	CAP CERAMIC 20% 100V 0.1uF
127	C7	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
128	C8	900224-005	CAP CERAMIC 10% 50V 3300PF
129	C9	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
130	C10	900224-005	CAP CERAMIC 10% 50V 3300PF
131	C11	900225-007	CAP CERAMIC 10% 100V 0.047uF
132	C12	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
133	C13	900215-002	CAP TANTALUM 10% 35V 22uF
134	C14	900859-000	CAP TANTALUM 20% 16V 47uF
135	C15	******-***	NOT USED
136	C16	900213-000	CAP TANTALUM 10% 6.3V 4.7uF
137	C17-C24	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
138	C25	900213-000	CAP TANTALUM 10% 6.3V 4.7uF
139	C26,C27	900225-007	CAP CERAMIC 10% 100V 0.047uF
140	C28	******-***	NOT USED
141	C29	900213-000	CAP TANTALUM 10% 6.3V 4.7uF
142	C30-C38	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
143	C39,C40	900213-000	CAP TANTALUM 10% 6.3V 4.7uF

144	C41-C48	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
145	C49	900213-000	CAP TANTALUM 10% 6.3V 4.7uF
146	C50,C51	900225-003	CAP CERAMIC 10% 100V 47PF
147	C52,C53	900811-002	CAP CERAMIC 20% 100V 0.1uF
148	C54	900213-000	CAP TANTALUM 10% 6.3V 4.7uF
149	C55-C62	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
150	C63	900213-000	CAP TANTALUM 10% 6.3V 4.7uF
151	C64	900225-001	CAP CERAMIC 10% 100V 12PF
152	C65	900213-001	CAP TANTALUM 10% 6.3V 10uF
153	C66-C71	900811-002	CAP CERAMIC 20% 100V 0.1uF
154	C72	900859-000	CAP TANTALUM 20% 16V 47uF
155	C73	900217-001	CAP TANTALUM 20% 35V 0.22uF
156	C74	900859-002	CAP TANTALUM 20% 16V 2.2uF
157	C75	900859-001	CAP TANTALUM 20% 16V 10uF
158	C76	900217-001	CAP TANTALUM 20% 35V 0.22uF
159	C77	900859-002	CAP TANTALUM 20% 16V 2.2uF
160	C78	900859-001	CAP TANTALUM 20% 16V 10uF
161	C79	900217-001	CAP TANTALUM 20% 35V 0.22uF
162	C80	900859-002	CAP TANTALUM 20% 16V 2.2uF
163	C81	900859-001	CAP TANTALUM 20% 16V 10uF
164	J1	900474-000	HEADER LOW PROFILE 34 POSITION
165	J2	900475-000	RECEPTACLE 64 POSITION
166	J3	900476-000	JACK PCB MODULAR 6 POSITION
167	J4	900471-000	HEADER W/LOCK 4 POSITION
168	J5	900477-000	HEADER 2 POSITION
169	J6	900863-000	HEADER 4 POSITION
170	E1	900806-000	HEADER 2PIN ASSY, SINGLE ROW
171	E2	900807-000	HEADER 3PIN ASSY, SINGLE ROW
172	E3	900806-000	HEADER 2PIN ASSY, SINGLE ROW
173	E4,E5	******-***	NOT USED
174	E6-E8	900806-000	HEADER 2PIN ASSY, SINGLE ROW
175	Y1	900173-000	CRYSTAL MP143 14.31818MHZ
176	BT1	900260-000	BATTERY 2.4V RECHARGE NICAD
177	FL1-FL6	900781-000	CHOKE
178		900808-000	JUMPER 2 CIRCUIT
179		900478-000	WIRE KYNAR 30AWG YEL

Display and I/O Board

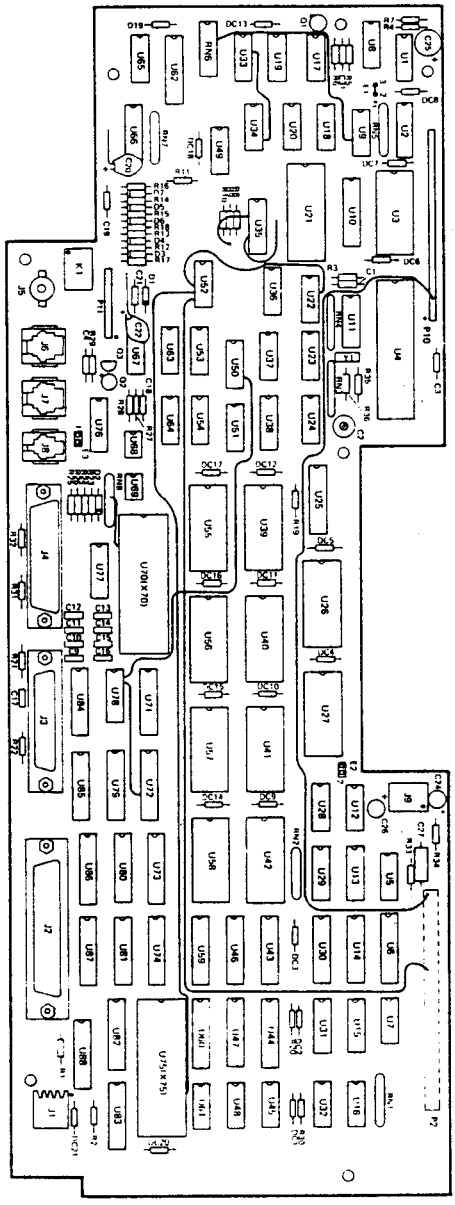


Fig. 4-2 – Display and I/O Board

4.7 PWA Display and I/O Board A7 Parts List Revision Level: 08

Note This parts list is to be used for those Display & I/O Boards from Revision 06 to 08.

Item	Reference	Part Number	Description
1	U1	900018-002	IC 74ALS74 DUAL D FLIP-FLOP
2	U2	900050-000	IC 74LS283 4BIT BINARY ADDER
3	U3	700001-000	EPROM CHARACTER GENERATOR
4	U4	900069-000	IC 8255A-5 PROG PERIPHERAL INTERFACE
5	U5	900010-000	IC 74LS14 HEX SCHMITT INVERTER
6	U6	700005-000	GENERATOR ATTRIBUTES
7	U7	900018-001	IC 74LS74A DUAL D FLIP-FLOP
8	U8	900018-002	IC 74ALS74 DUAL D FLIP-FLOP
9	U9	900001-001	IC 74ALS02 QUAD NOR GATE
10	U10	710004-000	GENERATOR DOUBLE WIDTH
11	U11	900085-000	IC MSM58321RS CMOS RTC CAL
12	U12	900181-000	OSC HYBRID CLOCK 12.4656MHZ
13	U13	900029-001	IC 74S153 DUAL 4TO1 MULTIPLEXER
14	U14	900055-000	IC 74LS374 OCTAL D FLIP-FLOP
15	U15	900036-000	IC 74LS166 8BIT SHIFT REGISTER
16	U16	900003-004	IC 74ALS04 HEX INVERTER
17	U17	900018-001	IC 74LS74A DUAL D FLIP-FLOP
18	U18-U20	900018-002	IC 74ALS74 DUAL D FLIP-FLOP
19	U21	900064-000	IC 8021-003 ATTRIBUTES CONTROLLER
20	U22	900003-004	IC 74ALS04 HEX INVERTER
21	U23	900007-001	IC 74LS08 QUAD AND GATE
22	U24	900014-002	IC 74ALS32 QUAD OR GATE
23	U25	710003-000	DECODER MEMORY
24	U26,U27	900002-000	IC HM6116-3 2Kx8 CMOS STATIC RAM
25	U28	900018-002	IC 74ALS74 DUAL D FLIP-FLOP
26	U29	900031-001	IC 74LS157 DUAL 2TO1 MULTIPLEXER
27	U30	900046-000	IC 74LS245 OCTAL BUS TRANCEIVER
28	U31	900036-000	IC 74LS166 8BIT SHIFT REGISTER
29	U32	900014-001	IC 74LS32 QUAD OR GATE
30	U33	900014-002	IC 74ALS32 QUAD OR GATE
31	U34	900014-001	IC 74LS32 QUAD OR GATE
32	U35	900031-001	IC 74LS157 DUAL 2TO1 MULTIPLEXER
33	U36,U37	900018-001	IC 74LS74A DUAL D FLIP-FLOP
34	U38	900028-000	IC 74LS139 DUAL 2TO1 DECODER
35	U39-U42	900092-000	IC HM6116-3 2Kx8 CMOS STATIC RAM
36	U43,U44	900055-000	IC 74LS374 OCTAL D FLIP-FLOP
37	U45	900007-001	IC 74LS08 QUAD AND GATE
38	U46,U47	900045-000	IC 74LS244 OCTAL BUFFER
39	U48	900007-001	IC 74LS08 QUAD AND GATE
40	U49	900018-002	IC 74ALS74 DUAL D FLIP-FLOP
41	U50	900003-003	IC 74LS04 HEX INVERTER

42	U51,U52	900007-001	IC 74LS08 QUAD AND GATE
43	U53,U54	900018-001	IC 74LS74A DUAL D FLIP-FLOP
44	U55-U58	900092-000	IC HM6116-3 2Kx8 CMOS STATIC RAM
45	U59	900046-000	IC 74LS245 OCTAL BUS TRANCEIVER
46	U60	900048-000	IC 74LS273 OCTAL D FLIP-FLOP
47	U61	900014-001	IC 74LS332 QUAD OR GATE
48	U62	900058-000	IC 74ALS574 OCTAL D FLIP-FLOP
49	U63	900014-001	IC 74LS32 QUAD OR GATE
50	U64	900018-001	IC 74LS74A DUAL D FLIP-FLOP
51	U65	900013-001	IC 74LS30 NAND GATE
52	U66	900045-000	IC 74LS244 OCTAL BUFFER
53	U67	900007-001	IC 74LS08 QUAD AND GATE
54	U68,U69	900090-000	IC UA9636A DUAL SINGLE ENDED DRIVER
55	U70	900091-000	IC Z80A SIO SERIAL I/O CONTROLLER
55A	X70	900331-000	SOCKET IC 40 PIN
56	U71	900045-000	IC 74LS244 OCTAL BUFFER
57	U72	900046-000	IC 74LS245 DUAL BUS TRANCEIVER
58	U73,U74	900045-000	IC 74LS244 OCTAL BUFFER
59	U75	900075-000	IC CRT9007 CRT CONTROLLER
59A	X75	900331-000	SOCKET IC 40 PIN
60	U76	900060-000	IC 75175 RS422/423 BUS RECEIVER
61	U77	900030-001	IC 74LS155 DUAL 2TO4 DECODER
62	U78	900038-000	IC 74LS174 HEX D FLIP-FLOP
63	U79-U81	900045-000	IC 74LS244 OCTAL BUFFER
64	U82	900901-000	IC PAL 14L4 EXPANSION LOGIC
65	U83	900045-000	IC 74LS244 OCTAL BUFFER
66	U84	900055-000	IC 74LS374 OCTAL D FLIP-FLOP
67	U85	900046-000	IC 74LS245 OCTAL BUS TRANCEIVER
68	U86-U88	900045-000	IC 74LS244 OCTAL BUFFER
69	U89	900019-001	IC 74S86 QUAD XOR GATE
70	D1	900161-000	SEMI 1N4004 GP RECT
71	D2-D7	900147-000	SEMI 1N4148 SIGNAL DIODE
72	Q1,Q2	900174-000	SEMI 2N4208 TRANSISTOR
73	Q3	900180-000	SEMI MPS-A14 DARLINGTON TRANSISTOR
74	Q4	900174-000	SEMI 2N4208 TRANSISTOR
75	R1,R2	900190-031	RES CARBON FILM 5% 1/4W 3.3K OHMS
76	R3	900190-004	RES CARBON FILM 5% 1/4W 100 OHMS
77	R4	900190-008	RES CARBON FILM 5% 1/4W 200 OHMS
78	R5	900190-031	RES CARBON FILM 5% 1/4W 3.3K OHMS
79	R6	900190-015	RES CARBON FILM 5% 1/4W 1K OHMS
80	R7	900190-008	RES CARBON FILM 5% 1/4W 200 OHMS
81	R8,R9	900183-001	RES FIXED COMP 5% 1/4W 33 OHMS
82	R10	900190-008	RES CARBON FILM 5% 1/4W 200 OHMS
83	R11	900190-012	RES CARBON FILM 5% 1/4W 510 OHMS
84	R12	900190-010	RES CARBON FILM 5% 1/4W 470 OHMS
85	R13	900190-009	RES CARBON FILM 5% 1/4W 220 OHMS
86	R14	900190-006	RES CARBON FILM 5% 1/4W 120 OHMS
87	R15	900190-003	RES CARBON FILM 5% 1/4W 82 OHMS
88	R16	900190-007	RES CARBON FILM 5% 1/4W 150 OHMS
89	R17-R19	900190-010	RES CARBON FILM 5% 1/4W 470 OHMS

90	R20	900190-008	RES CARBON FILM 5% 1/4W 200 OHMS
91	R21,R22	900190-031	RES CARBON FILM 5% 1/4W 3.3K OHMS
92	R23,R24	900190-019	RES CARBON FILM 5% 1/4W 12K OHMS
93	R25-R27	900190-031	RES CARBON FILM 5% 1/4W 3.3K OHMS
94	R28	900190-015	RES CARBON FILM 5% 1/4W 1K OHMS
95	R29	900190-004	RES CARBON FILM 5% 1/4W 100 OHMS
96	R30	900190-008	RES CARBON FILM 5% 1/4W 200 OHMS
97	R31	900190-031	RES CARBON FILM 5% 1/4W 3.3K OHMS
98	R32	900190-021	RES CARBON FILM 5% 1/4W 47K OHMS
99	R33	900190-008	RES CARBON FILM 5% 1/4W 200 OHMS
100	R34	900190-000	RES CARBON FILM 5% 1/4W 10 OHMS
101	R35,R36	900190-030	RES CARBON FILM 5% 1/4W 750 OHMS
102	R37	900190-055	RES CARBON FILM 5% 1/4W 2.2K OHMS
103	R38	900190-031	RES CARBON FILM 5% 1/4W 3.3K OHMS
104	R39	900190-015	RES CARBON FILM 5% 1/4W 1K OHMS
105	R40	900190-008	RES CARBON FILM 5% 1/4W 220 OHMS
106	RN1	900198-000	RES DIP 8PIN 7RES 2% 0.2W 2.2K OHMS
107	RN2	900798-000	RES DIP 8PIN 4RES 0.3W 22 OHMS +/-2
108	RN3,RN4	900797-000	RES DIP 8PIN 7RES 2% 0.2W 10K OHMS
109	RN5	900198-000	RES DIP 8PIN 7RES 2% 0.2W 2.2K OHMS
110	RN6	900200-000	RES DIP 16PIN 8RES 1/4W 33 OHMS +/-2
111	RN7,RN8	900198-000	RES DIP 8PIN 7RES 2% 0.2W 2.2K OHMS
112	C1	900225-001	CAP CERAMIC 10% 100V 12PF
113	C2-C4	900811-002	CAP CERAMIC 20% 100V 0.01uF
114	C5	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
115	C6	900225-009	CAP CERAMIC 10% 100V 27PF
116	C7	900225-001	CAP CERAMIC 10% 100V 12PF
117	C8	900227-000	CAP VARIABLE 250V 2-40PF
118	C9	900213-002	CAP TANTALUM 10% 6.3V 33uF
119	C10	900224-002	CAP CERAMIC 10% 50V 0.22uF
120	C11	900214-000	CAP TANTALUM 10% 16V 33uF
121	C12	******-***	NOT USED
122	C13-C26	900811-002	CAP CERAMIC 20% 100V 0.01uF
123	C27	900856-000	CAP TANTALUM 20% 10V 22uF
124	C28,C29	900811-002	CAP CERAMIC 20% 100V 0.01uF
125	C30	900856-000	CAP TANTALUM 20% 10V 22uF
126	C31	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
127	C32	900225-009	CAP CERAMIC 10% 100V 27PF
128	C33-C36	900811-001	CAP CERAMIC 20% 100V 150PF
129	C37-C40	******-***	NOT USED
130	C41-C45	900811-001	CAP CERAMIC 20% 100V 150PF
131	C46	900225-009	CAP CERAMIC 10% 100V 27PF
132	C47	900811-002	CAP CERAMIC 20% 100V 0.01uF
133	J1	900463-000	HEADER 4 POSITION
134	J2	900464-000	RECEPTACLE "D" 50 POS FEMALE
135	J3	900465-000	RECEPTACLE "D" 25 POS FEMALE
136	J4	900466-000	CONNECTOR "D" 25 POS MALE
137	J5	900467-000	JACK PHONO
138	J6,J7	900468-000	JACK PCB MODULAR 6 POSITION
139	J8	900469-000	JACK PCB MODULAR 4 POSITION
140	J9	900471-000	HEADER W/LOCK 4 POSITION
141	P2	900470-000	HEADER INTERCONNECT 64 POSITION

142	P10	900472-000	RECEPTACLE VERTICAL MOUNT 28 POSITION
143	P11	900473-000	RECEPTACLE VERTICAL MOUNT 10 POSITION
144	E1	******-***	NOT USED
145	E2,E3	900806-000	HEADER 2PIN ASSY. SINGLE ROOW
146	E4	******-***	NOT USED
147	E5	900807-000	HEADER 3PIN ASSY. SINGLE ROW
148	K1	900240-000	RELAY PCB MOUNT SPDT 2VDC
149	Y1	900280-000	CRYSTAL 32.768KHZ MX-30 CASE
150		900808-000	JUMPER 2 CIRCUIT
151		900478-000	WIRE KYNAR 30AWG YEL

Modem Board

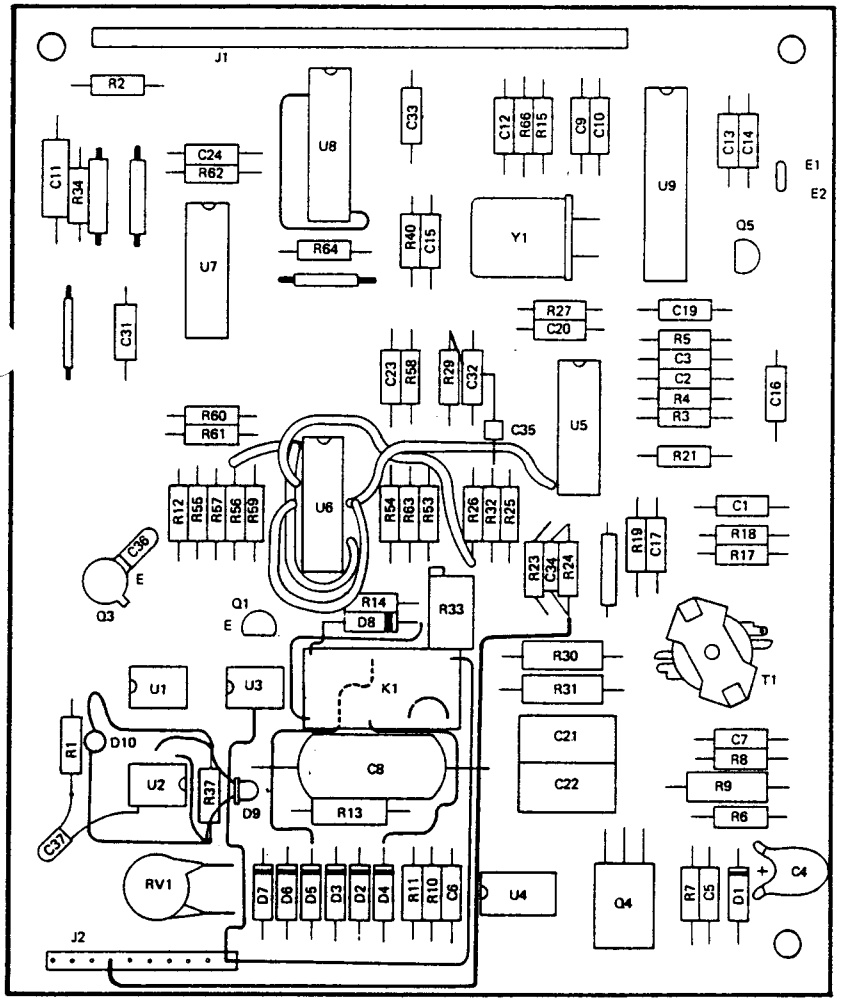


Fig. 4-3 – Modem Board

4.10 PWA Modem Board A8 Parts List Revision Level: 08

Note: This parts list is to be used for those Modem Boards Revision 05 to 08.

Item	Reference	Part Number	Description
1	U1	900083-000	IC MK5089 INTERGATED TONE DIALER
2	U2	900089-000	IC TMS99532 300 BPS FSK MODEM
3	U3,U4	900079-000	IC MC3403 QUAD DIFF INPUT OP AMP
4	U5	900081-000	IC MC14066 QUAD ANALOG MULTIPLEXER
5	U6	900824-000	SEMI 4N26 ISOLATOR OPTO COUPLER
6	U7	900177-000	SEMI 4N36 ISOLATOR OPTO COUPLER
7	U8	900824-000	SEMI 4N26 ISOLATOR OPTO COUPLER
8	U9	900077-000	IC LM358 DUAL DIFF INPUT OP AMP
9	D1,D2	900161-000	SEMI 1N4004 GP RECT
10	D3	900858-000	SEMI 1N4761 ZENER 75V 1W
11	D4-D7	900161-000	SEMI 1N4004 GP RECT
12	D8	900178-000	SEMI 1N5236B DIODE ZENER 7.5V 1/2W
13	D9,D10	900865-000	SEMI TIL38 DIODE P-N
14	Q1	900080-000	IC MC79L05ACP VOLTAGE REG -5V
15	Q2	900172-001	SEMI 2N222A TRANSISTOR
16	Q3	900180-000	SEMI MPS-A14 DARLINGTON NPN TRANSISTOR
17	Q4	900176-000	SEMI MJE340 POWER TRANSISTOR 300V 20W
18	RV1	900910-000	VARISTOR 250V RMS 200V DC
19	R2	900190-000	RES CARBON FILM 5% 1/4W 10 OHMS
20	R3,R4	******_***	NOT USED
21	R5	900190-000	RES CARBON FILM 5% 1/4W 10 OHMS
22	R6	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
23	R7	******_***	NOT USED
24	R8	900190-021	RES CARBON FILM 5% 1/4W 47K OHMS
25	R9	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
26	R10	******_***	NOT USED
27	R11	900190-040	RES CARBON FILM 5% 1/4W 10M OHMS
28	R12	900190-033	RES CARBON FILM 5% 1/4W 1.6K OHMS
29	R13,R14	900891-000	RES CARBON FILM 5% 1/2W 0 OHMS
30	R15	900190-044	RES CARBON FILM 5% 1/4W 56K OHMS
31	R16	900190-014	RES CARBON FILM 5% 1/4W 910 OHMS
32	R17	900190-021	RES CARBON FILM 5% 1/4W 47K OHMS
33	R18	900190-054	RES CARBON FILM 5% 1/4W 27K OHMS
34	R19	900190-021	RES CARBON FILM 5% 1/4W 47K OHMS
35	R20	900190-024	RES CARBON FILM 5% 1/4W 200K OHMS
36	R21	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
37	R22	900190-020	RES CARBON FILM 5% 1/4W 15K OHMS
38	R23	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
39	R24	900189-000	RES METAL FILM 2% 1/4W 39K OHMS
40	R25	900189-001	RES METAL FILM 2% 1/4W 47K OHMS
41	R26	900190-035	RES CARBON FILM 5% 1/4W 18K OHMS
42	R27	900190-036	RES CARBON FILM 5% 1/4W 20KK OHMS
43	R28	******_***	NOT USED

44	R29	900190-017	RES CARBON FILM 5% 1/4W 8.2K OHMS
45	R30	900190-044	RES CARBON FILM 5% 1/4W 56K OHMS
46	R31	900190-024	RES CARBON FILM 5% 1/4W 200K OHMS
47	R32-R34	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
48	R35	900190-053	RES CARBON FILM 5% 1/4W 24K OHMS
49	R36	900190-044	RES CARBON FILM 5% 1/4W 56K OHMS
50	R37	******-***	NOT USED
51	R38,R39	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
52	R40	900190-044	RES CARBON FILM 5% 1/4W 56K OHMS
53	R41	900190-017	RES CARBON FILM 5% 1/4W 8.2K OHMS
54	R42	900190-052	RES CARBON FILM 5% 1/4W 300K OHMS
55	R43	900190-023	RES CARBON FILM 5% 1/4W 160K OHMS
56	R44	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
57	R45	900819-000	RES CARBON FILM 5% 1/4W 0 OHMS
58	R46	900190-021	RES CARBON FILM 5% 1/4W 47K OHMS
59	R47	900190-044	RES CARBON FILM 5% 1/4W 56K OHMS
60	R48	900190-045	RES CARBON FILM 5% 1/4W 82K OHMS
61	R49	900190-046	RES CARBON FILM 5% 1/4W 150K OHMS
62	R50	******-***	NOT USED
63	R51	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
64	R52	900195-000	RES VARIABLE 10% 1/2W 2K OHMS
65	R53,R54	900184-005	RES FIXED COMP 5% 1/2W 300K OHMS
66	R55	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
67	R56,R57	******-***	NOT USED
68	R58	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
69	R59	900190-001	RES CARBON FILM 5% 1/4W 620 OHMS
70	R60	900190-025	RES CARBON FILM 5% 1/4W 2M OHMS
71	R61	900191-000	RES CARBON FILM 5% 1/4W 470 OHMS
72	R62	900190-000	RES CARBON FILM 5% 1/4W 10 OHMS
73	R63	900190-012	RES CARRBON FILM 5% 1/4W 510 OHMS
74	R64	900190-041	RES CARBON FILM 5% 1/4W 120K OHMS
75	C1	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
76	C2	900224-002	CAP CERAMIC 10% 0.22uF
77	C3	******-***	NOT USED
78	C4,C5	900225-002	CAP CERAMIC 10% 100V 22PF
79	C6,C7	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
80	C8	900224-002	CAP CERAMIC 10% 50V 0.22uF
81	C9	900224-004	CAP CERAMIC 10% 50V 820PF
82	C10,C11	******-***	NOT USED
83	C12	900225-007	CAP CERAMIC 10% 100V 0.047uF
84	C13,C14	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
85	C15	900224-004	CAP CERAMIC 10% 50V 820PF
86	C16,C17	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
87	C18	900224-004	CAP CERAMIC 10% 50V 820PF
88	C19-C23	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
89	C24,C25	900225-002	CAP CERAMIC 10% 100V 22PF
90	C26	******-***	NOT USED
91	C27	900224-004	CAP CERAMIC 10% 50V 820PF
92	C28	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
93	C29	900220-002	CAP METAL FILM 10% 250V 0.47uF

94	C30,C31	900220-001	CAP METAL FILM 10% 250V 0.1uF
95	C32	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
96	C33	900224-005	CAP CERAMIC 10% 50V 3300PF
97	C34	900215-001	CAP TANTALUM 10% 35V 4.7uF
98	C35	900221-000	CAP CERAMIC +80/-20% 50V 0.1uF
99	C36	900213-000	CAP TANTALUM 10% 6.3V 4.7uF
100	C37	900213-002	CAP TANTALUM 10% 6.3V 33uF
101	J1	900462-000	HEADER ASSY UNSHROUDED 28 POSITION
102	J2	900461-000	HEADER ASSY UNSHROUDED 10 POSITION
103	TI	520004-000	TRANSFORMER 600/600 OHMS RM5 CORE AUDIO
104	Y1	900279-000	CRYSTAL 4.032MHZ PRL RES H3WHC18.U1
105	K1	900855-000	RELAY PCB MOUNT DPDT 5VDC
106		900492-000	WIRE SOLID BUS 24AWG
107		900874-000	BUMPER MOULDED

4.11 CRT Parts List

Item	Reference	Part Number	Description and Phillips Part Number
1		900990-000	CRT TUBE
2		900991-000	CRT MONITOR BOARD
3	R27	900992-000	RES VARIABLE 20% 0.2W 10K OHMS (2122 377 00012)
4	R30	900191-004	RES CARBON FILM 5% 1/2W 3.9K OHMS
5	R37	900190-018	RES CARBON FILM 5% 1/4W 10K OHMS
6	R46	900992-000	RES VARIABLE 20% 0.2W 10K OHMS (2122 377 00012)
7	R49	900992-001	RES VARIABLE 20% 0.2W 470 OHMS (2122 377 00025)
8	R53	900992-000	RES VARIABLE 20% 0.2W 10K OHMS (2122 377 00012)
9	R94,R95	900993-000	RES VARIABLE 30% 0.2W 2M2 OHMS (2122 377 00026)
10	R110	900993-001	RES VARIABLE 30% 0.2W 22K OHMS (2122 377 00022)
11	CR85	900994-000	DIODE 1N914
12	F1	900995-000	PICO FUSE, SUBMINIATURE 2.5A
13	L51	900996-000	HORIZONTAL LINEARITY COIL ADJUSTABLE (5107 140 00451)
14	L52	900997-000	HORIZONTAL WIDTH COIL (5107 140 00151)
15	Q56	900998-000	BU407 (9332 883 00682)

4.12 Disk Drive Parts List

Item	Reference	Part Number	Description
1		900880-000	EJECTOR
2		900887-000	EJECTOR SPRING
3		900881-000	FRONT BEZEL/CLUTCH ASSY
4		900879-000	LED, WRITE CONTROL
5		900886-000	LOAD ARM/MEDIA GUIDE ASSY
6		900884-000	PHOTOTRANSISTOR, WRITE CONTROL
7		900878-000	PRINTED CIRCUIT CARD, CONTROL
8		900877-000	PRINTED CIRCUIT CARD, JAPAN SERVO
9		901000-000	TRACK 00 OPTO SWITCH
10		900883-000	BAND ASSY
11		900876-000	HEAD CARRIAGE ASSY
12		900999-000	SPRING, COMPRESSION CLUTCH
13		900879-000	LED,INDEX
14		900884-000	PHOTOTRANSISTOR, INDEX
15		900982-000	SPRING,STEPPER MOTOR ADJUST
16		900882-000	STEP MOTOR ASSY
17	L1	900983-000	CHOKE 33uH
18	L2,L3	900983-001	CHOKE 82uH
19	L4,L5	900983-002	CHOKE 330uH
20	L6-L8	900983-003	CHOKE 150uH
21	8B	900984-000	IC 1CL7660
22	7D	900985-000	IC DG211
23	Z1	900986-000	IC HA11714
24	Z2	900987-000	IC HA11715
25	Z3	900988-000	IC uPC1043C
26	VR1,VR2	900989-000	DIODE, ZENER RD2.2EC

5.1 System Board

General

The System Board contains the Keyboard Interface, the System Clock, CPU (and co-processor if installed), Priority Interupt Controller (PIC), I/O Wait State Generator, Bus Arbiter and Bus Controller, Floppy Disk Controller and associated Read/Write and Drive Control Circuits, Address Demultiplexer, Buffers, Parity Generator and Checker, BIOS EPROM, and the Dynamic RAM with Memory Addressing as well as Timer and Speaker Circuits.

NOTE : These circuit descriptions refer to REV 06 system boards (REV 04 Hyperions).
: A (/) in front of a signal indicates the signal is active low.

Keyboard Interface

The Keyboard sends serial data LSB first at the rate of 300 baud. The data is inverted (U89-2), to obtain an active high start bit, and shifted into shift register (U96), on the eighth rising edge the high appears at U96-12. The ninth rising edge clocks the high from U96-12 to flip-flop U29, its high output (5) inhibits the shift register and sends an interrupt request to the PIC (U43-19). The low output pulls the KBCLK line low and the keyboard stops sending. Once the processor reads the character stored in the shift register, it initiates, via PAL U23-16, a write operation to the keyboard port. If DB7 (U96-4) is low, it is clocked into U28-2 by /WRTKBREG. The low appears at pin 5, enabling U30, causing U54-1 to go low resulting in a /KBRST. The keyboard reset is cleared by writing 80H to the keyboard port.

System Clock

The System Clock generation is performed by a clock generator chip (U83) driven by a 14.318 Mhz crystal which is divided by three in the clock generator to provide a 4.77Mhz clock rate with a 33% duty cycle. The clock generator is configured to use asynchronous ready inputs (U83-15 tied low).

5.0 Technical Reference

On Power up, a /RES signal is applied to the clock generator (U83-11), resulting in a RESET signal (83-10). This reset signal is applied directly to the processor. It is also inverted and RESET and /RESET are used throughout the System to set, reset and preset various devices.

RDY1 (U83-4), (derived from /WAIT U86-6 and IOCRDY U5-5) and /AEN (U83-3) (derived from /IORDY U45-9) are sampled by the clock generator. If RDY1 goes low or /AEN goes high, READY (U83-5) goes low on the next negative going clock pulse, signalling the processor that an unready condition exists. The READY signal lasts for at least one MCLK cycle.

Processor

The CPU (U41) is an Intel 8088 configured for maximum mode (pin 33 tied low). In this configuration the CPU supplies status data on three lines, /S0 to /S2, rather than supplying fully decoded control lines. In this way a coprocessor (U42), which can share the Bus Controller and certain I/O lines, may be added to increase the system mathematical capabilities. The Bus Controller (U18) interprets the condition of the status lines (which are active low) and generates the appropriate command and control signals.

Status Line			Control Signal
S0	**S1**	**S2**	
0	0	0	INTERRUPT ACKNOWLEDGE
0	0	1	READ I/O PORT
0	1	0	WRITE I/O PORT
0	1	1	HALT
1	0	0	CODE ACCESS (INSTRUCTION FETCH)
1	0	1	READ MEMORY
1	1	0	WRITE MEMORY
1	1	1	PASSIVE; NO BUS CYCLE

Three tri-state latches U19, U20, and U21 demultiplex the address bus. Address information is latched in on the low going edge of ALE (U18-5). The latches go to the tri-state condition (OFF) only when /AEN (U87-8) is high during a DMA transfer.

When both processors are installed, local bus arbitration uses a request/grant protocal. The co-processor initiates a request by sending /RQ/GTO (U42-31) to the processor. On a passive cycle the processor will respond with a /RQ/GTO (U41-31) indicating that it will enter a "hold acknowledge" state at the end of the next clock cycle, thus giving the co-processor control of the bus. When the co-processor has finished its task, it sends an /RQ/GTO to the processor which indicates the "hold request" is about to end. The processor may then take control of the bus at the next clock cycle.

Reset Circuit

On power up, the system reset circuit provides an initialization signal to the System Board.

While the +5v is building up to approximately 4.6v, zener diode D4, is non-conducting and the voltage drop across R32 is insufficient to forward bias Q4, thus the collector of Q4 and base of Q3 are at VCC. This causes Q3 to conduct heavily, keeping its collector voltage at about 0.2v. Capacitor C65 is effectively short circuited.

When the +5v supply exceeds the D4 breakdown point, Q4 is biased ON and its collector voltage drops to about 0.2V, cutting off Q3.

The collector of Q3 goes to VCC and capacitor C65 starts to charge at an exponential rate set by R28. The signal /RES stays below 1.5v for 70us after VCC rises to 4.5v.

Priority Interrupt Controller

The 8088 CPU supports nine interrupt vectors. One, NMI, is nonmaskable for signalling parity errors or CRT interrupts (for vertical retrace). The other eight are programmable using the Priority Interrupt Controller (PIC) U43. Its registers may be written to or read from the CPU.

On a write operation, the CPU causes the assertion of /IOWC on U43-2 and /CSPIC on U43-1. The CPU then outputs the data to the local bus and the PIC accepts it.

When the PIC detects an active input (IR0-IR7) from a device indicating a request for service, the PIC sends an INT (U43-17) to the CPU. The CPU places /S0-S2 to the interrupt

acknowledge state (000), causing the Bus Controller (U18) to send an /INTA to the PIC, which generates a /SP/EN (U43-16) to disable the data buffer U66. The PIC then sends the interrupt information to the CPU on data bus AD0-7.

When the transfer is complete /INTA and /SP/EN are released and the data buffer is re-enabled.

Wait State Generator

The Wait State Generator is used to allow the Hyperion processor(s) to handle slow peripherals. It is reset on power-up. Both the CPU and Direct Memory Access Controller (U47) generate a wait state for all I/O activities.

Two wait states are used on all CPU initiated I/O accesses, and one wait state is asserted on all DMAC accesses. Wait states are also generated by the Display and I/O Board for all accesses to either the CRT memory or expansion bus peripheral initiated wait states.

CPU Wait States

When either /IORC (U18-13) or /IOWC (18-12) go low, a positive going edge at U44-8 clocks U45 producing IORDY. IORDY is synchronized by the Clock Generator U83-3. Because IORDY is high, /RDY (U83-5) is sent to the processors on the next negative clock edge. When the MCLK edge rises, the high at U45-9 is clocked into U67-12 and U67-8 goes low, clearing U45. On the next negative going clock edge, RDY is sent to the processors and normal operation resumes.

DMA Wait States

Wait states extend the memory read and write pulses from the DMAC (U47). The DMAC may be programmed for normal write or extended write. The normal write is selected by having /IOWC (U18-12) active 1 DMA clock period after /MEMR (U18-7) goes active. The extended write feature is selected by having /MEMR (U18-7) and /IOWC (U18-12) active at the same time.

When either /IORC (U18-13) or /IOWC (U18-12) are low, U45-8 goes low. This is asserted as a "not ready" condition at U47-6. On the next rising MCLK edge, U67-8 goes low, clearing U45 and U45-8 goes high. On the following rising clock edge U67-8 goes high, asserting a ready condition at the DMAC (U47-6).

However, if data transfers are occurring to or from DMA Channel 0 (DREQ 0), /DACK0 (U47-25) is inverted in U87 and asserted as a READY at the DMAC thus inhibiting the wait state.

Memory and Device Decoders

Three programmable array logic (PAL) devices decode the Memory, Support and peripheral device addresses.

PAL	Interpret	Generate
U22	Address lines BA15 to BA19, /MEMR and /MEMW.	Memory chip device selects and control signals
U23 and U24	Address lines BA3 to BA9, /IORC, /IOWC and AEN.	I/O device chip selects

Table 1: Address Decoder Functions

Device	Address range for up to Rev4 machine	Address range for Rev5 machine
DMA Controller	0-F	0-F
DMA Page Register	10-17	80-83
PIC	18-1F	20-3F
Interval Timer	20-27	40-5F
FDC	28-2F	C0-C7
Control Register	30-37	C8-CF
Keyboard Port	38-3F	E0-EF
Status Register	40-47	61
Volume Control Reg	48-4F	61
Serial I/O Port	100-10F	100-10F
Parallel I/O Port	140-14F	140-14F
Parallel Printer Port	150-15F	378-37F
CRT Controller	180-1FF	180-1FF

Table 2: I/0 Map

Device	Address Range
R/W Memory	00000-3FFFF
Reserved	40000-7FFFF
CRT Mode Memory	A0000-AFFFF
CRT Memory	B0000-BFFFF
Boot EPROM	F8000-FFFFF

Table 3: Memory Map

EPROM

The EPROM (U48) installed is a 2764-3. When stable address information is on the system address bus, the CPU requests a Memory Read (/S0 – /S2 = 101) to the Bus Controller which outputs /MEMR to PAL U22-8 causing U22-18 to go low placing an active low on U48-20 (/CS) and U48-22 (/OE) and the EPROM outputs its data to the CPU. The cycle is terminated when /MEMR goes high.

System Bus Arbiter

The System Bus Arbiter allocates use of the system bus to the CPU and the DMAC. If the DMAC requires the bus to carry out a requested transfer, HRQ is output at U47-10. Acknowledgement of the request is denied if:

— The CPU has initiated a bus cycle (either S0, 1, 2 low).

— An interrupt acknowledge is in progress (S0-2 low).

— A locked instruction is in progress (LOCK low).

If all of NAND U65 inputs are high, U65-8 is low. The Phase Generator (U85) samples U65-8 on the rising edge of MCLK (U85-9). On the next rising edge of MCLK, U67-5 goes high indicating to the DMAC that its request for mastery of the bus has been acknowledged. The low at U67-6 holds the flip-flop in RESET for the duration of the transfer.

The high at U67-5 is also applied to U85-5 and on the next rising clock edge, U85-6 goes low, sending /WAIT to indicate a "not ready" condition to the CPU and /AEN to disable the CPU

address demultiplexers (U19, 20, and 21) and /AEN to the Bus Controller (U18) causing its I/O Command lines to go to tri-state condition. In the next time, U85-10 goes high on the rising edge of MCLK. If either U85-7 or U85-10 are high, U92-4 is low, enabling the DMA Page Register U49 and the address bus. The DMAC is the bus master and will control the bus until the transfer is completed, at which time U47-10 goes low (HRQ is released) clearing U67-5. HOLDA (U47-7) is released and U85-7 going low forces U92-4 high disabling the DMA page register and the DMA address buffer.

The low at U85-7 appears at U85-10 on the next rising MCLK edge. U85-6 and U85-11 are ANDed (U86) producing AEN and /AEN, enabling the Bus Controller I/O command and control lines. The CPU address demuxers are also enabled.

U85-14 goes high forcing /WAIT (U86-6) high, thereby releasing "not ready" condition at the Clock Generator U83-3. This results in a READY signal to the CPU and the CPU now becomes the Bus Master.

Direct Memory Access

The DMAC (U47) operates in either the slave or master mode. In slave mode the DMAC has no active requests pending but may be programmed by the CPU.

If an active request is received at DREQ0-3 of an enabled channel, DMAC will send an "hold request" (U47-10), and control of the system bus will be transfered as detailed under System Bus Arbiter. While HOLDA is high at U47-7, the DMAC places DB0-7 onto the data bus. The information is latched into address buffer U69 by ADSTB (U47-8). Both U69 and the Page Register (U49) are enabled by the low at U92-4 and data is transfered from the I/O device to memory (/IORC and /MEMW active at the same time) or from memory to the I/O device (/IOWC and /MEMR both active).

Termination of the DMA cycle occurs when the DMAC releases the hold request (HRQ goes low) and the CPU regains bus control as detailed under System Bus Arbiter.

The DMAC requires a 50% clock cycle. This is achieved by ORing MCLK which is 33% with the output of Flip-Flop U45-5. The data input (U45-2) is MCLK and is clocked by OSC. The output when ORed with MCLK produces a 50% clock to drive the DMAC.

DMA Page Register

The DMA Page Register (U49) is a 4 bit by 4 page register file which expands the DMAC address word to 20 bits. It is a non-incrementing register, therefore transfer across a 64K byte boundry are not possible.

Page selection is achieved by decoding the state of /DACK2 (U47-14) and /DACK3 (U47-15).

Active Request	DACK2	DACK3	Page Selected
1	1	1	3
2	0	1	1
3	1	0	2

Page 0 is never accessed because /DACK2 and /DACK 3 are never active low simultaneously. The contents of the page selected form the four most significant bits (MSB) of the address during DMA transfer.

Dynamic Random Access Memory

The System Board contains 256K of dynamic random access memory (DRAM), consisting of 64K by 1 memory devices organized as a 256K by 9 array. Address multiplexing, refresh address counting and RAS/CAS generation are performed by the Dynamic Memory Controller (DMC) (U55).

Addressing

The bus master initiates a memory access cycle when U22-1 (BA19) and U22-2 (BA18) and either /MEMR (U22-8) or /MEMW (U22-9) are low. This causes U22-17 to output /RAMENB and the DMC uses the address information on address lines BA0-17 to select the memory location. Row addresses are multiplexed from BA0-7, while column addresses are multiplexed from BA8-15. RAS (range) decoding is derived from BA16 & BA17 as shown.

BA16	BA17	RAS	Address Range (HEX)
0	0	0	00000 to 0FFFF
1	0	1	10000 to 1FFFF
0	1	2	20000 to 2FFFF
1	1	3	30000 to 3FFFF

DRAM Write

If the memory access cycle was initiated by an active /MEMW, the write strobe generator (U31) and data buffer U97 are enabled. The next negative going MCLK edge causes a /WE at U31-9. The negative going edge of /WE latches data into the selected byte of memory.

When the write is completed, the CPU releases /MEMW, the write strobe generator is toggled to preset and the data buffer is tri-stated. The write cycle is terminated by the release of /RAS and /CAS.

DRAM Read

If the memory access cycle was initiated by an active /MEMR, the DRAM data buffer (U98) is enabled and when the address selection is completed /CAS is asserted, the selected memory output drivers transmit the information onto the data bus.

At the completion of the transfer /MEMR goes high, disabling the data buffer U98. /RAS and /CAS are released to disable the memory output drivers.

Parity Generation and Checking

Each DRAM write operation requires parity generation and during each DRAM read operation, parity is checked.

The parity generator/checker (U95), is wired for even mark parity. It is cleared on power up and reset. When /MEMW is asserted it causes a low at U54-8, and U95-4. The data on the bus is sampled and if there are an odd number of "1"s a 1 is asserted at U95-5. If there are an even number of "1"s a 0 is asserted. As /WE (U31-9) goes low this parity bit is latched into memory as the MSB of the data being transfered.

During a read cycle, the data is sampled by U95 and if there are an even number of "1"s normal operation continues. If there are an odd number of "1"s, U95-5 goes high, and when /CSRAM and /MEMR are released at the end of the read cycle, U29-9 goes high sending a Non-Maskable Interrupt (NMI) to the CPU. The status of U29-9 can be read under software control by sampling U30-8, and a parity error cleared under software control by U54-11.

Refresh

Refresh is required to ensure that information stored in RAM is not lost or changed due to "leakage". In the Hyperion,refresh is arranged so that either 128 row or 256 row DRAM devices may be used.

The refresh timer U94 generates a rising edge at U94-10 every 14usec causing U31-6 to go high. This initiates a request for DMA transfer via DMAC Channel 0. Once the DMAC becomes the bus master /DACK0 is asserted, resetting U31. /RFSH (U55-25) and /RASI (U55-3) are low, multiplexing the refresh counter onto the DRAM address bus (U55-00 to 07) and RAS0-3 strobe the refresh counter address into the four banks of memory. At the end of the refresh cycle /DACK0, /RFSH and /RASI are released. The rising edge of /RFSH increments the refresh counter by one in preparation for the next cycle.

During refresh cycles U55-6 (/CAS) is held high, and the data buffers U97 and U98 and the parity generator/checker U95 are inhibited.

Floppy Disk Controller

The Floppy Disk Controller (FDC) (U50) provides an interface between the CPU and the Disk Drives. The Hyperion can support two floppy drives.

Drive Control Interface

The drive control interface at the output of the FDC is a multiplexed active high. The disk drive requires a demultiplexed active low. Demultiplexing is performed by the output of U50-39 (RW/SEEK). Drive selection is made by U8-4 and U8-12, based on the contents of the status register (U93).

During a diskette read or write cycle, U50-39 goes low ensuring STEP (53-11) and FAULT (U50-33) are inactive. In addition, U50-34 is low, disabling Write Protect (WP) unless WRITE PROTECT is high at U7-12 which will be asserted by U46-3 to U50-34.

In the seek mode, U50-39 goes high, WRITE PROTECT will appear at U50-34 and if TRK000 is low, a fault signal will appear at U50-33. If U50-37 is also high, STEP appears at J1-20.

FDC Write

Data to be written to the disk drive is converted from parallel to serial format. Precompensation of 125nsec limits the degree of bit shift.

The FDC base clock frequency of 8Mhz is generated by U27 and appears divided by 2 at U70-6. The 4Mhz signal increments the write clock generator (U71) until a count of OFH is reached, at which time the carry out at U71-15 goes high, resetting the generator to its preprogrammed 08H start point and counting continues. The carry out is propogated via U70-12 (to ensure that no switching errors occur) to the FDC WR CLK (U50-21). The signals WRDATA (U50-30), PSO (U50-32) and PSI (U50-31) are synchronous with U50-21.

Precompensation Logic

During the time that WRDATA is low, U52-9 (ST/LD) is high. On the rising edge of the 8Mhz clock, data is loaded into U52-4, 5, 6, 7. When WRDATA goes high, the data is shifted through U52. As a low appears at U52-11, U51 is cleared, U51-6 goes low and WRITE DATA is asserted at U26-6. On the following 8Mhz rising edge, clocking of U51 is inhibited, (U51-4 is low), but U52-11 goes high. U51-6 continues to inhibit U26. The next rising clock edge clocks a high out U51-6, releasing U26-6.

FDC Host Interface

The host interface is configured to allow either a DMA mode of operation or host direct access to the FDC.

The DMA mode may occur when:

1) The FDC requires data from the host memory during a diskette write operation.

2) The FDC requires to store data in the host memory during a diskette read operation.

A DMA transfer is initiated by the FDC asserting DRQ at U50-14, and following a 2usec delay, caused by DRQ propagation through (U72), DREQ1 appears at U72-15 and at the DMAC (U47-18). The DMAC (U47) generates a request for bus mastery. When it becomes bus master the DMAC transmits /DACK1 clearing the request at U72-15.

The host performs direct access to the FDC when it is required that the FDC perform a specific command or when status information is to be read.

Host to FDC

To complete a transfer of information from host memory to the FDC, the DMAC sends /DACK1 to U72 clearing the request, then /MEMR (U47-3) and /IOWC (U47-2) are asserted. The data at the output of read buffer (U98) is valid (for 294nsec max), and it is latched into the FDC on the rising edge of /IOWC, thus ending the memory to FDC cycle. The DMAC releases HRQ and control of the bus is passed back to the CPU. This process continues until the byte count of the DMAC reaches 0. /EOP (U47-36) goes low causing TC (U87-10) to be propagated via U26-11 to the FDC at U50-16.

FDC To Host

To complete a transfer from FDC to host memory, the DMAC sends /DACK1 to U72 clearing the request, then /MEMW (U74-4) and /IORC (U47-1) are asserted. The data at the output of the FDC (D0-D7) is strobed into memory on the negative going edge of /CAS. The DMAC releases HRQ (U47-10) and control of the bus is passed back to the CPU. The process continues until the byte count of the DMAC reaches 0. /EOP (U47-36) going low causes TC to be propagated via U26-11 to the FDC at U50-16.

Timer

The 8253A-5 programmable timer (U94) provides:

OUTPUT 0	DRAM refresh timing with a rising edge every 14usec.
OUTPUT 1	Generates baud rate frequencies for the SIO on the Display and I/O board.
OUTPUT 2	MODE 1: Generates tones for the speaker. MODE 2: Generates timed interrupts to the CPU.

Control Register

The Control Register is a 4 bit write only register, (U93).

BIT 0	0 = Deselects drive A 1 = Selects drive A
BIT 1	0 = Deselects drive B 1 = Selects drive B
BIT 2	0 = Inhibits parity 1 = Select parity
BIT 3	0 = Reset FDC 1 = Enable FDC

Status Register

The Status Register is a 5 bit read only memory. It consists of U88, and 1/4 of U30.

BIT 0 (U88-11)	0 = Drive A selected 1 = Drive A deselected
BIT 1 (U88-8)	0 = Drive B selected 1 = Drive B deselected
BITS 2,3,4	NOT USED
BIT 5 (U88-3)	RESERVED

BIT 6 (U88-6)	RESERVED
BIT 7 (U30-8)	0 = No parity error 1 = Parity error occured

Volume Control Register

The volume control register is a one bit write only register.

BIT 0	0 = speaker enabled 1 = speaker disabled

The volume control register is a two bit write only register used to control the speaker output.

BIT 0	0 = Disables gate input of timer 2 1 = Enables gate input of timer 2
BIT 1	0 = Disables speaker data output 1 = Enables speaker data output

5.2 Display and I/O Board

The Display and I/O Board contains the CRT control logic, Parallel Printer Port, Serial Port, Parallel I/O Expansion Port, Real Time Clock, and Connections to the optional Modem Board.

Note: : These circuit descriptions refer to REV 04 Display and I/O Boards (REV 04 Hyperions.)
: A(/) in front of a signal indicates the signal is active low.

CRT Control Logic

The CRT Control Logic is based around the CRT9007 LSI Controller chip. This chip accesses information in the CRT memory, provides timing signals for the generation of dot-matrix characters, synchronizes the CRT monitor raster and is capable of interupting the CPU. The Video display circuitry consists of an LSI CRT controller chip (CRT9007) (U75), 20K bytes (10K words) of 2K × 8 CMOS static Ram (character or graphics memory), (U26, U27, U39-U42, U55-U58), EPROM character generator (U3), Attributes circuitry, and Low and High resolution graphics circuitry.

The CRT9007 accesses 16 bits of memory data either as character/attributes information or graphics video. The character/attributes information is passed to the attributes logic and the attributes controller (U21), as well as the character generator (U3). The character generator produces dot level video which is modified and serialized by the attributes controller. The graphics information is serialized into two parallel bit streams for low resolution graphics or multiplexed into a single bit stream for high resolution graphics.

The circuit can be programmed to operate in one of several modes

1) 40 by 25 character alphanumeric:
The screen contains a page of alphanumeric characters arranged in 25 rows of 40 characters.

2) 80 by 25 character alphanumeric:
The screen contains a page of alphanumeric characters arranged in 25 rows of 80 characters.

3) 320 by 250 pixel graphics:
Each pair of bits in memory (0 and 1, 2 and 3, 4 and 5, 6 and 7) is displayed on the screen as one picture element. The screen contains 320 pixels per scan line and has a total of 250 scan lines per raster.
Each pixel can have one of four states:
0,0 = black
0,1 = dark grey
1,0 = light grey
1,1 = white

4) 640 by 250 pixel graphics:
Each bit in memory appears as a pixel, which can only be on or off. There are no grey states available.

5) 320 by 200 graphics:
Uses only 200 raster lines and 16k of memory.

6) 640 by 200 graphics:
Uses only 200 raster lines and 16k of memory.

7) Row Table Mode
In each of the above modes the memory is accessed by the CRT9007 sequentially, i.e. the data appears from the lowest address to the highest on the page. In Row Table Mode the memory is accessed during non-display intervals in order to fetch the address of the next row of characters to be displayed. The address of each of 25 displayable rows is contained in a table which can modified by editing the table.

The end result of the CRT control logic is a set of signals: Vertical Sync, Horizontal Sync, Video Out and Composite Video Out. The sync signals are produced by the CRT9007 and along with the video output are used to drive the CRT monitor board. The composite video signal is a combination of those signals and appears at an RCA-type phono socket.

Timing Generation

DOTCLK

The functions of the display circuitry are all synchronized to the CRT raster timing which is derived from the Master Clock 12.4656MHZ (U12). This signal is divided down to 6.2328MHZ

by U28. U28-8 is fed to multiplexer U13-3 & 4 and the 12MHZ signal is fed to U13-5 & 6. The output U13-7 is switchable from 6 to 12 MHZ by the B select (U13-2), (Control Bit 4), and is called DOTCLK. In the 80 character mode, and high resolution graphics, 12MHZ DOTCLK is used, for all other modes, including low resolution graphics, 6MHZ DOTCLK is used.

Phase Generator

DOTCLK clocks the phase generator (U62-11), an 8 bit SIPO type shift register. The first 7 outputs are wired into U65. Its output, pin 8, feeds the serial input of the shift register (U62-2). The input is high until all 7 bits are shifted in, U65-8 goes low and is shifted into the register. The outputs of the register (BDC1-8) are fed through 33 ohm resistors, and are called DC1-8. The period of each is the same as the character clock or one eighth of DOTCLK.

/VIDCYC

The two types of memory cycle (CRT 9007 and CPU) may both take place within one cycle of the phase generator. Each are allowed non overlapping time slots /VIDCYC and /CPCYC.

/VIDCYC is produced at U20-5, which has a logic 0 at pin 2 clocked in by the rising edge of DC4. This stays low until the flip-flop is set (U20-4) by DC8 (U33-1) and DOTCLK (U33-2) being low simultaneously.

/CPCYC

/CPCYC is produced at U20-9, which has a logic 0 at pin 12 clocked in by the rising edge of DC8. The low at pin 12 is produced by ORing /XCRTCSI (U33-10) and the cycle enabling signal (U33-9). This stays low until the flip-flop is set (U20-10) by DC4 (U33-12) and DOTCLK (U33-13) being low simultaneously.

The two sets of signals, /VIDCYC and /CPCYC, are used to enable the two sets of address buffers (U73 and U74, U80 and U81).

/CCLK

The clock for the CRT9007 is produced at U8-6. It is set low in the middle of DC8 low time from U33-3. At the trailing edge of DC1 it is clocked high.

8088 Write Cycle Timing

/XMEMW and /CPCYC gated through U34, cause U18-2 to be low. This signal is clocked either by the trailing (rising) edge of DC1, or in the middle of DC1 time, (depending on the position of jumper E1) producing /MW at pin 5. /MW ends when the falling edge of DC4 resets U18. The low at U18-12 is clocked in when U9-10 goes high (middle of DC2 low time) producing /MWE at U18-9. /MWE ends simultaneously with /CPCYC when U33-11 presets U18-10 and U20-10.

CRT9007 Bus Interface

Address Bus Buffers

The CRT9007 address lines VA0-13 are buffered by U73 and U74 before driving memory address lines (MA0-13). The buffers are enabled by /VIDCYC.

Row Table Buffer

Because the CRT9007 cannot write to memory there are no data buffers required, however under Row Table Mode, it reads memory and uses the information to point to the next row of characters. The Controller can only read 8 bit bytes even though it accesses a 16 bit byte, the byte used is from the even bank of memory. CC0-7 are used in Row Table Mode and are clocked into U44 by /VIDCYC (U44-11). The outputs of U44 (LCC0-7) are buffered by the Row Table Buffer U47 and drive the Controller data lines VD0-7. U47 is enabled when VIDCYC (U20-6) is low, INT (U57-27) is low and CB0 (U60-2) is high.

8088 Bus Interface

The CPU may read or write a byte of memory, if the CRT9007 is not accessing it. CPU accesses are synchronized to the character clock. When a CPU cycle to the CRT memory starts, "CRT IOCHRYD" line to the CPU is held inactive until the CRT9007 is finished its cycle. This causes the CPU to enter its "WAIT STATE" until CRT IOCHRDY is activated. Thus the CPU cycles to the CRT memory are longer than normal memory cycles.

Address Buffers

The external address bus signals, XBA0-14, are buffered by U80 and U81, the outputs corresponding to XBA1-14 drive memory address bus lines, MA0-13, during CPU accesses. This bus is also driven by the CRT9007 address buffers, (U73 and U74) but the two sets of buffers are never enabled at the same time. U80 and U81 are enabled by /CPCYC while U73 and U74 are enabled by /VIDCYC. The output corresponding to XBA0 (U80-18) is not used. XBA0 is inverted at U86-8 and used to select between odd or even bytes of the 16-bit memory word. The even byte is the character code and the odd byte is the attribute associated with that character.

The lines XBA0-5 are also buffered by U79, in order to drive the CRT9007 address lines during access to its internal registers. The controllers address lines must be tri-stated during such access, so the signal which enables these buffers /XCRTCS0, also drives the /TSC input of the controller, pin 33, causing it to tri-state its drivers.

Data Buffers

The external data bus lines, XDB0-7, are buffered by U59 when accesses are to the CRT9007 or the control register U60 and by U43 and U46 when accesses are to memory.

U59 direction control (pin 1) is driven by AND gate U23, whose output is low for either a memory write cycle (/XMEMW) or an I/O write cycle (/XIOWC). Data flow is from B to A for a write cycle or from A to B the rest of the time. The device is enabled (pin 19) by OR gate U61, which is active low for any of the four types of cycles (/XMEMW, /XIOWC, /XMEMR, /XIORC), but

only if one of /XCRTSC0 or /XCRTCS2 is active. U59 will respond for accesses both to the CRT9007, which is I/O mapped, and to the control register U60, which is memory mapped. U60 is cleared by the inverted XRESET at (U5) and is clocked by the rising edge of its chip select, /CREGCS. Its ouptuts, CB0-7, control the various mode settings for the hardware.

Memory data buffers U43 (latch) and U46 (bus buffer) serve together as a latching transceiver. In a read cycle, the latch is clocked by /CPCYC. The data read from memory (CC0-CC7) is latched into U43 so that the internal memory bus may be used by the CRT9007 while the 8088 finishes the read cycle. The latch outputs (XDB0-7) are enabled (U43-1) by the combination of /XCRTCSI and /XMEMR at OR gate U61-6. On a write cycle the signal /MWE enables the buffer U46-1 and 19 putting the data (XDB0-7) onto the internal memory bus (CC0-7).

CRT Memory Array

The memory consists of 20,480 bytes of static RAM, using 2K by 8 CMOS. The 8088 can access each chip seperately but the CRT9007 can only access two at once. Under Row Table mode the CRT9007 can only read 8 bits so it is only allowed data from one of the chips it is addressing.

The memory is divided into two banks, A and B. A bank contains the odd-numbered locations (Attributes) and B bank contains the even-numbered locations (Characters)..

Memory Address Decoding

Memory address bus (MA0-13) is driven by the CRT9007 or the CPU to produce the memory addresses. MA0-10 decode the memory addresses while MA11-13, /XCRTCSI, /XBA0, /CPCYC, and /VIDCYC are decoded to produce /CS inputs (pin 8) for the memory array by U25 and U38. Decoding is done so that when /CPCYC is active only one bank will be selected, but when /VIDCYC is active both banks will be selected.

U24 is used to gate the chip select signals so that they occur after the /MW signal. U51-1 to 6 allow the /CS signals to occur on a /MW, /VIDCYC, or an /XMEMR cycle. U51-9 to 11 is used to provide a OE signal to the memory array on either a /VIDCYC or /CPCYC cycle.

Memory Data

The A bank data bus (lines AT0-7) are connected to octal latch U14 and the A side of U30. Data read from the A bank is latched into U14 by the trailing (rising) edge of /VIDCYC (pin 11), the same signal latches the B bank (lines CC0-7) into U44. The outputs of U14 (LAT0-7) and U44 (LCC0-7) are used for character generation and attributes decoding. The lines CC0-7 are also connected to the B side of U30 and to the "latching transceiver" circuit composed of U43 and U46.

U30 is used for 8088 memory cycles, enabled at pin 19 by the output of U61 (pin 11), when the external address bit /XBA0 and /CPCYC are active. It is used to isolate the two banks and is only active when the 8088 is attempting to access the A bank. The direction of U30 is controlled by /MWE.

Alphanumerics Generation

Attributes Decoding

Character code bits, LCC0-7 are presented at the inputs of character generator U3. At the same time the attributes code bits LAT0-7 are at the inputs to PAL U6. If CB3 is high, the bits will pass unmodified to become FAT0-7, if CB3 is low, the bits will be modified. COL/MONO drives pin 11 and prevents the underline attribute from being decoded when the memory is mapped as a Monochrome adapter. When CB3 is low, FAT3 and 4 and CB3 are used by PAL U25 to activate the CHARBL attribute input to the 8021 attribute controller U21. The three bits, FAT0, 1, 2 go directly to inputs UND (underline), REV (reverse video), BLINK (character blink). FAT3, 4 go to U1 to produce superscript and supscript attributes. FAT5 goes to U37 to produce the intensify attribute. FAT6, 7 go to U10 to produce the first and second halves of the double width character attribute. FAT6 is also routed to U23 to allow a double width cursor.

Attributes Controller

The CRT8021 attributes controller, U21, samples the status of inputs CHB, UND, REV, BLINK, scan-count inputs SL0-3, CURSOR and RTBL, and the video data parallel inputs A0-7,

once every character clock interval. On the basis of the attribute inputs, the data may be modified before being shifted out at DOTCLK frequency on the VIDEO output. The VS input is driven at the vertical raster frequency by the VSYNC output of CRT9007. It is internally divided to produce character and cursor blink rates.

Superscript and Subscript Logic

FAT3 and 4 are clocked into U1 on the rising edge of DC1, the outputs (5 and 9) drive the B inputs of adder U2. The adder adds a number (0 for no action, 1 for superscript, and 14 for subscript) to the scan count on SL0-2 from CRT9007 and DSL3 (U22-4) causing the character block to shift up by one or down by two scan lines on the screen. The result of the addition is the scan-count, used, as the LSB of the address to the character generator EPROM. When CB3 is low the super and subscript flip-flop U1 is held inactive.

Intensify Logic

FAT5 is given a two character delay by flip-flop U37 (clocked by DC4) to match the delay in the 8021 input and output. The delayed FAT5 is clocked into U49 by DC8 and will appear at the output, pin 9, at the same time as the video output at pin 5, which has been reclocked by DOTCLK to synchronize it.

Double Width Characters

FAT6 and 7 are connected to U10. When both are inactive, U10 passes unmodified bits 00-07 from U3 to inputs A0-7 of 8021. When FAT6 is active the first four bits 00-03 are reproduced across A0-7, when FAT7 is active 04-07 are reproduced.

Cursor Circuitry

Three types of cursor are available under program control, A) invisible, B) double-width, and C) underline.

The cursor signal from the CRT9007 is ANDed (U23) with CB7, so CB7 can turn the cursor on or off. If CB7 is high the cursor is ORed (U34) with the Q output of flip-flop U36, so if Q is set, the cursor will be forced active. The signal is then

ANDed (U23), with CURTYP, (produced by ORing SL3 and CB6). CB6 is the cursor type selection bit which can provide either a block or underline cursor. For underline, CURTYP is only active the same time as SL3, for block cursor, CURTYP is permanently high. If CURTYP is high, the CURSOR signal reaches U21 pin 27. It is also ANDed with FAT6 (first half of a double width character) to produce a signal clocked into U36 by DC7. If the cursor goes active at the first half of a double width character, the output of U36 will go high for one character time, forcing the cursor to be active for two character times.

Graphics Generation

In graphics mode none of the alphanumeric circuitry is used. Characters are looked up in a table by software and written to the screen.

Serializers

The 16-bit memory word, LCC0-7 and LAT0-7 go to two PISO registers. U15 receives the odd numbered bits and U31 receives the even bits. The serial outputs appear as bits 0 and 1, 2 and 3, 4 and 5, 6 and 7.

Low Resolution Graphics

These pairs of bits are used directly in low resolution graphics mode, to define the four grey scales possible for each pixel:

Even	Odd		
0	0	= Black	
0	1	= Dark Grey	(these are actually
1	0	= Light Grey	shades of amber)
1	1	= White	

These bits drive two of the inputs of the graphics mode selection multiplexer, U29-3 and 6. The shift registers are clocked at DOTCLK frequency 6MHZ.

High Resolution Graphics

The two parallel bit streams from U15 and U31 must be multiplexed into a single bit stream at twice the dot rate. The odd and even bits enter U13 and are selected in turn by the high and low states of the same clock which clocks them out of the shift registers, (6Mhz from U28). The serialized bit stream (U13-9) is clocked by the 12Mhz clock through U28 and fed to both grey scale inputs of the high resolution side of U29 (inputs 2 and 5), making the video output white for on and black for off, with no intermediate states.

Graphics Blanking

The blanking signal, CBLANK, from U75-35 is inverted by U22-11 and NORed with DC3 (U9) to drive the input of flip-flop U36-2. U36 is clocked by the 12 MHZ clock so that CBLANK, if active, is clocked into the flip-flop at the same time the registers (U15 and U31) are loaded. U36-6 is used to clear the registers at this time. Stray bits may appear at the outputs of the shift registers before they are cleared, so U36-5 is fed to the enable inputs of multiplexers U13 and U29. U29 will be disabled when CB1 = 1 (low resolution mode) because the bits go directly to U29. U13 will be disabled directly in the High resolution mode.

Mode Selection

Several mode bits have been described, all coming from the control register U60.

Control BIT 0

CB0 selects either the Row Table (CB0 = 1) or Normal Mode (CB0 = 0).

Control BIT 1

CB1 selects between high and low resolution graphics mode. This bit has no relevance if CB2 = 0. The selection is done at U29 by selecting either the A (2 and 5) or B (3 and 6) inputs to drive the two outputs (4 and 7). The two outputs contain the video information for the graphics mode selected. CB1 = 0 for high resolution and 1 for low resolution.

Control BIT 2

CB2 selects which of two pairs of bits (Graphics or Alphanumeric) will drive the Grey Scale Bits, GR0 and GR1. It is connected to the SEL input of U35. The two graphic bits from U29 go to the B inputs of U35 and will be selected when CB2 = 1. When CB 2 = 0 the two alphanumeric bits from AND gate U52 are selected.

Control BIT 3

CB3 selects between either IBM attributes (CB3 = 0) or Hyperion (CB3 = 1).

Control BIT 4

CB4 is used to select the 12Mhz DOTCLK (CB4 = 0) or the 6Mhz DOTCLK (CB4 = 1) at U13-2. The 12MHZ DOTCLK is used to display 80 characters and high resolution graphics while the 6MHZ DOTCLK is used to display 40 characters and low resolution graphics.

Control BIT 5

CB5 is buffered by U66 bus driver and appears at J1-3 to drive the CRT board 60/70 Hz vertical size control input. 60Hz is selected when CB5 = 1 and provides for 250 scan lines, 70Hz is selected when CB5 = 0 and provides for 200 scan lines.

Control BIT 6

CB6 selects either Cursor Underline (CB6 = 0) or Block Cursor (CB6 = 1).

Control BIT 7

CB7 selects either Cursor Invisible (CB7 = 0) or Cursor Visible (CB7 = 1).

Video Output Circuits

Sync Signals

The drive signals /HSYNC (inverted by U5) and /VSYNC are fed to buffer U66. The outputs (positive-going horizontal and negative going vertical) are fed to J1-1 and J1-4.

Video Signals

The two grey scale bits GR0 and GR1 are fed into buffer U66 and the resulting out signals drive the network consisting of R17, R19, D1, D3, R20, and the tap at R20 driving the VIDEO output J1-2. There are four voltage levels provided to drive the required brightness levels of the CRT.

GR1	GR0	Vout
0	0	0v
0	1	1.6v
1	0	2.0v
1	1	2.25v

Composite Video

The two grey scale bits are fed into U66 along with CSYNC, the three buffered outputs are fed to a network consisting of R18, R21, R22, D2, D4, D5, and R25. The output appearing across R25 is a composite video signal with the sync combined with four levels of active video, and drives the RCA connector J5.

Real Time Clock

The RTC (U11) receives its power from the battery circuit on the System Board. It updates time and date once every second. Four control bits and four data input/output bits are used to read and write data to the clock, through (U4) an Intel 8255A-5 general purpose parallel interface port.

Parallel Printer Port

During a write to the printer data or control ports, the eight data bits (XDB0-7) appear at the "A" output of U72 as BB0-7. They are fed to U84 and output synchronously to the printer. The control register (U78) provides control bits to synchronize the data output (strobe control), select, initialize or enable the autofeed feature of the printer. One control bit is used to enable or disable the printer interrupt to the CPU.

Five status bits (U71) are used to interpret the current state of the printer.

Serial Port

The serial port uses the Z80A-SIO controller (U70), which has two seperate channels, one for the serial port and one for the modem.

Both synchronous (up to 100K baud) and asynchronous (all common baud rates from 75 to 19.2K) modes are supported. For snychronous mode an internal or an external clock can be used. Asynchronous mode may be configured for five to eight bits per character, optional parity, one or two stop bits and baud rate selection.

Synchronous mode may be byte or bit synchronous, monosync, bisync or SDLC.

Expansion Connector Signals

Signal	I/O	Description
OSC	O	OSCILLATOR: 14.31818MHz at 50% duty cycle.
MCLK	O	MASTER CLOCK: 4.77MHz at 33% duty cycle.
RESET	O	RESET: Reset or initialize system logic on power up.
BA0-19	O	ADDRESS BITS 0-19.
DB0-7	I/O	DATA BITS 0-7.
ALE	O	ADDRESS LATCH ENABLE: Used to latch valid addresses from the processor.
/IO CH CK	I	I/O CHANNEL CHECK: Provides the CPU with parity information on memory or devices in the I/O Channel.
IO CH RDY	I	I/O CHANNEL READY: This line is pulled low by a memory or I/O device to lengthen memory or I/O cycles.
/IRQ3,4,5	I	INTERRUPT REQUEST 3-5: Used to signal the processor that an I/O device requires attention.
/IROC	O	I/O READ COMMAND: Instructs an I/O device to place its data onto the data bus. Signal may come from the processor or DMA Controller.

/IOWC	O	I/O WRITE COMMAND: Instructs the I/O device to read the data bus. Signal may come from the processor or DMA Controller.
/MEMR	O	MEMORY READ COMMAND: Instructs the memory device to place its data onto the data bus. Signal may come from the processor or DMA Controller.
/MEMW	O	MEMORY WRITE COMMAND: Instructs the memory device to store the data on the data bus. Signal may come from the processor or DMA Controller.
/DRQ1 & 3	I	DMA REQUEST 1 and 3: These are asynchronous channel requests.
/DACK0,1,3	O	DMA ACKNOWLEDGE 0,1 and 3: these lines acknowledge the corresponding DMA request.
AEN	O	ADDRESS ENABLE: Used to delegate the bus between the processor and DMA Controller.
T/C	O	TERMINAL COUNT: Provides a pulse when the terminal count for any DMA channel is reached.

5.3 Modem Board

The Modem Board is composed of the following major areas:

A) Modem Chip

B) Tone Generator

C) Telephone Line Interface

Modem Chip

The Modem Board can support the 20 pin National 74HC942 or the 18 pin Texas Instrument TMS 99532 Modem Chip. Both chips use the same socket location on the PCB. For this reason the schematic shows two pin numbers. The numbers in brackets refer to the TMS 99532 chip and those without brackets refer to the numbering of the 74HC942.

The Modem Chip (U2) currently installed is an 18 pin TMS 99532 operating at 300 Baud.

Several external components are required when using this Modem Chip:

1) 4.032MHZ parallel resonant crystal.

2) A parallel RC circuit for adjusting /DCD sensitivity on TMG, pin 4 (3).

3) Resistive pullup on /ATE, pin 10 (9).

4) +12v supply for VDD, pin 15 (14).

When the alternate Modem Chip (20 pin National 74HC942) is installed the following external components are required.

1) 3.579549MHZ crystal (selected by jumper E3).

2) A parallel RC circuit for adjusting /DCD sensitivity on CDT, pin 4 (3).

3) Resistor pullup on TLA, pin 20.

4) Resistive voltage divider on CDA, pin 7 (6).

5) Decoupling capacitor on FTLC, pin 10 (9).

The Modem Chip acts as a translator of data from digital to analog or analog to digital. The digital information is sent to or received from the SIO Controller (U70) and the 8255A-5 PPI (U4) on the Display & I/O Board. The analog information is sent to or received from the direct connect telephone line interface and the acoustic interface.

Tone Generator

The Mostek MK5089 Integrated Tone Dialer, (U1), provides DTMF or "touch tone" signals for dialing numbers. Each number or symbol on the 12 key telephone pad is comprised of a "row" and "column" frequency. The chip digitally synthesizes the row and column frequencies.

Telephone Line Interface

The Modem draws a DC current in the two wires TIP and RING, which is called going "Off-Hook". This is acknowledged by the Central Office providing a dial tone. The Modem then routes the call by dialing a series of numbers, which is called "network addressing". All voice and data (AC) signals are carried on TIP and RING and are superimposed on the DC current flow in TIP and RING. To terminate a call the DC current must be interupted for about one second, which is called going "On-Hook".

DC Loop Characteristics

The relay K1 initiates or terminates the DC loop current. Upon going off-hook (K1 closed), R64 and R60 bias op-amp U9 with respect to its power rails (TIP and RING). The DC level at the base of Q4 turns it on. At loop currents below 40mA, Q4 passes all of the DC current, but as the current rises above 40mA, D8 turns on and starts to dissipate the excess current. D4, D5, D6, and D7 form a rectifying circuit to provide the proper DC volage polarity for op-amp U9 regardless of the polarity of TIP and RING.

Signal Transmission

Tones from the tone generator (U1-16) or signals from the Modem chip (U2-17) are summed through one of the op-amps of U4. The output is DC coupled through isolation transformer (T1) to U9. The output of U9, modulates the base of Q4 causing the signal to appear on TIP and RING.

Signal Reception

Signals on TIP and RING are received by a capacitively coupled differential op-amp (U4), providing AC coupling and high voltage isolation (provided by the 300k resistors). The signal is then gated through U5 to protect the Modem receiver input from signal levels greater than – 12dBm.

Ring Detection

The ring signal is a 40-150 Vrms, 16-68Hz sinusodal waveform superimposed on a 48V battery feed voltage. A ring consists of a two second burst of sine wave followed by four seconds of silence. Capacitor C29 is used to AC couple the ring detect circuit and give the proper ring detect impedence. When the 75V zener D3 turns on during one half of the ringing waveform, optoisolator U7 becomes forward biased and pulls the base of Q2 low. This allows the input to comparator U3-2 to rise. When it reaches the reference level of VBIAS, the output goes low producing RI. This signal is sent to the SIO on the Display & I/O Board to indicate ringing is occuring. RI will go low for signals greater than 36-38 Vrms of any frequency.

Extension Hookswitch Status

If the extension phone is on-hook it draws virtually no current but if the phone is off-hook it draws several milliamperes. The DC current flow when off-hook can be in either direction so two optoisolators are required, U6 and U8. When forward biased the opto which is "on" will cause HS2 to be active. The infa-red emitters D9 and D10 are used to shunt excess current from U6 and U8 since off-hook DC current may vary from 5 to 120mA.

Surge Protection

RV1 acts as an open circuit below 250VDC, above this it gradually begins to conduct and dissipate the excess voltage. R41, R44, R52, R53, R54 provide protection to the Modem for lightening and longitudinal surges.

Isolation

The Modem is isolated from the telephone line by several high voltage components providing electrical isolation for voltages up to 1500VDC. These components are T1, K1, U6, U7, U8, R53, R54, C30 and C31.

Acoustic Interface

U3-5 to 10 and associated circuitry provide the acoustic interface to and from acoustic cups.

Speaker Volume Control

The signal to the speaker may be turned on or off using one gate of U5 via control port VM1. Four volume levels are obtained by selectively switching R35 and R36 in or out of the circuit using two other gates of U5 and control ports VM2 and VM3.

Keytelephone Interface

The Hyperion may be used in a keytelephone system if the Hyperion Keytelephone Adapter is used. This adapter is a seperate part and is not included with the Hyperion itself.

6.0 Terms and Definitions

6.1 General Terms

BAUD	Bits Per Second
CPU	Central Processing Unit
CRT	Cathode Ray Tube
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DRAM	Dynamic Random Access Memory
EPROM	Erasable Programmable Read Only Memory
FDC	Floppy Disk Controller
I/O	Input/Output
LED	Light Emitting Diode
LSB	Least Significant Bit
LSI	Large Scale Integration
MODEM	Modulator/Demodulator
MSB	Most Significant Bit
PAL	Programmable Array Logic
PCB	Printed Circuit Board
PIC	Priority Interrupt Controller
RTC	Real Time Clock
SIPO	Serial In Parallel Out

6.2 System Board Signals

AEN	Address Enable. Active low signal generated by the Bus Arbiter to disable the CPU address demultiplexers during DMA transfers.
ALE	Address Latch Enable. Signal produced by the Bus Controller to enable the address latches. Enables on the negative going edge.
A0-A19	Address lines 0 to 19.
CAS	Column Address Strobe. (Active Low).
CSRAM	Chip Select for onboard RAM. (Active Low).
CSPIC	Chip Select for PIC. (Active Low).
DACK 0-3	DMA Acknowledge Lines. Active low lines used by the DMAC to notify the individual peripherals when they have been granted a DMA cycle.
DREQ 0-3	DMA Request Lines. Active low lines used by the peripheral circuits to obtain DMA service.
DB0-7	Data Bus Lines 0 to 7.
EOP	End Of Process. (Active Low).
HLDA	Hold Acknowledge. (Active Low).
HRQ	Hold Request. (Active High).
INTA	Interrupt Acknowledge. Active low signal from the Bus Controller to the PIC causing it to release interrupt information onto the Data Bus.
IOCHRDY	Input/Output Channel Ready. (Active High).
IORC	Input/Output Read Cycle. (Clocks on negative going edge).

IORDY	Input/Output Ready. (Active High).
IOWC	Input/Output Write Cycle. (Active Low).
KBCLK	Keyboard Clock. A 600Hz signal from the Keyboard used to clock data into the Keyboard shift register (U96). It is pulled low by the CPU, (ACK), to prevent the Keyboard from sending data while the CPU is reading the register.
KBRST	Keyboard Reset. Active low generated by U28 to reset the Keyboard if DB7 is low when WRTKBREG is active.
MCLK	Master Clock.
MEMR	Memory Read. (Active Low).
NMI	Non Maskable Interrupt. Signal generated to indicate a parity error in RAM.
RAMENB	RAM Enable. Active low signal, output from PAL U22, used to initiate a memory access cycle.
RAS	Row Address Strobe. Active low signal, derived from BA16 and BA17, used to select the RAM bank.
RDY	Ready.
RFSH	RAM Refresh. Active low signal, derived from DACK0, used to initiate a RAM refresh cycle.
RQ/GTO	Request/Grant. Active low signal exchanged between processor and co-processor, used to initiate local bus transfer.
RW/SEEK	Read/Write or Seek. (RW Active Low). (Seek Active High).
S0-S2	Status Lines. Active low lines issued by the CPU to the Bus Controller. The Bus Controller interprets these lines and generates command and control signals.
SP/EN	Slave Program/Enable Buffer. (Active Low).

STEP	Step. (Moves Disk Head)(Active Low).
WE	Write Enable. Active low signal used to latch data into the selected byte of memory.
WRDATA	MFM Encoded Data to Disk Drive. (Active Low).
WRTKBREG	Write Keyboard Register. Active low signal initiated by the CPU through PAL U26, used to clear the Keyboard shift register (U96).
WP	Write Protect. Active low signal indicating the diskette installed in the drive is Write Protected.

6.3 Display and I/O Board

AT0-7	Attribute lines 0-7 from bank A of memory.
CCLK	Cycle Clock for the CRT9007 controller chip.
CC0-7	Character Code lines 0-7 from Bank B of memory.
CB0-7	Control Bits 0-7. Produced by Control register U60, used to select different modes of operation.
CBLANK	Composite Video Sync. (Active High).
CURTYP	Cursor Type. (Active High).
DC1-DC8	Clock pulses produced by the Phase Generator. The period of each is one-eighth of DOTCLK. They are used to control functions on the Display Board.
DOTCLK	DOT Clock, 12 or 6 MHz clock used by the display circuitry. 12MHz DOTCLK is used in 80 character mode and high resolution graphics, 6MHz DOTCLK is used for all other modes.
FAT0-7	Functional Attribute 0-7. Outputs of PAL U6 which enable various attribute circuitry if CB3 is low.
HSYNC	Positive going horizontal sync signal used to drive the CRT board.
LAT0-7	Latched Attribute 0-7. (Active High).
LCC0-7	Latched Character Code 0-7. (Active High).
MA0-7	Memory Address Lines.
MW	Memory Write. Active low signal used to enable WE (pin21), of the CRT RAM chips.
MWE	Memory Write Enable. Active low used to enable data buffer U46, causing data from the CPU to be placed on the internal memory bus as CC0-7.

PIXEL	Picture Element. A dot on the screen in graphics defined by a combination of bits in memory.
SL0-3	Scan Lines 0-3 produced by the CRT9007 controller chip.
VIDCYC	CRT Chip memory (CRT Memory) Cycle. Time when CRT chip may access memory, valid between DC5 to DC8.
VSYNC	Vertical Sync. Negative going vertical sync signal used to drive the CRT board.
XCRTCS0-3	CRT Chip Select. (External)(Active Low).
XBA	Bus Address. (External).
XDB0-7	Data Bus 0-7. (External).
XIOWC	Input/Output Write Cycle. (External)(Active Low).
XMEMW	Memory Write. (External)(Active Low).
XMEMR	Memory Read. (External)(Active Low).
XRESET	Reset. (External).

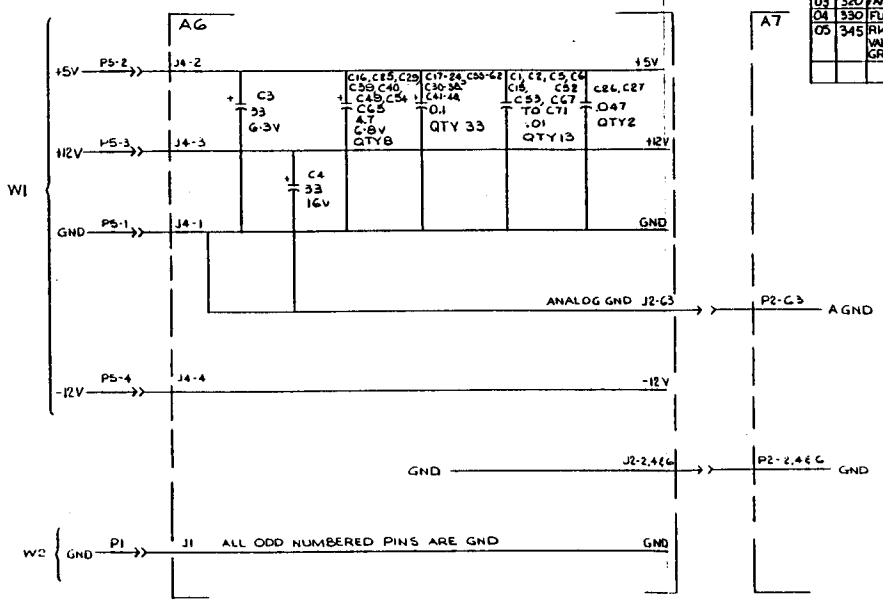
6.4 Modem Board Signals

ATE	Answer Tone Enable. (Active Low).
dB	Decibel. Ratio of output signal power to input signal power.
DCD	Data Carrier Detect. Active low signal signifying the Modem has detected a signal of the proper mark frequency and amplitude for error free reception of data.
DTMF	Dual Tone Multi-Frequency.
DUPLEX	Full: Allows simultaneous transmission and reception of data. Half: Allows either transmission or reception of data only.
FSK	Frequency Shift Keying. Frequency modulation method which varies the carrier frequency to correspond to binary logic.
HS2	Hookswitch2. Active low signal indicating current flow in LEDs U6 and U8.
OFF-HOOK	Electrically connected state of data transmission system, ie, current is flowing in the local loop.
ON-HOOK	Electrically disconnected state of data transmission system, ie, current is not flowing in the local loop.
RI	Ring Indicator. Active low signal used in combination with a software filter to determine if ringing is occurring.
EIA RS232	An interface specification of Electronic Industry Association that determines a standard interconnect scheme between data terminal equipment and data communications equipment.
EIA RS243	See RS232.

7.0 Schematic Diagrams

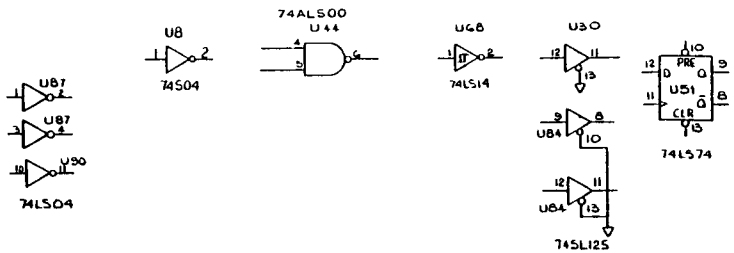
REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
99		PRELIMINARY RELEASE				
9B		CIRCUIT & DESIG. CHANGES				
0A		CIRCUIT & DESIG. CHANGES				
00	315	PRODUCTION RELEASE				
01	321	CIRCUIT UPDATE				
02	ATT3 321	SHT.5 ZONE C5 & A6 U8 WAS 74LS04				
03	320	FAN CIRCUITRY JUMPERS ADDED				
04	330	FULL FAN CIRCUITRY ADDED				
05	345	R14 DELETED. R10, R12 & R13 VALUES CHANGED. R11 & R13 GROUNDED.				

POWER AND GROUND TABLE				
IC No	TYPE	POWER	GROUND	QTY
U55	Am2964B	10	30	1
U91	FDC 9216B	8	4	1
U9-U17, U33-U40, U56-U64, U74-U82	2164A-20	8	16	36
U22-U24	PAL10L8	20	10	3
U73	RCLL-13XX	14	7	1
U47	8237A-5	31	20	1
U42	8087	40	1,20	1
U41	8088	40	1,20	1
U94	8253A-5	24	12	1
U43	8259A-5	28	14	1
U50	8272	40	20	1
U83	8284A	18	9	1
U18	8288	20	10	1
U48	2764A-3	28	14	1
UT1	74LS161A	16	8	1
U52	74LS195A	16	8	1
U95	74LS280	14	7	1
U96	74LS322A	20	10	1
U49	74LS670	16	8	1
UT2, U85, U93	74LS175	16	8	3
U19-U21, U46	74LS373	20	10	4
U65	74LS30	14	7	1
U53	74LS00	14	7	1
U92	74LS02	14	7	1
U87, U90	74LS04	14	7	2
U26, U54, U84	74LS08	14	7	3
U7, U68, U89	74LS14	14	7	3
U66	74LS32	14	7	1
U28, U75, U2-U5, U88, U45	74LS74	14	7	6
U30, U86, U88	74LS125	14	7	3
U1-U5, U97, U98	74LS244	20	10	7
U6, U66	74LS245	20	10	2
U45	74LS74	14	7	1
U25	LM386	6	4	1
U44	74ALS00	14	7	1
U8	74S04	14	7	1



NOTES:
1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, 1/4 W; CAPACITANCE VALUES ARE IN MICROFARADS.

SPARE GATES:



HIGHEST DESIGNATIONS USED												
BT	C	D	E	FL	J	Q	R	RN	U	Y		
BT1	C81	D8	E6	FL6	J6	Q13	R54	RN8	U98	Y1		
HIGHEST DESIGNATIONS NOT USED												
C28	D1						R14					

										REV	SHEET
										04	00
										03	05
										00	C
										3	05
7	6	5	4	3	2	1	SHEET INDEX				

100004-800	HYPERBUS		
NEXT ASSY	USED ON		

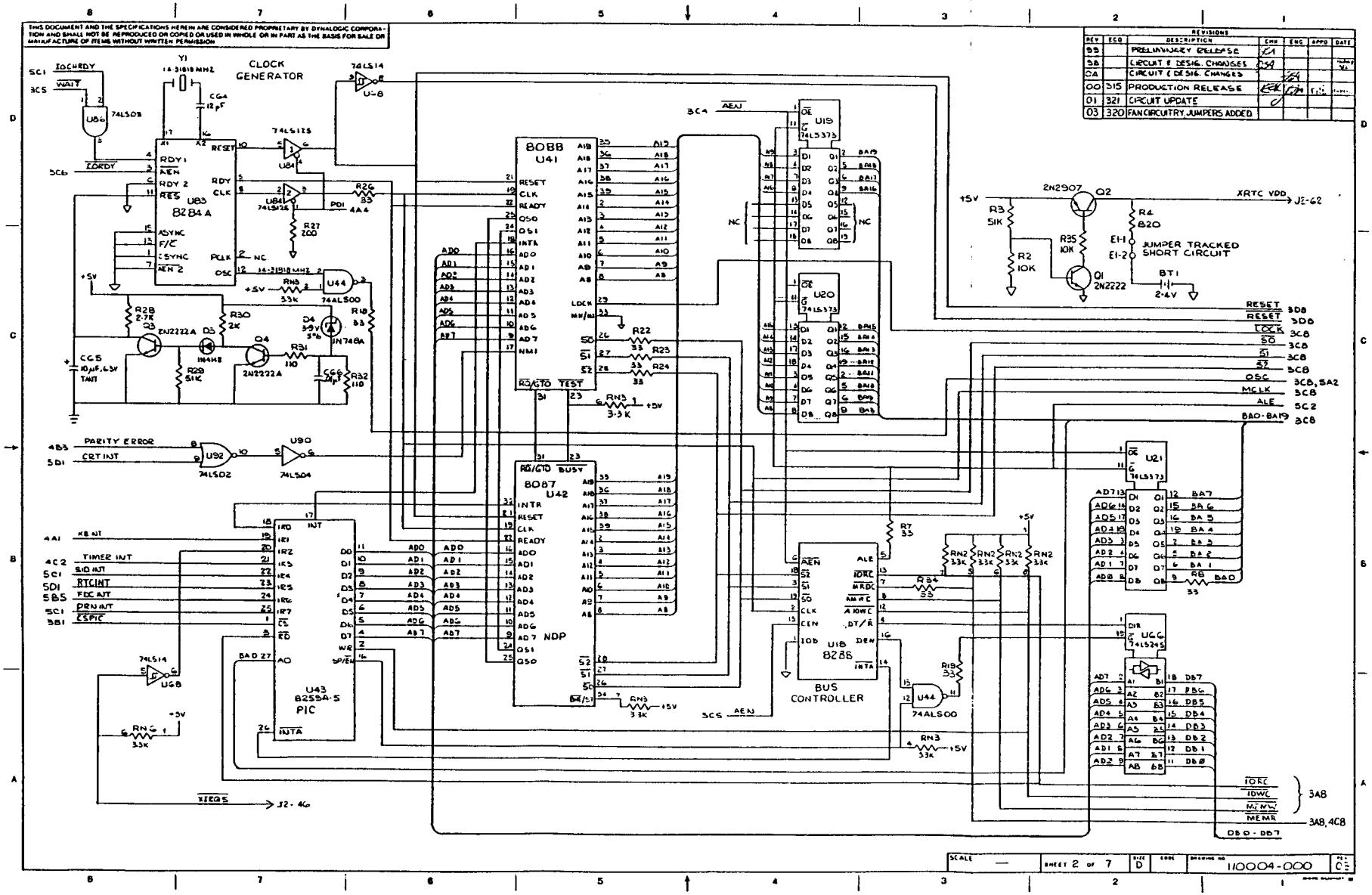
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS ±1/32 DECIMAL .X ±.03 .XX ±.010 ANGLES ±2°
PARTS TO BE FREE FROM BURRS AND ALL SHARP EDGES
UNLESS OTHERWISE SPECIFIED ALL MACHINE SURFACES
MATERIAL
FINISH

DRAWN GL / KCK
CHECKED
ENGINEER
APPROVED (MFG. MGR.)
INITIAL APPROBATION
SHEET 1 OF 7

Dynalogic Corporation
Ottawa – Canada

TITLE
SCHEMATIC DIAGRAM
SYSTEM CARD A6

SIZE D | CODE | DRAWING NO 110004-000 | REV 05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REVISIONS
REV | ECO | DESCRIPTION | ENG | APPD | DATE
99 | | PRELIMINARY RELEASE
9B | | CIRCUIT & DESIG. CHANGES
9A | | CIRCUIT & DESIG. CHANGES
00 | 315 | PRODUCTION RELEASE
01 | 321 | CIRCUIT UPDATE
03 | 320 | FAN CIRCUITRY, JUMPERS ADDED
CLOCK GENERATOR
Y1 14.31818 MHZ
CG4 12pF
74LS14 U68
74LS08 U86
74LS123 U84
U83 8284A
RESET
RDY1
AEN
RDY 2
RES
ASYNC
F/C
CSYNC
AEN 2
RDY
CLK
PCLK
OSC
14.31818 MHZ
NC
IOCHRDY
WAIT
XRDY
R26 33
R27 200
PDI 4A4
+5V
RN3 33K
U44 74ALS00
R28 2.7K
Q3 2N2222A
D5 1N4148
R30 2K
Q4 2N2222A
R31 110
R29 51K
CG5 10µF, 6.3V TANT
CG6 .1µF
R32 110
D4 3.9V 5%
1N748A
R18 33
8088 U41
RESET
CLK
READY
QS0
QS1
INTA
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
NMI
RQ/GT0
TEST
LOCK
MN/MX
R22 33
R23 33
R24 33
RN3 1 3.3K +5V
8087 U42
INTR
RESET
CLK
READY
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
QS1
QS0
RQ/GT0
BUSY
NDP
RN3 3.3K +5V
AEN
U19 74LS373
U20 74LS373
NC
BA19
BA18
BA17
BA16
U21 74LS373
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BA0
R84 33
RN2 3.3K
R7 33
U18 8288 BUS CONTROLLER
AEN
CLK
CEN
IOB
ALE
MRDC
AMWC
AIOWC
DT/R
DEN
INTA
U44 74ALS00
R19 33
RN3 33K +5V
U66 74LS245
DIR
G
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
2N2907 Q2
R3 51K
R2 10K
R4 820
R35 10K
E1-1
E1-2
JUMPER TRACKED SHORT CIRCUIT
Q1 2N2222
BT1 2.4V
+5V
XRTC VDD → J2-62
PARITY ERROR
CRT INT
U92 74LS02
U90 74LS04
U43 8255A-5 PIC
INT
IR0 IR1 IR2 IR3 IR4 IR5 IR6 IR7
CS RD WR SP/EN A0
D0 D1 D2 D3 D4 D5 D6 D7
BAD 27
INTA
KB INT
TIMER INT
SIO INT
RTCINT
FDC INT
PRN INT
ESPIC
RN6 33K
XREQ5 → J2-46
RESET 3D8
RESET 3D8
LOCK 3C8
S0 3C8
S1 3C8
S2 3C8
QSC 3C8, 5A2
MCLK 3C8
ALE 5C2
BA0-BA19 3C8
IORC
IOWC
MEMW
MEMR
3A8
3A8, 4C8
DB0 - DB7
SCALE —
SHEET 2 OF 7
SIZE D
DRAWING NO 110004-000
REV C3

REVISIONS					
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99		PRELIMINARY RELEASE				
9B		CIRCUIT & DESIG CHANGES				
0A		CIRCUIT & DESIG CHANGES				
00		PRODUCTION RELEASE				

SYSTEM BUS ARBITER

WAIT STATE GENERATOR

DMAC

DEVICE DECODERS

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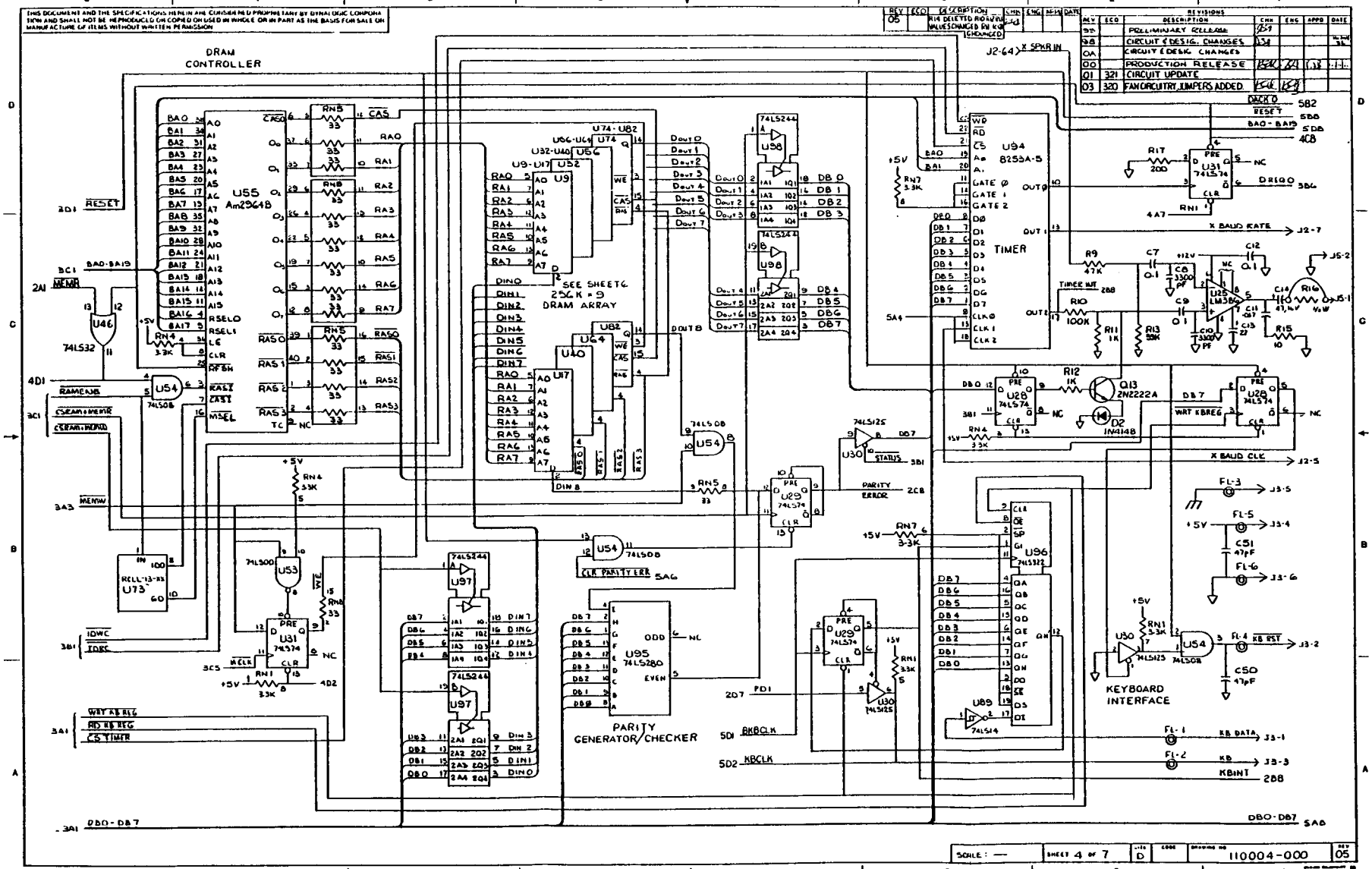
DRAM CONTROLLER
U55 Am29648
SEE SHEET 6 256K x 9 DRAM ARRAY
U74 · U82
U66 · U64
U32 · U40
U9 · U17
U56
U52
U9
U64
U40
U17
U82
U74
U98
U97
U96
U95 74LS280 ODD EVEN
PARITY GENERATOR/CHECKER
U94 8255A-5
TIMER
U73 RCLL-13-83 60
U53 74LS00
U54 74LS08
U46 74LS32
U30 74LS125
U89 74LS14
U28 74LS74
U29 74LS74
U31 74LS74
U26 74LS74
U35 LM336
Q13 2N2222A
D2 IN4148
RESET
RAMENB
CSRAM+MEMR
CSRAM+MEMW
MEMR
MEMW
IOWC
IORC
MCLK
WRT KB REG
RD KB REG
CS TIMER
PARITY ERROR
CLK PARITY ERR
STATUS
WRT KBREG
X BAUD RATE
X BAUD CLK
X SPKR IN
KEYBOARD INTERFACE
KB DATA
KB
KBINT
KB RST
KBCLK
DBO - DB7
BAO - BA19
DACKO
DREQO
TIMER INT
FL-1
FL-2
FL-3
FL-4
FL-5
FL-6
J3-1
J3-2
J3-3
J3-4
J3-5
J3-6
J2-7
J2-5
J5-1
J5-2
J2-64
SCALE: —
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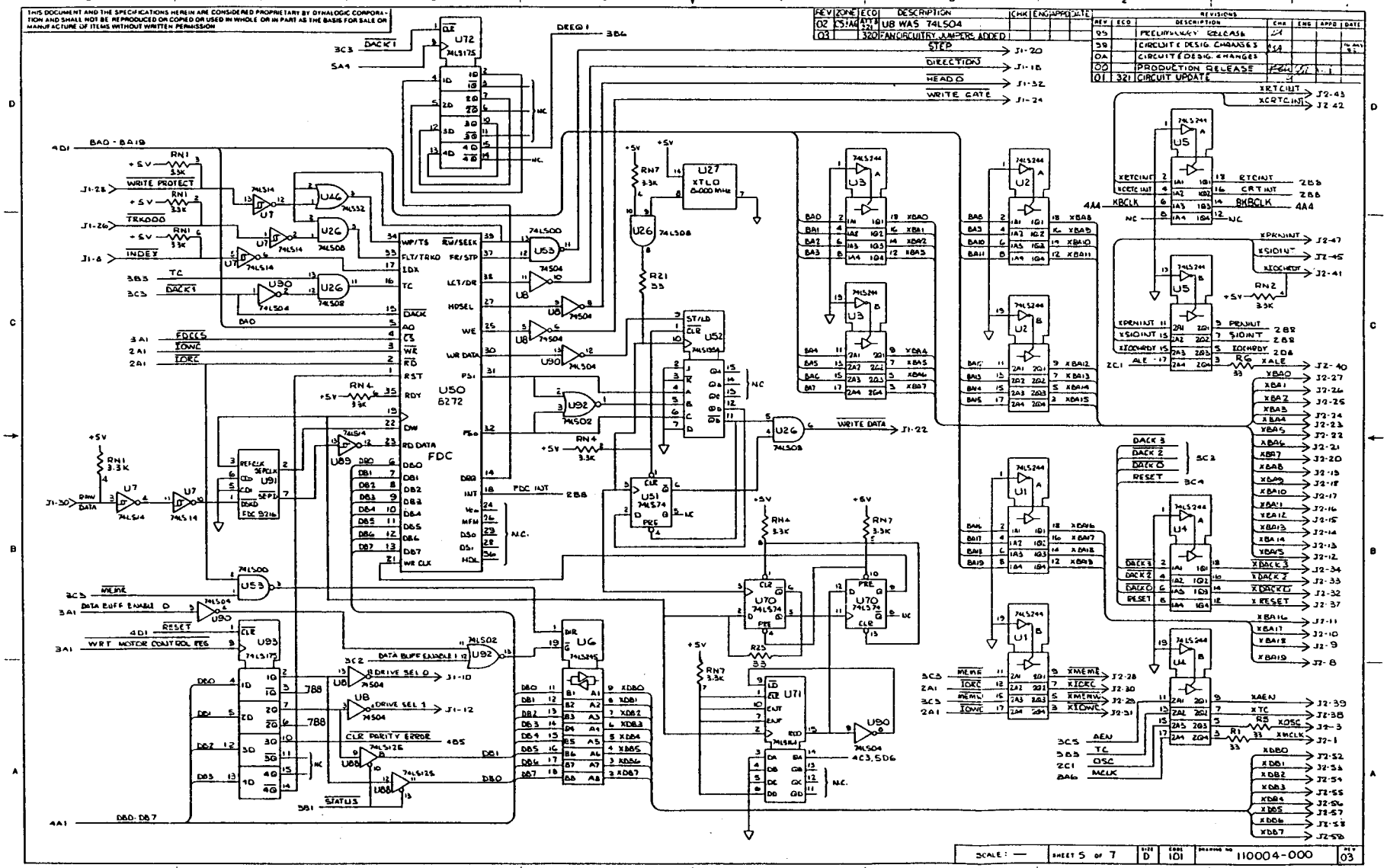
SIZE D
110004-000
REV 05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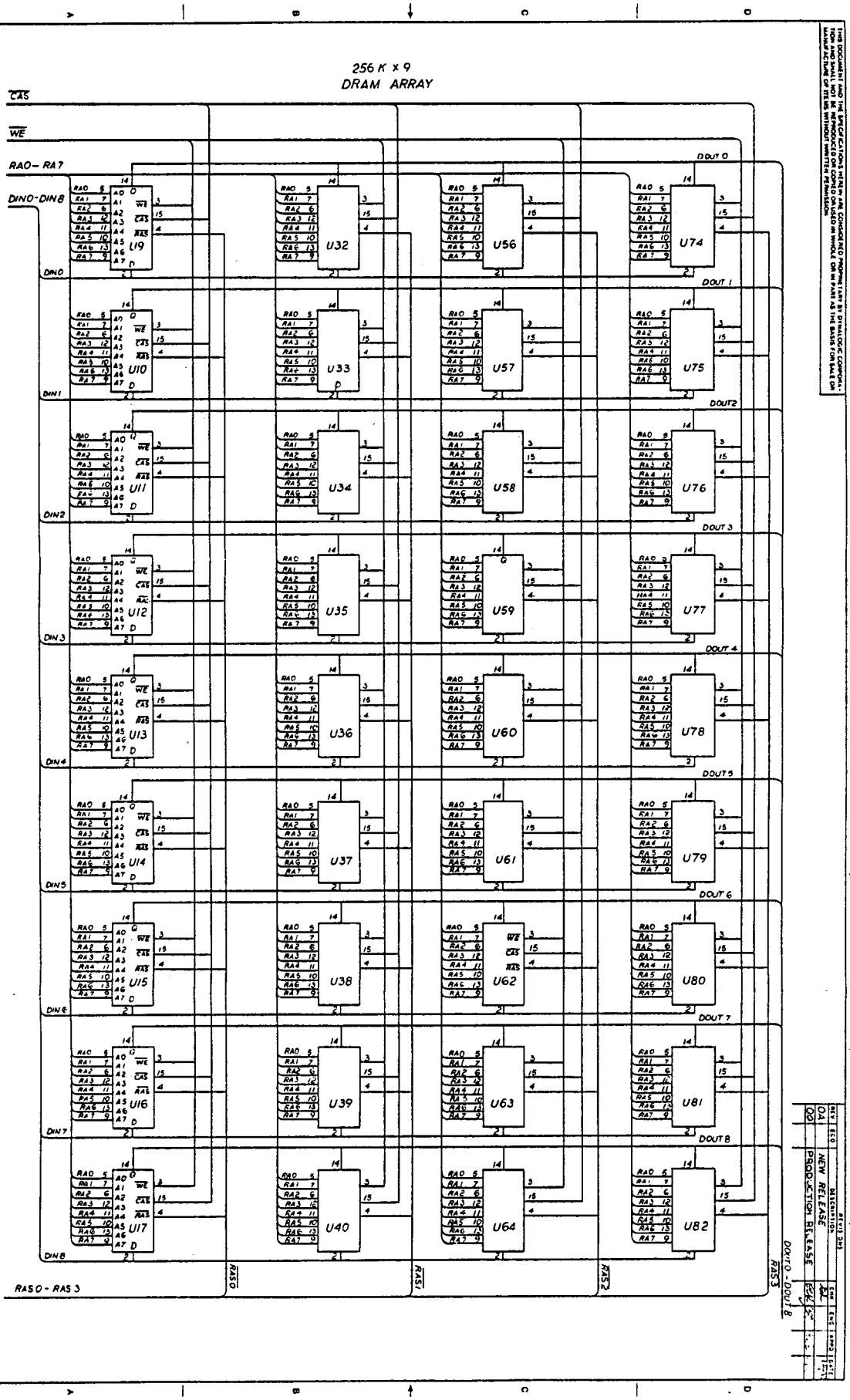
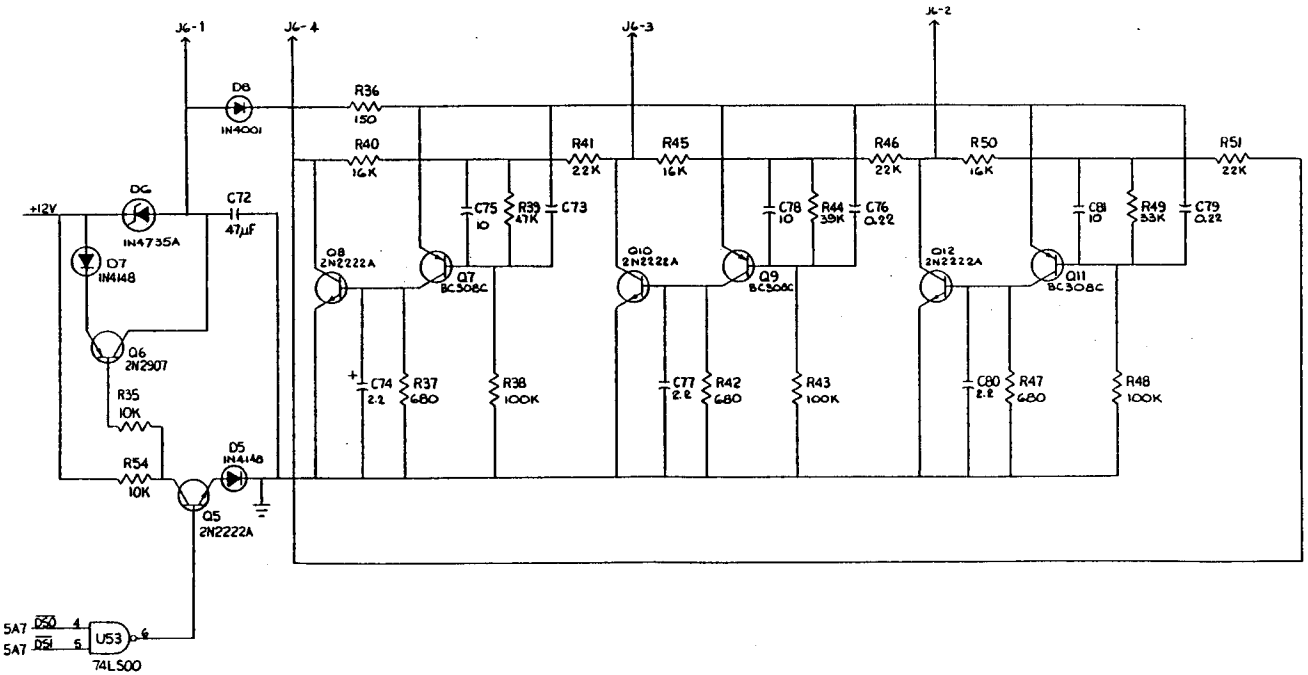
REV ZONE ECO DESCRIPTION CHK ENG APPD DATE
02 CS1A6 A119 321 U8 WAS 74LS04
03 320 FAN CIRCUITRY JUMPERS ADDED
REVISIONS
REV ECO DESCRIPTION CHK ENG APPD DATE
99 PRELIMINARY RELEASE
98 CIRCUITE DESIG. CHANGES
0A CIRCUIT DESIG. CHANGES
00 PRODUCTION RELEASE
01 321 CIRCUIT UPDATE
U50 8272 FDC
U72 74LS175
U27 XTLO 8.000 MHz
U26 74LS08
U46 74LS32
U30 74LS04
U53 74LS00
U8 74S04
U90 74LS04
U92 74LS02
U52 74LS95A
U51 74LS74
U89 74LS14
U91 8216
U7 74LS14
U95 74LS175
U6 74LS245
U88 74LS125
U5 74LS244
U4 74LS244
U3 74LS244
U2 74LS244
U1 74LS244
U70 74LS74
U71 74LS164
RN1 3.3K
RN2 3.3K
RN4 3.3K
RN7 3.3K
R21 33
R22 33
R5 33
R1 33
R6 33
DREQ1
STEP
DIRECTION
HEAD 0
WRITE GATE
WRITE DATA
FDC INT
XRTCINT
XCRTCINT
XKBCLK
XRPRNINT
XSIOINT
XIOCHRDY
XALE
XBA0
XBA1
XBA2
XBA3
XBA4
XBA5
XBA6
XBA7
XBA8
XBA9
XBA10
XBA11
XBA12
XBA13
XBA14
XBA15
XBA16
XBA17
XBA18
XBA19
XDACK3
XDACK2
XDACK0
XRESET
XMEMR
XIORC
XMEMW
XIOWC
XAEN
XTC
XOSC
XMCLK
XDB0
XDB1
XDB2
XDB3
XDB4
XDB5
XDB6
XDB7
DACK 3
DACK 2
DACK 0
RESET
WRT MOTOR CONTROL REG
DATA BUFF ENABLE D
DATA BUFF ENABLE I
DRIVE SEL 0
DRIVE SEL 1
CLR PARITY ERROR
STATUS
WRITE PROTECT
TRK000
INDEX
TC
DACK1
FDCCS
IOWC
IORC
RAW DATA
SCALE: —
SHEET 5 OF 7
SIZE D
CODE 101
DRAWING NO 110004-000
REV 03


256 K x 9
DRAM ARRAY
CAS
WE
RA0 - RA7
DIN0 - DIN8
DOUT 0
DOUT 1
DOUT2
DOUT 3
DOUT 4
DOUT 5
DOUT 6
DOUT 7
DOUT 8
DOUT0 - DOUT8
U19
U32
U56
U74
U10
U33
U57
U75
U11
U34
U58
U76
U12
U35
U59
U77
U13
U36
U60
U78
U14
U37
U61
U79
U15
U38
U62
U80
U16
U39
U63
U81
U17
U40
U64
U82
RAS0
RAS1
RAS2
RAS3
RAS0 - RAS 3
THIS DOCUMENT AND THE SPECIFICATIONS HEREIN ARE CONSIDERED PROPRIETARY BY DYNALOGIC CORPORATION
DESCRIPTION
NEW RELEASE
PRODUCTION RELEASE
SCALE 1 —
SHEET 6 OF 7
SIZE D
DRAWING NO 110004-000
REV 03

REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
04		FAN CIRCUITRY ADDED (SHT. 7)				

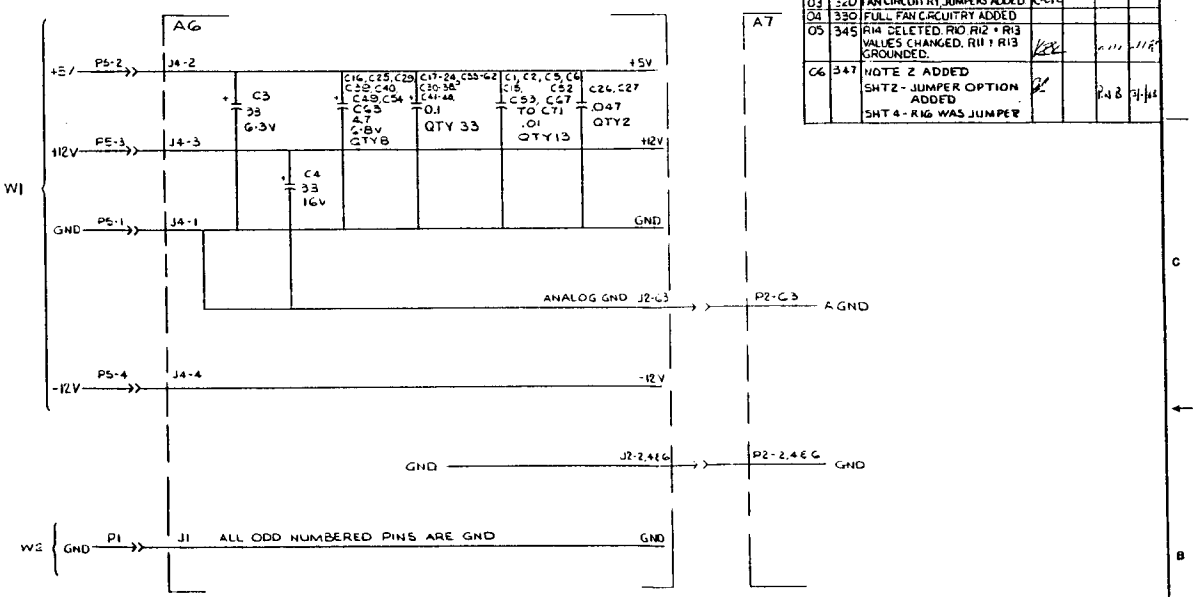


SCALE	SHEET 7 OF 7	SIZE D	CODE	DRAWING NO 110004-001	REV 04

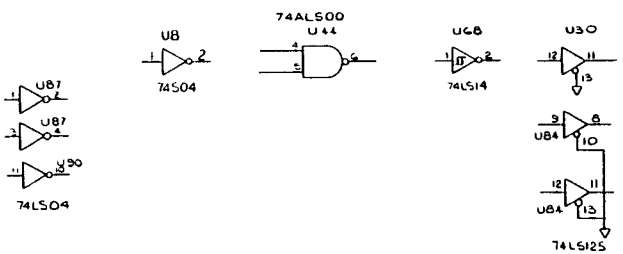
7.2 System Board Rev 06

REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
99		PRELIMINARY RELEASE				
9B		CIRCUIT & DESIG. CHANGES				
0A		CIRCUIT & DESIG. CHANGES				
00	315	PRODUCTION RELEASE				
01	321	CIRCUIT UPDATE				
02	ATT3 321	SHT 5 ZONE C5 ! A6 U8 WAS 74LS04				
03	320	FAN CIRCUITRY JUMPERS ADDED				
04	330	FULL FAN CIRCUITRY ADDED				
05	345	R14 DELETED. R10, R12 + R13 VALUES CHANGED. R11 ? R13 GROUNDED.				
06	347	NOTE 2 ADDED SHT2 - JUMPER OPTION ADDED SHT 4 - R16 WAS JUMPER				

POWER AND GROUND TABLE				
IC No	TYPE	POWER	GROUND	QTY
U55	Am2964B	10	30	1
U91	FSC 9216B	8	4	1
U9-U17, U32-U36 U56-U64, U74-U82	2164A-20	8	16	36
U22-U24	FAL10L8	20	10	3
U73	PCLL-13XX	14	7	1
U47	8237A-5	31	20	1
U42	8087	40	1,20	1
U41	8088	40	1,20	1
U84	8253A-5	24	12	1
U43	8259A-5	28	14	1
U50	8272	40	20	1
U85	8284A	18	9	1
U18	8288	20	10	1
U48	2764A-3	28	14	1
U71	74LS161A	16	8	1
U52	74LS195 A	16	8	1
U95	74LS280	14	7	1
U96	74LS322A	20	10	1
U49	74LS670	16	8	1
U72, U85 U93	74LS175	16	8	3
U19-U21, U69	74LS373	20	10	4
U65	74LS30	14	7	1
U53	74LS00	14	7	1
U92	74LS02	14	7	1
U87, U90	74LS04	14	7	2
U26 U54 U84	74LS08	14	7	3
U7, U68, U89	74LS14	14	7	3
U46	74LS32	14	7	1
U23, U24, U27, U28, U30, U31, U33, U34	74LS74	14	7	8
U30, U84, U88	74LS125	14	7	3
U1-U5, U37, U88	74LS244	20	10	7
U6, U66	74LS245	20	10	2
U45	74ALS74	14	7	1
U25	LM386	6	4	1
U44	74ALS00	14	7	1
U8	74S04	14	7	1



SPARE GATES:



HIGHEST DESIGNATIONS USED														
BT	C	D	E	FL	J	G	R	AN	U	Y				
BT1	CB1	D8	E6	FL6	J6	Q13	R54	AN6	U56	Y1				
HIGHEST DESIGNATIONS NOT USED														
	C28	D1					R14							

NOTES:
1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, 1/4 W; CAPACITANCE VALUES ARE IN MICROFARADS.
2. SCHEMATIC 100004-000-06 IS TO BE USED WITH PWA 100004-000-06 AND PWB 200003-000-02 ONLY.

04	00	02	04	00	00	06	REV	SHEET
7	6	5	4	3	2	1	SHEET	INDEX

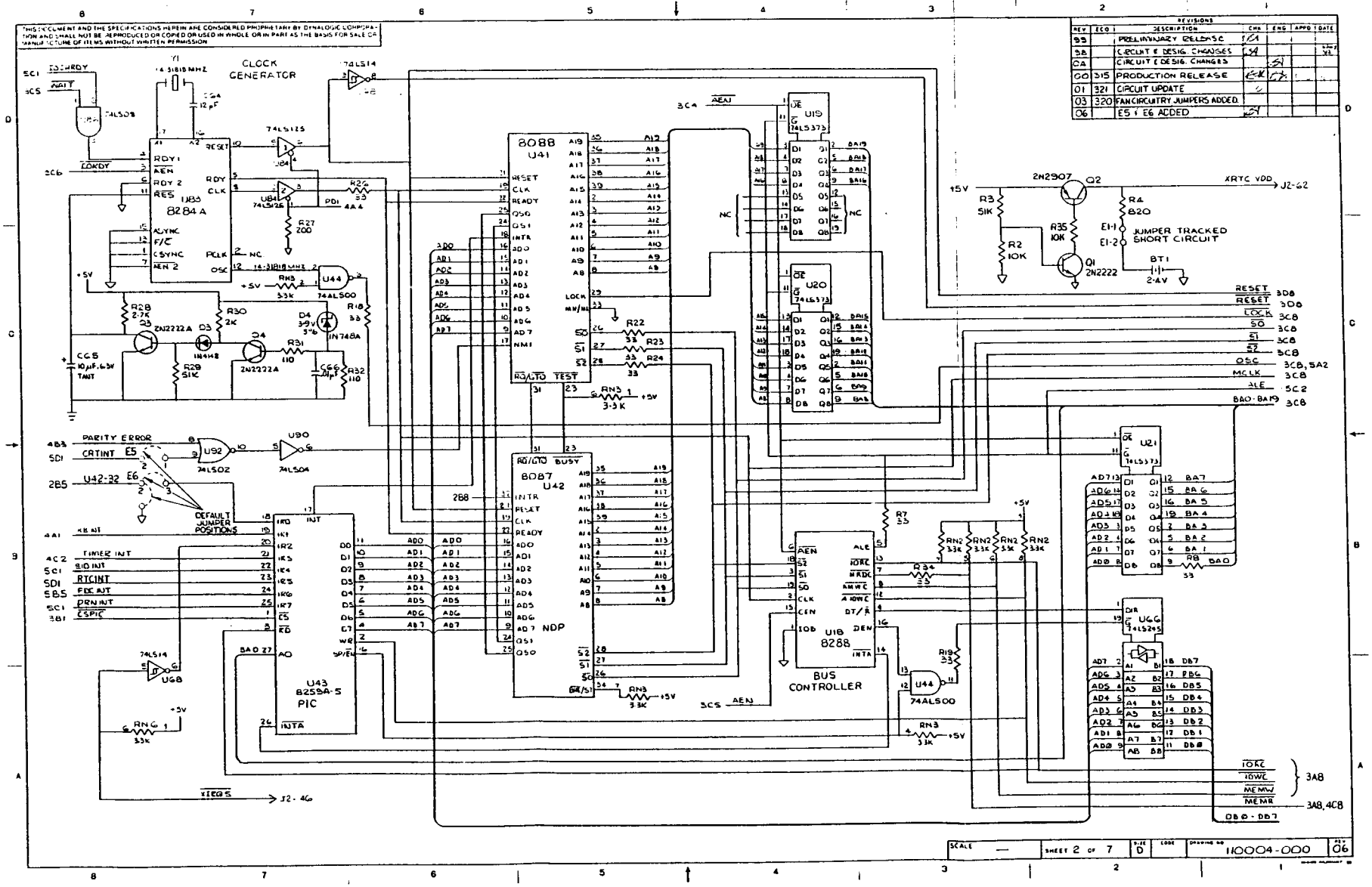
DRAWN	CL / KCK	SCALE	32
CHECKED			
ENGINEER			
APPROVED			
SHEET 1 OF 7		SIZE	D
		CODE	

Dynalogic Corporation
Ottawa – Canada

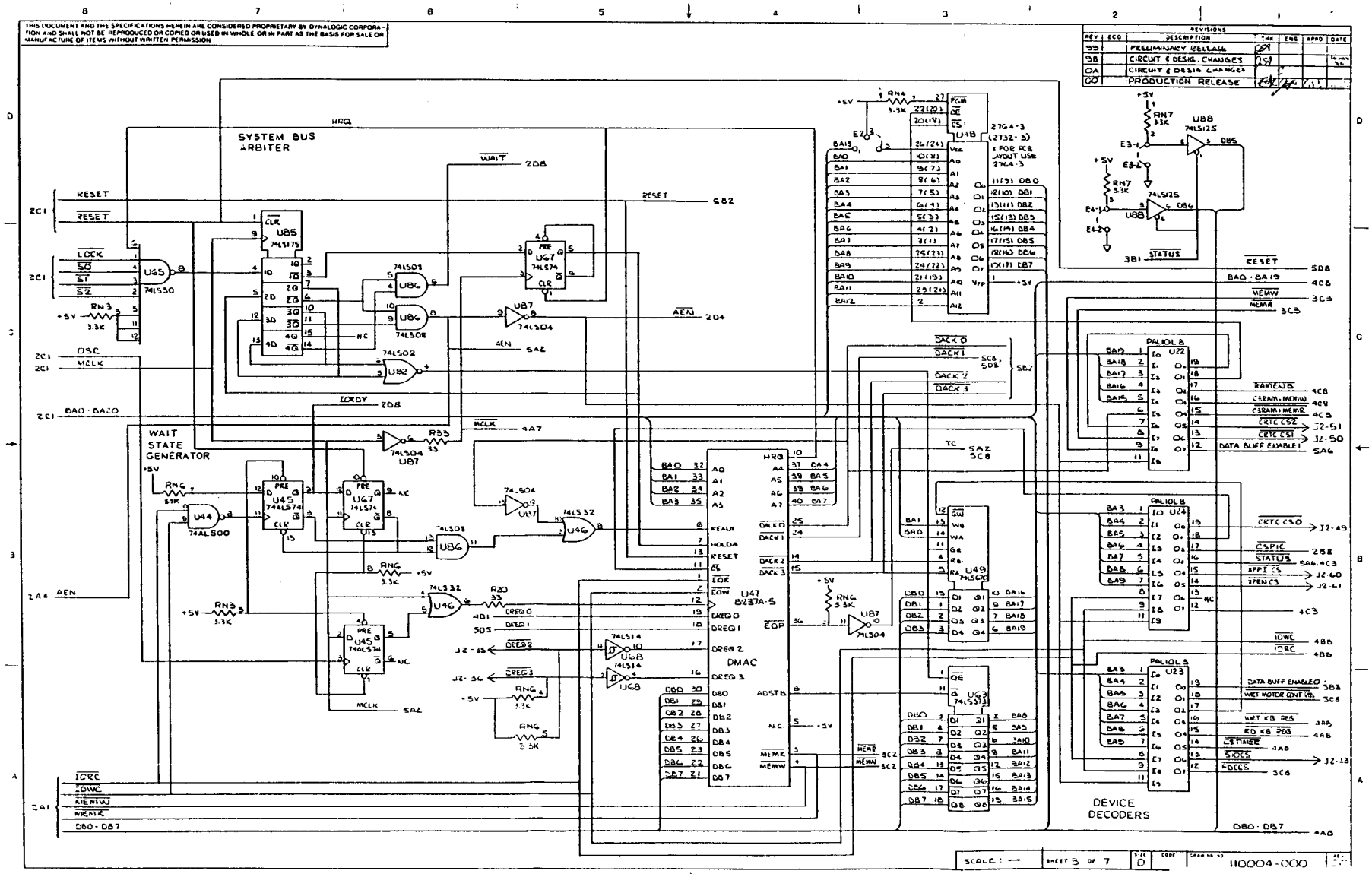
TITLE
SCHEMATIC DIAGRAM
SYSTEM CARD A6

DRAWING NO 110004-000 REV 06

100004-000 HYBRID
NEXT ASSY USED ON



REV	ECO #	DESCRIPTION	CHK	ENG	APPD	DATE
99		PRELIMINARY RELEASE				
5A		CIRCUIT & DESIG. CHANGES				
CA		CIRCUIT & DESIG. CHANGES				
00	315	PRODUCTION RELEASE				
01	321	CIRCUIT UPDATE				
03	320	FAN CIRCUITRY JUMPERS ADDED.				
06		E5 & E6 ADDED				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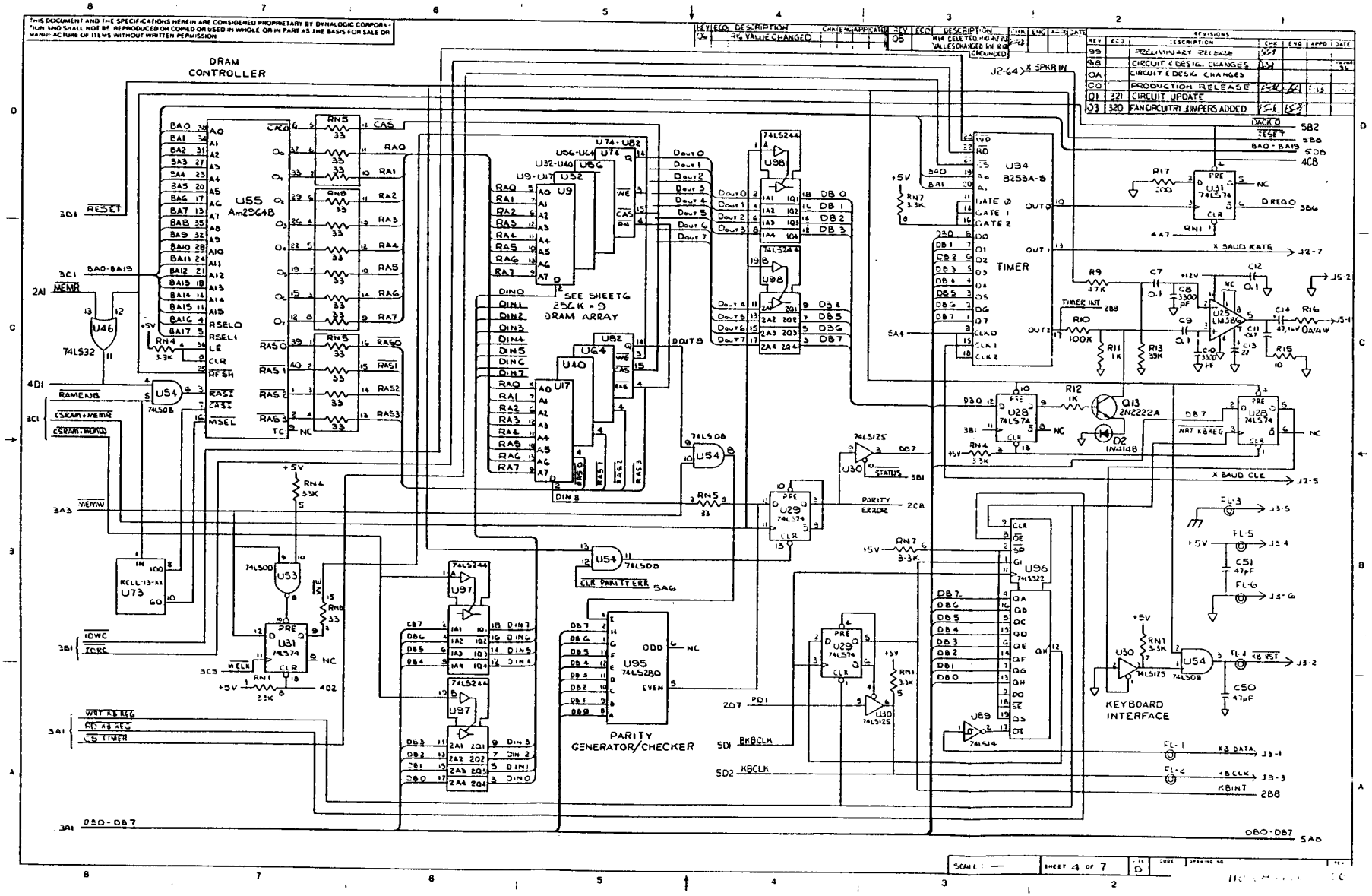
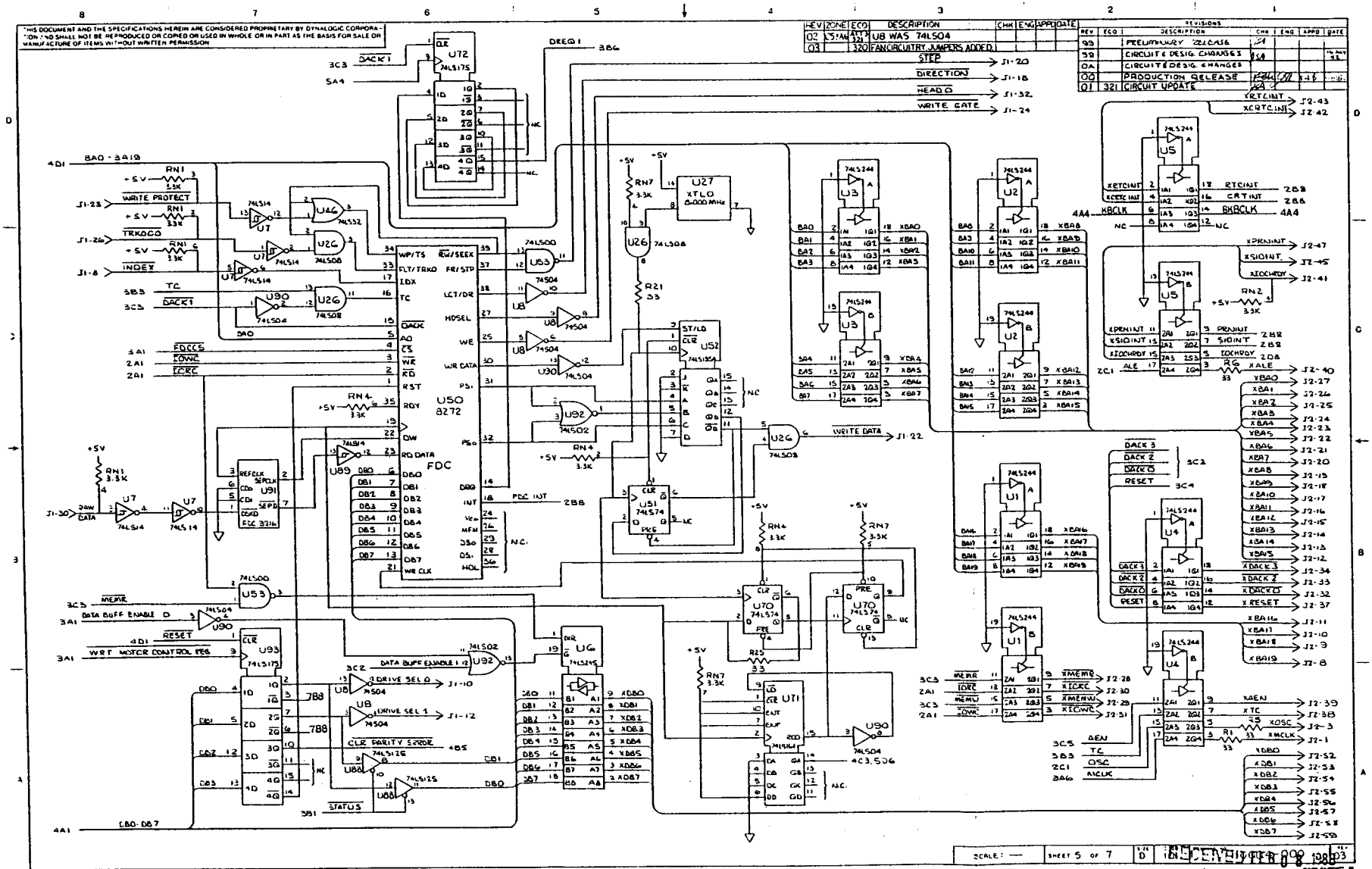
REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
55 | PRELIMINARY RELEASE
5B | CIRCUIT & DESIG. CHANGES
0A | CIRCUIT & DESIG CHANGES
00 | PRODUCTION RELEASE
SYSTEM BUS ARBITER
WAIT STATE GENERATOR
DMAC
U47 8237A-5
DEVICE DECODERS
PAL10L8
74LS245
74LS125
74LS175
74LS74
74LS08
74LS02
74LS04
74LS00
74LS32
74LS14
74LS373
2764-3 (2732-5)
RESET
HRQ
WAIT
AEN
RDY
MCLK
OSC
STATUS
110004-000
SCALE : —
SHEET 3 OF 7


DRAM CONTROLLER
U55 Am2964B
U46 74LS32
U54 74LS08
U73 RCLL-13-33
U53 74LS00
U31 74LS74
U97 74LS244
U95 74LS280 PARITY GENERATOR/CHECKER
U74-U82
U32-U40 U56-U64
U9-U17
SEE SHEET6 256K x 9 DRAM ARRAY
U34 8253A-5 TIMER
U31 74LS74
U25 LM386
U28 74LS74
U29 74LS74
U96 74LS322
U30 74LS125
U89 74LS14
KEYBOARD INTERFACE
Q13 2N2222A
D2 IN4148
RESET
MEMR
MEMW
RAMENB
CSRAM+MEMR
CSRAM+MEMW
IOWC
IORC
WRT KB REG
RD KB REG
CS TIMER
BA0-BA19
DB0-DB7
DOUT0-DOUT7
DIN0-DIN7
RA0-RA7
RAS0-RAS3
CAS
WE
RFSH
MSEL
RSEL0
RSEL1
PARITY ERROR
CLR PARITY ERR
PD1
SD1 KBCLK
SD2 KBCLK
KBINT
X SPKR IN
X BAUD RATE
X BAUD CLK
KB DATA
KB CLK
KB RST
DREQ0
TIMER INT
SCALE —
SHEET 4 OF 7
SIZE D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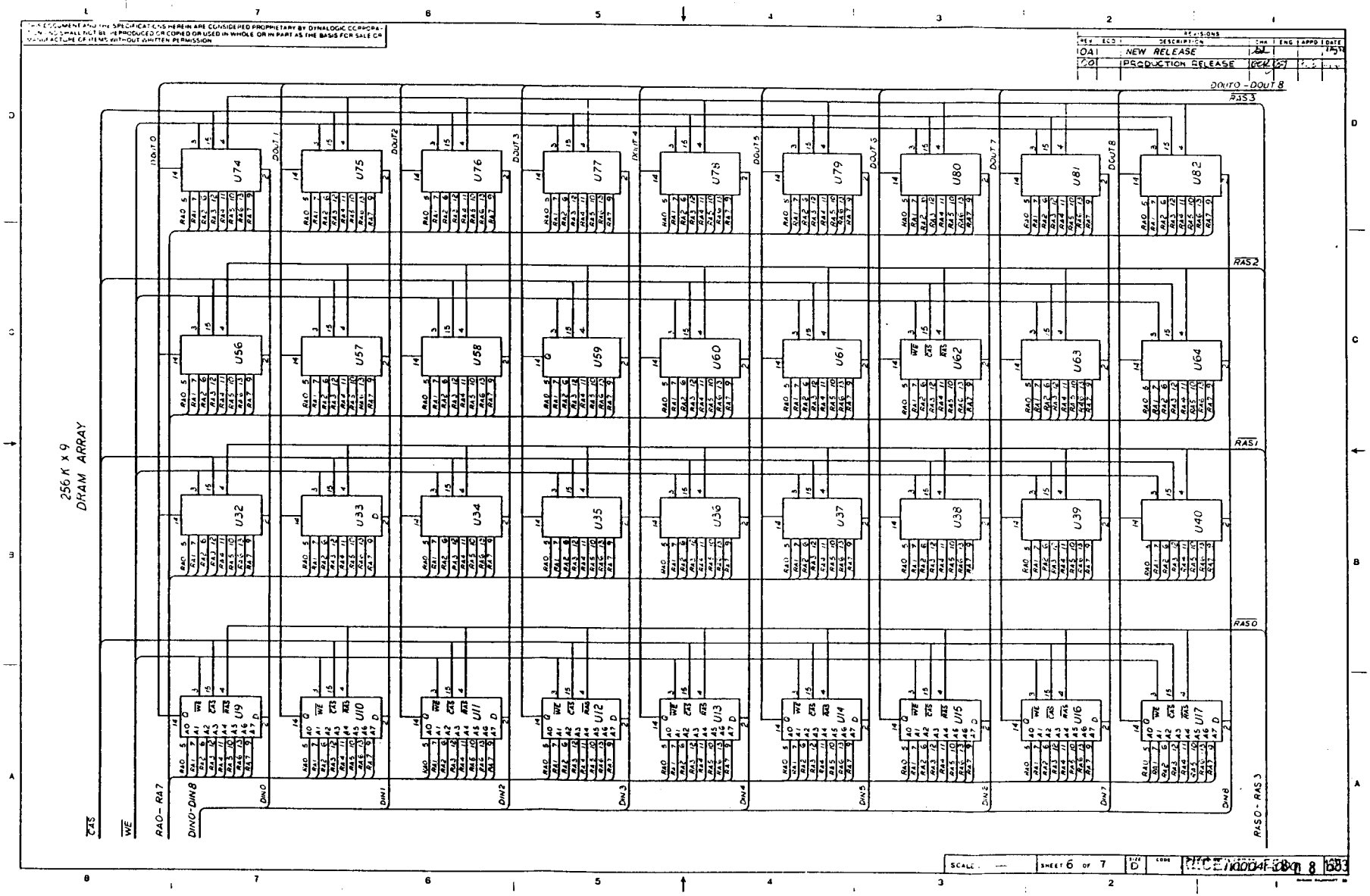
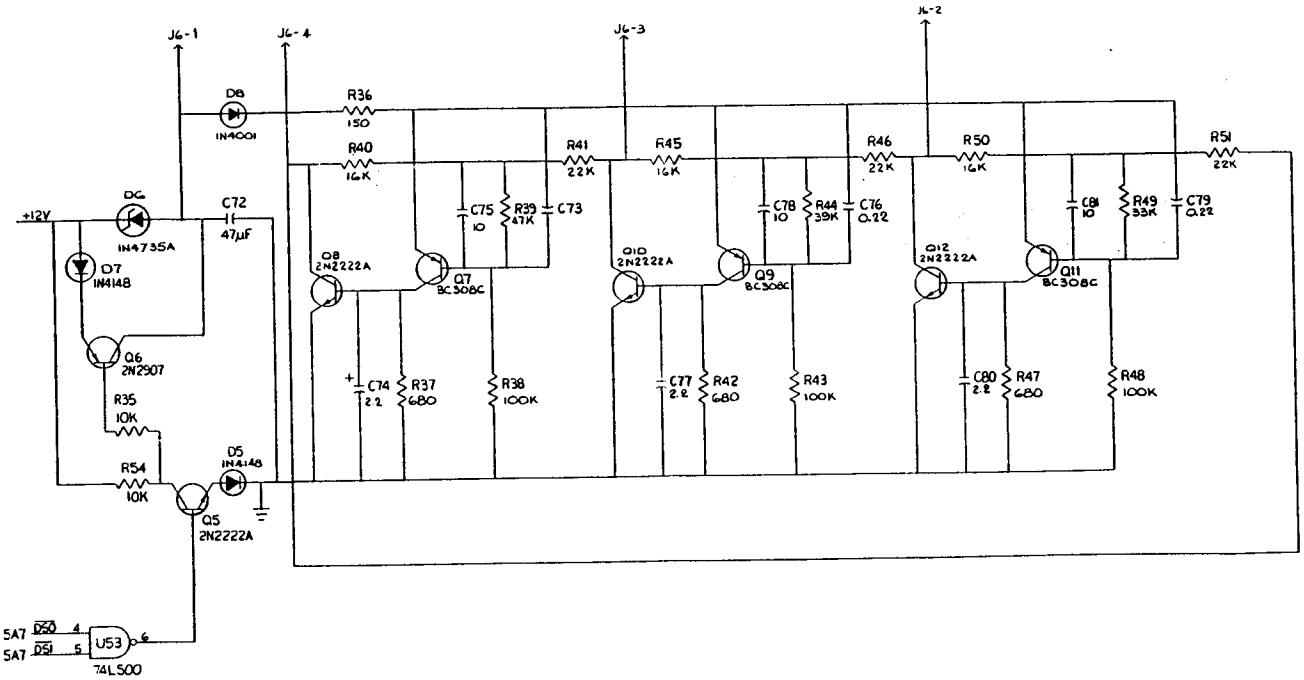
REV ZONE ECO DESCRIPTION CHK ENG APP DATE
02 321 U8 WAS 74LS04
03 320 FANCIRCUITRY JUMPERS ADDED
REVISIONS
99 PRELIMINARY 22 CASE
59 CIRCUIT DESIG. CHANGES
0A CIRCUIT DESIG. CHANGES
00 PRODUCTION RELEASE
01 321 CIRCUIT UPDATE
DREQ1
DACK1
STEP
DIRECTION
HEAD 0
WRITE GATE
XRTCINT
XCRTCINT
BA0 - BA19
WRITE PROTECT
TRK0CO
INDEX
TC
FDCCS
FDWR
FDRD
FDC 37C65
U50 8272 FDC
U72 74LS175
U27 XTLO 8.000 MHz
U26 74LS08A
U51 74LS74
U70 74LS74
U93 74LS175
U90 74LS04
U89 74LS14
U91 REFCLK SERCLK
U92 74LS02
U53 74LS00
U46 74LS32
U26 74LS08
U30 74LS04
U8 74LS04
U6 74LS245
U1 74LS244
U2 74LS244
U3 74LS244
U4 74LS244
U5 74LS244
U2G 74LS08
U52 74LS164
U71 74LS164
RN1 5.5K
RN2 3.3K
RN4 3.3K
RN7 3.3K
R21 33
R25 33
R1 33
R2 33
+5V
WE
WR DATA
RD DATA
WR CLK
INT
RST
RDY
DRQ
PS0
PS1
HDL
HDSEL
LCT/DR
FR/STP
FLT/TRK0
WP/TS
RW/SEEK
DRIVE SEL 0
DRIVE SEL 1
CLR PARITY ERROR
DATA BUFF ENABLE 0
DATA BUFF ENABLE 1
WRT MOTOR CONTROL REG
RESET
STATUS
FDC INT
WRITE DATA
ALE
RTCINT
CRTINT
KBCLK
KBRCLK
PRNINT
SIOINT
IOCHRDY
XALE
XBA0
XBA1
XBA2
XBA3
XBA4
XBA5
XBA6
XBA7
XBA8
XBA9
XBA10
XBA11
XBA12
XBA13
XBA14
XBA15
XBA16
XBA17
XBA18
XBA19
XDACK3
XDACK2
XDACK0
XRESET
XMEMR
XIOWC
XMEMW
XIORC
XAEN
XTC
XOSC
XMCLK
XDB0
XDB1
XDB2
XDB3
XDB4
XDB5
XDB6
XDB7
SCALE: —
SHEET 5 OF 7
SIZE D
DYNALOGIC CORP. 800 1988
REV 03



REVISIONS					
REV	ECO	DESCRIPTION	CHK	ENG APPD	DATE
01		NEW RELEASE			
02		PRODUCTION RELEASE			

SCALE: — SHEET 6 OF 7 SIZE D CODE DWG NO 10004-080 B REV 8

REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
04	330	FULL FAN CIRCUITRY ADDED.				

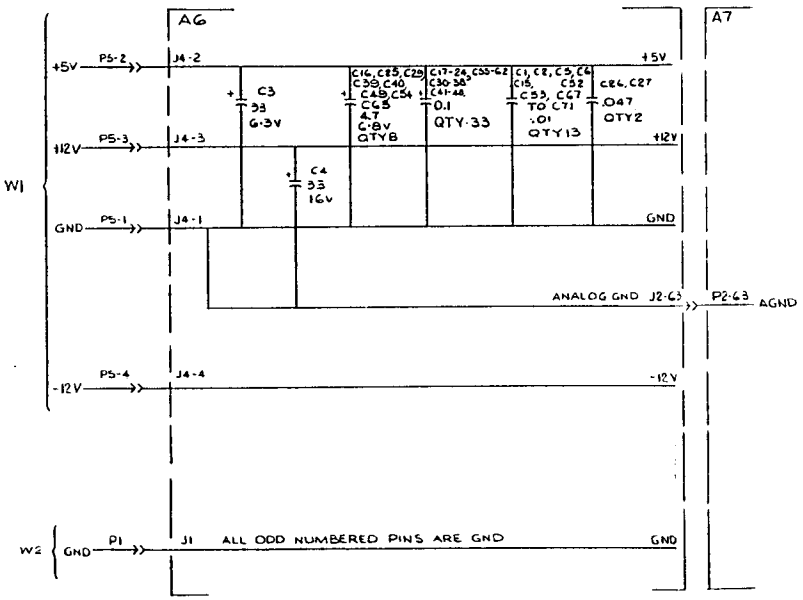


SCALE	SHEET 7 OF 7	SIZE D	CODE	DRAWING NO 110004-000	REV 04

7.3 System Board Rev 12

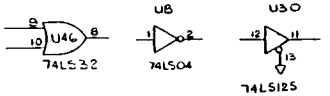
POWER AND GROUND TABLE

IC No	TYPE	POWER	GROUND	QTY
U55	Am2964B	10	30	1
U91	FDC9216B	8	4	1
U9-U17, U52-U60 U56-U64, U74-U82	2164A-20	8	16	36
U22-U24	PAL10L8	20	10	3
U73	PCLL-13XX	14	7	1
U47	8237A-5	31	20	1
U42	8087	40	1,20	1
U41	8088	40	1, 20	1
U94	8253A-5	24	12	1
U43	8259A-5	28	14	1
U50	8272	40	20	1
U83	8284A	18	9	1
U18	8288	20	10	1
U48	2764A-3	28	14	1
U71	74LS161A	16	8	1
U52	74LS135 A	16	8	1
U95	74LS280	14	7	1
U96	74LS322A	20	10	1
U49	74LS670	16	8	1
U72 U85 U93	74LS175	16	8	3
U19-U21, U69	74LS373	20	10	4
U65	74LS30	14	7	1
U53	74LS00	14	7	1
U92	74LS02	14	7	1
U87, U90	74LS04	14	7	2
U26 U54 U84	74LS08	14	7	3
U7 U68, U89	74LS14	14	7	3
U46	74LS32	14	7	1
U100	74LS393	14	7	1
U30, U84, U88	74LS125	14	7	3
U1-U5, U97, U98	74LS244	20	10	7
U6, U66	74LS245	20	10	2
U45	74ALS74	14	7	1
U25	LM386	6	4	1
U44	74ALS00	14	7	1
U8	74S04	14	7	1
U28 U29 U31 U50 U70 U67 U59	74LS74	14	7	7



REV	ECO	DESCRIPTION	CHK	ENG	APPR	DATE
99		PRELIMINARY RELEASE	KK			
9B		CIRCUIT & DESIG. CHANGES	KK			9-01-82
0A		CIRCUIT & DESIG. CHANGES		KK		
00	315	PRODUCTION RELEASE	KK	KK		
01	321	CIRCUIT UPDATE	KK			
02	ATT3 321	SHT 5 ZONE C5 : A6 U8 WAS 74LS04	KK			
03	320	FAN CIRCUITRY JUMPERS ADDED	KK			
04	330	FULL FAN CIRCUITRY ADDED				
05	345	R14 DELETED. R10, R12 : R13 VALUES CHANGED. R11 : R13 GROUNDED.	KK			
06	347	NOTE 2 ADDED SHT 2 - JUMPER OPTION ADDED SHT 4 - R16 WAS JUMPER	KK			4-18-83
07	373	SHT 1 - R53 ADDED TO NOT USED COLUMN SHT 2 - RESISTOR BETWEEN Q2-BASE : Q1-COLLECTOR WAS R35				
08	382	ADDED JUMPER FROM E5-1 TO E6-3		DSA		
10	393	ADDED U85 (U100 UPDATED CIRCUITRY	KK	DSA		7-11-83
11	435	SHT 2, B2, 7 JUMPER DESIGNATIONS SHEET 2 E5 TO E6 JUMPER	KK	DSA	KK	9-29-83
12	461	C8, C10 CHANGED	KK			

SPARE GATES



HIGHEST DESIGNATIONS USED													
BT	C	D	E	FL	J	C	R	RN	U	Y			
BT1	C81	D8	E6	FL6	J6	Q13	R50	RN8	U100	Y1			
HIGHEST DESIGNATIONS NOT USED													
	C28	D1 D2 D5 D7	E4 E5				Q5 Q6	R14 R33 R35 R54 R12					

NOTES:
1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, 1/4 W; CAPACITANCE VALUES ARE IN MICROFARADS.
2. SCHEMATIC 110004-000-12 IS TO BE USED WITH PWA 100004-000-12 AND PWB DRAWING 100003-000-04. (BOARD REV IS STILL AT 03).

11	10	11	10	10	11	12	REV	SHEET
7	6	5	4	3	2	1	SHEET	INDEX

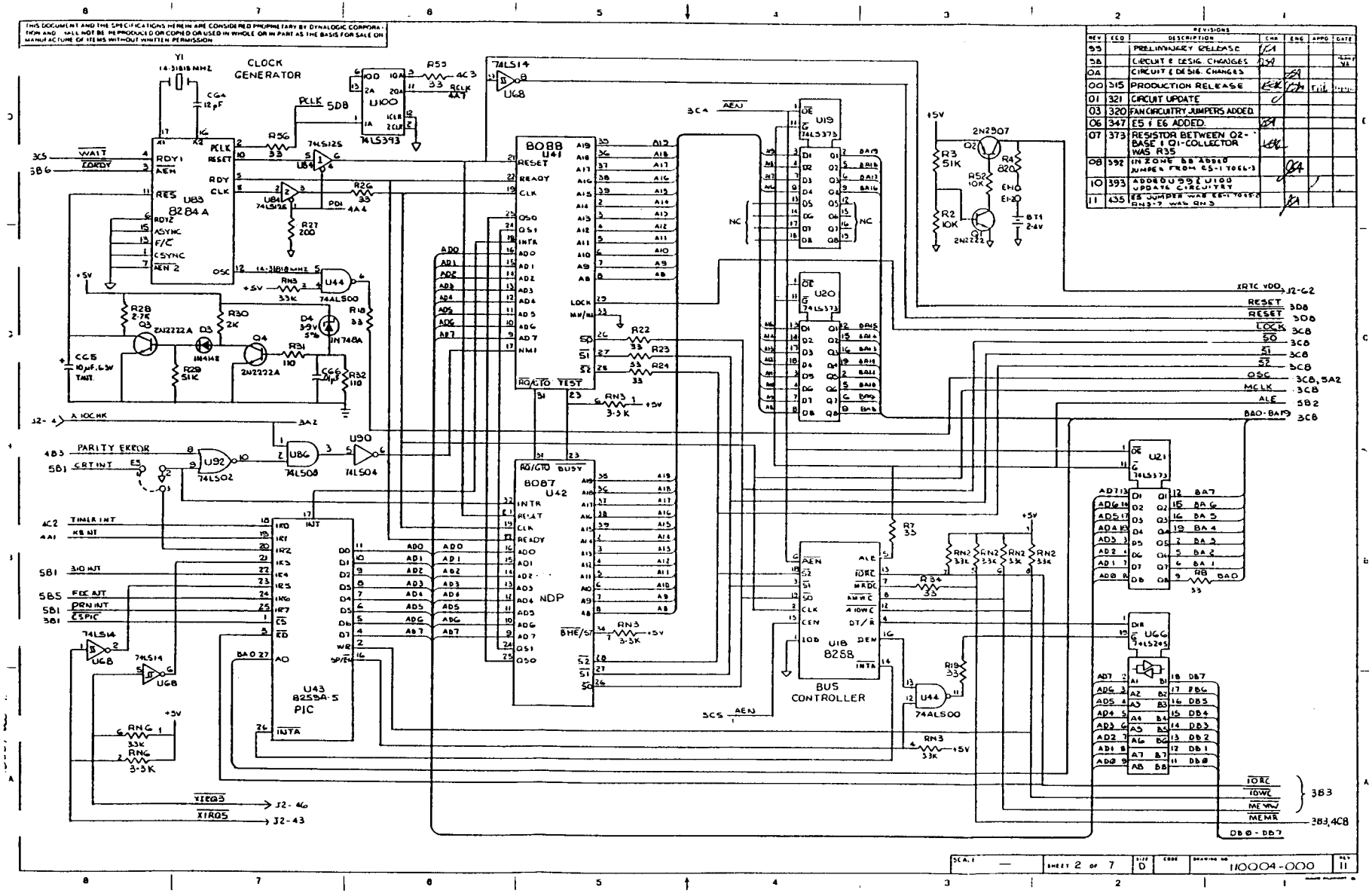
Dynalogic Corporation
Ottawa – Canada

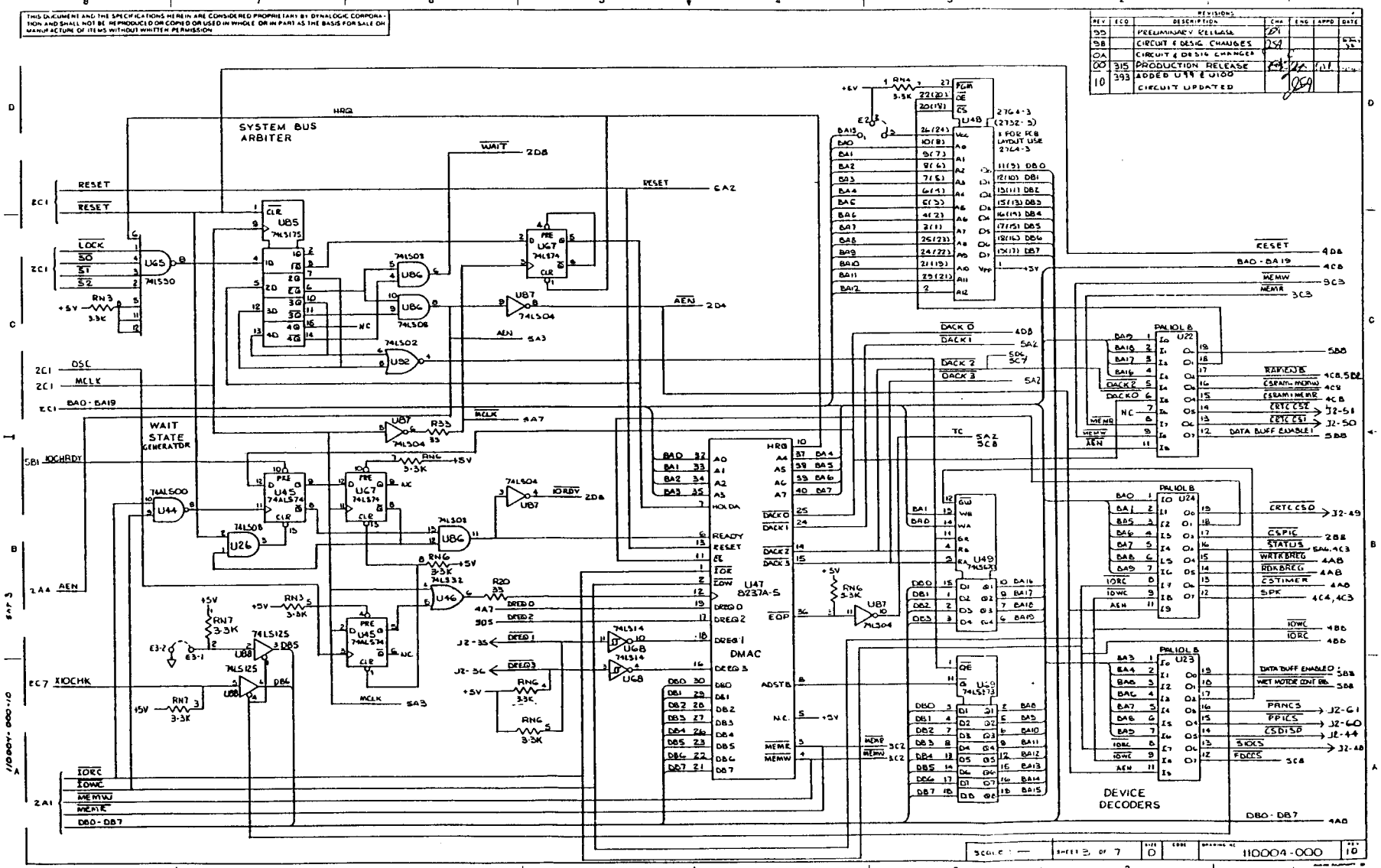
TITLE: SCHEMATIC DIAGRAM SYSTEM CARD A6

DRAWN: G.L./K.K.K. 9-01-82
CHECKED: 82-09-29
ENGINEER: 82-09-29
APPROVED: 82-09-29
MFG/QUAL: 82-09-29
INITIAL APPLICATION

SIZE: D
CODE:
DRAWING NO: 110004-000
REV: 12
SHEET 1 OF 7

100004-000 MYPLE/DW
NEXT ASSY: USED ON


CLOCK GENERATOR
8088 U41
8284A U83
8087 U42
NDP
8259A-5 PIC U43
8288 BUS CONTROLLER U18
74LS373 U19
74LS373 U20
74LS373 U21
74LS245 U66
74LS393 U100
74LS125 U84
74LS14 U68
74LS02 U92
74LS08 U86
74LS04 U90
74ALS00 U44
2N2907 Q2
2N2222 Q1
2N2222A Q3
2N2222A Q4
1N4148 D3
1N4148 D4
PARITY ERROR
CRT INT
TIMER INT
KB INT
FDC INT
DRN INT
ESPIC
WAIT
READY
RESET
RCLK
PCLK
AEN
LOCK
ALE
DEN
DT/R
BUS CONTROLLER
XIRQ3
XIRQ5
XRTC VDD
RESET
LOCK
OSC
MCLK
ALE
BA0-BA19
DB0-DB7
IORC
IOWC
MEMW
MEMR
REVISIONS
REV ECO DESCRIPTION CHK ENG APPD DATE
99 PRELIMINARY RELEASE
5A CIRCUIT & DESIG. CHANGES
0A CIRCUIT & DESIG. CHANGES
00 315 PRODUCTION RELEASE
01 321 CIRCUIT UPDATE
03 320 FAN CIRCUITRY JUMPERS ADDED
06 347 E5 & E6 ADDED.
07 373 RESISTOR BETWEEN Q2-BASE & Q1-COLLECTOR WAS R35
08 392 IN ZONE 8B ADDED JUMPER FROM E5-1 TO E6-3
10 393 ADDED U99 & U100 UPDATE CIRCUITRY
11 435 E5 JUMPER WAS ECO'D TO E6 RN3-7 WAS ON 3
SCALE — SHEET 2 OF 7 SIZE D DRAWING NO 10004-000 REV 11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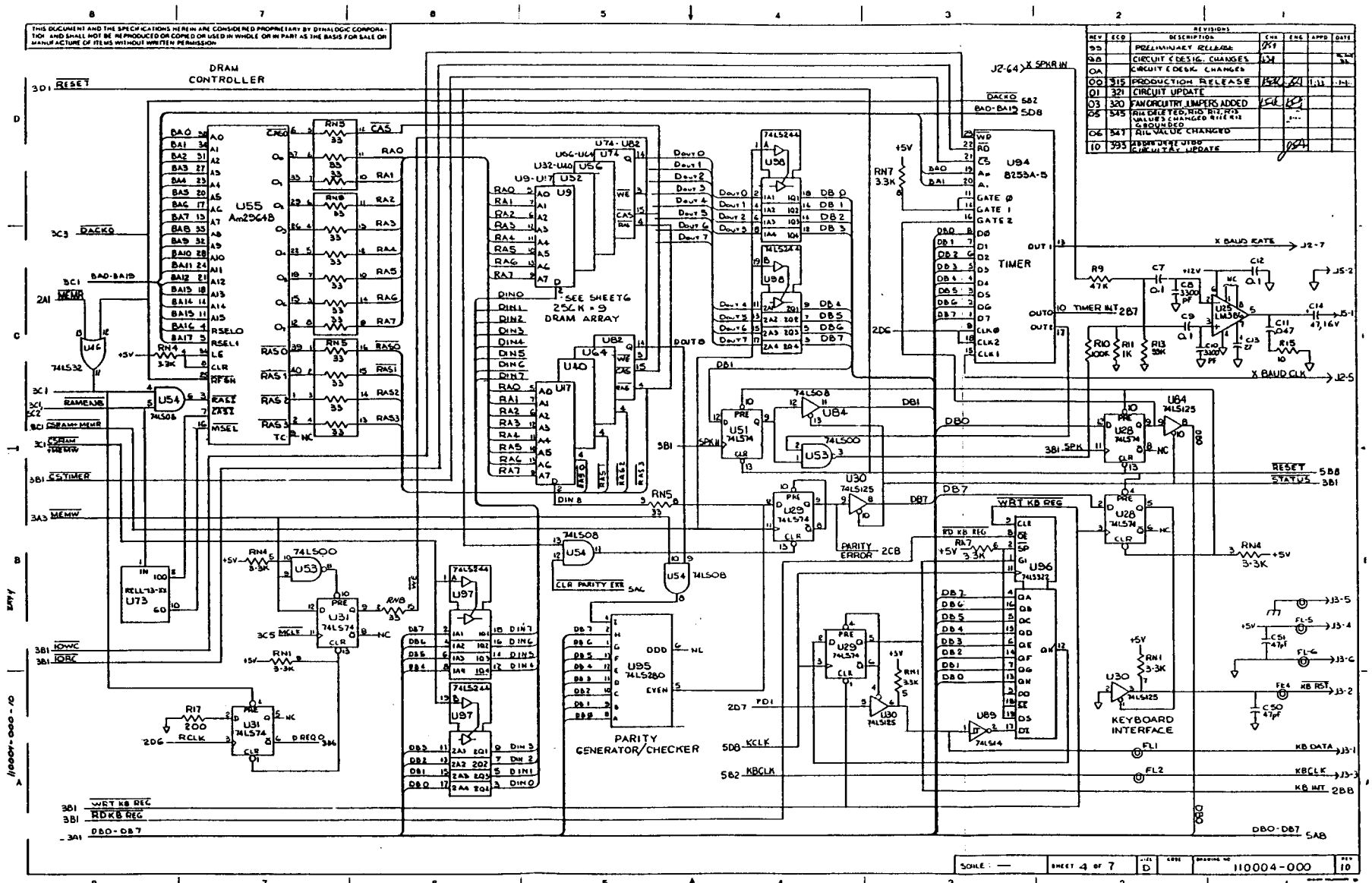
REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
55 | | PRELIMINARY RELEASE
58 | | CIRCUIT & DESIG CHANGES
OA | | CIRCUIT & DESIG CHANGES
00 | 315 | PRODUCTION RELEASE
10 | 393 | ADDED U99 & U100 CIRCUIT UPDATED
SYSTEM BUS ARBITER
WAIT STATE GENERATOR
DEVICE DECODERS
DMAC 8237A-5
HRQ
RESET
WAIT
AEN
MCLK
OSC
IOCHRDY
IOCHK
BA0 - BA19
DB0 - DB7
IORC
IOWC
MEMW
MEMR
DACK 0
DACK 1
DACK 2
DACK 3
TC
READY
HOLDA
EOP
ADSTB
DREQ 0
DREQ 1
DREQ 2
DREQ 3
U85
U86
U87
U88
U44
U45
U46
U47
U48
U49
U22
U23
U24
U26
U67
U82
RN3
RN4
RN6
RN7
R20
R33
RNG
74LS175
74LS374
74LS08
74LS02
74LS04
74LS32
74LS50
74LS125
74LS138
74LS244
74LS273
74LS373
74LS514
27C64-3
(27C32-5)
PALIOL8
SCALE: —
SHEET 3 OF 7
SIZE D
DRAWING NO 110004-000
REV 10


DRAM CONTROLLER
U55 Am2964B
U74-U82
U9-U17
U32-U40
U56-U64
SEE SHEET 6 25CK-9 DRAM ARRAY
U94 8259A-5
TIMER
U25 LM380
U96
KEYBOARD INTERFACE
PARITY GENERATOR/CHECKER
U95 74LS280
U73 RELL-73-103
U97
U87
U89
U30 74LS125
U64 74LS125
U54 74LS08
U53 74LS00
U84 74LS08
U51 74LS74
U28 74LS74
U29 74LS74
U31 74LS74
U13 74LS74
RN1 3.3K
RN4 3.3K
RN5 33
RN7 3.3K
RN8 33
R9 47K
R10 500K
R11 1K
R13 33K
R15 10
R17 200
C7 0.1
C8 3300 pf
C9 0.1
C11 .047
C12 0.1
C13 27
C14 47,16V
C50 47pf
C51 47pf
J2-64 X SPKR IN
X BAUD RATE J2-7
X BAUD CLK J2-5
J5-2
J5-1
J3-5
J3-4
J3-6
J3-2
J3-1
J3-3
RESET 5B8
STATUS 3B1
KB RST
KB DATA
KBCLK
KB INT 2B8
DB0-DB7 5A8
WRT KB REG
RD KB REG
PARITY ERROR 2C8
CLR PARITY ERR 5A6
DACK0 582
BA0-BA15 5D8
RESET 3D1
DACK0 3C3
BA0-BA15 3C1
MEMR 2A1
RAMENJB 3C1
DRAM MEMR 3C1
DRAM MEMW 3C1
CSTIMER 3B1
MEMW 3A3
IOWC 3B1
IORC 3B1
WRT KB REG 3B1
RDKB REG 3B1
DB0-DB7 3A1
MCLK 3C5
RCLK 2D6
DREQ0 3B6
FDI 2D7
KCLK 5D8
KBCLK 582
TIMER INT 2B7
SPK 3B1
FL1
FL2
FE4
FL-5
FL-6
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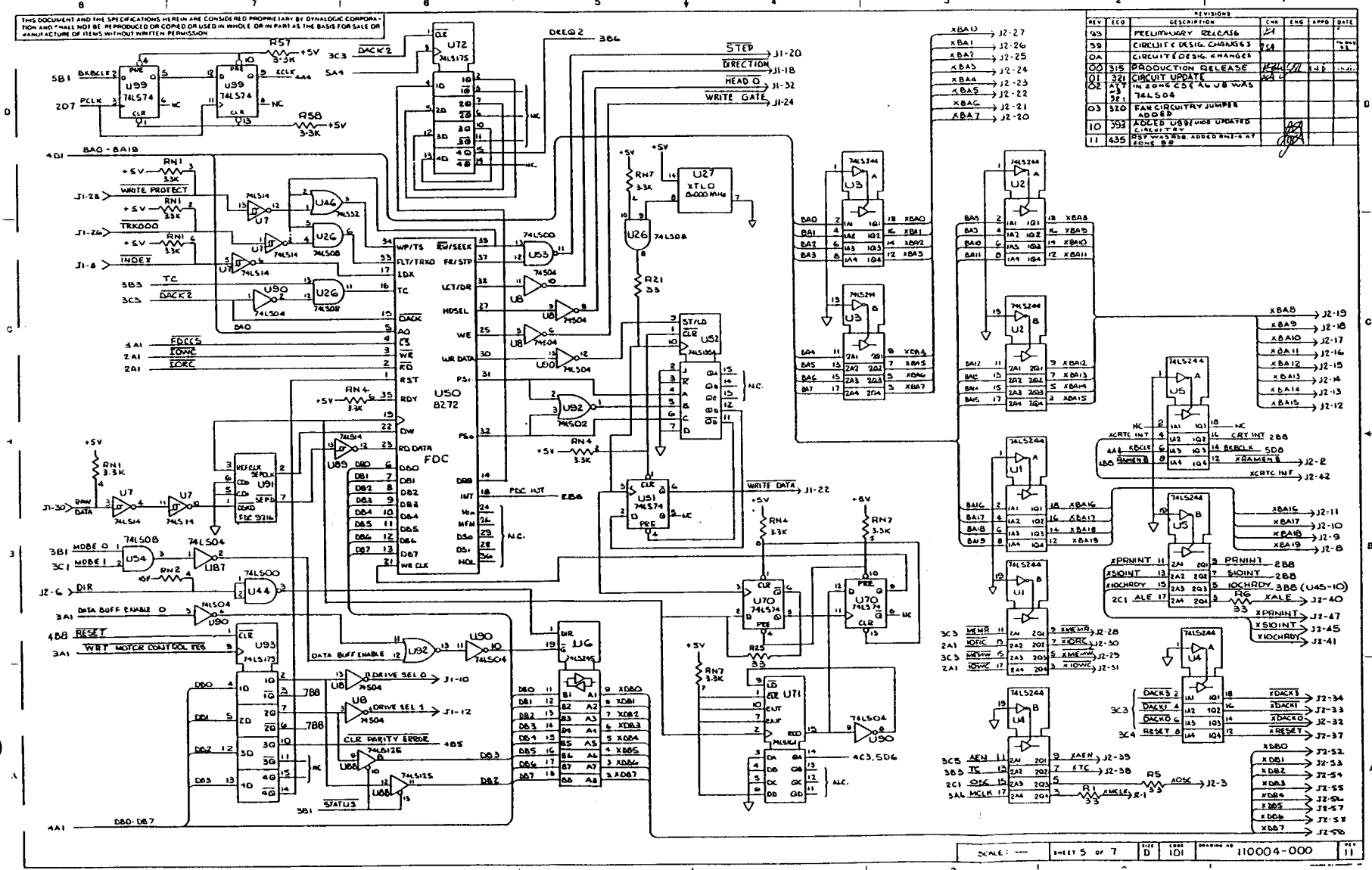
REVISIONS
REV ECO DESCRIPTION CHK ENG APPD DATE
99 PRELIMINARY RELEASE
AB CIRCUIT DESIG. CHANGES
OA CIRCUIT DESIGN CHANGES
00 315 PRODUCTION RELEASE
01 321 CIRCUIT UPDATE
03 320 FAN CIRCUITRY JUMPERS ADDED
05 345 R14 DELETED, R10, R12, R15 VALUES CHANGED R16 R18 GROUNDED
06 347 R15 VALUE CHANGED
10 393 ADDED DRAM CIRCUITRY UPDATE
SCALE: — SHEET 4 OF 7 SIZE D CODE DRAWING NO 110004-000 REV 10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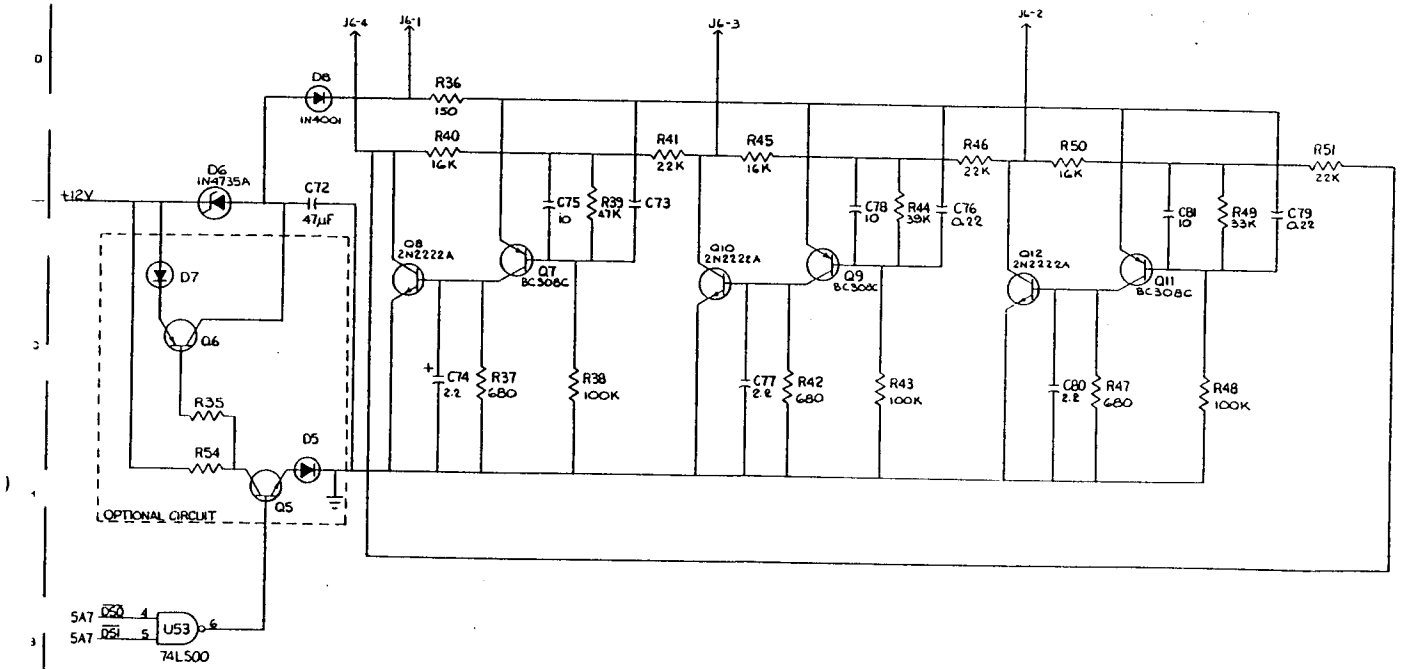
REVISIONS
REV ECO DESCRIPTION CHK ENG APPD DATE
93 PRELIMINARY RELEASE
99 CIRCUITS DESIG. CHANGES
OA CIRCUITS DESIG. CHANGES
00 315 PRODUCTION RELEASE
01 321 CIRCUIT UPDATE
02 327 IN ZONE C5F A6 U8 WAS 74LS04
03 320 FAN CIRCUITRY JUMPER ADDED
10 393 ADDED U89 U108 UPDATED CIRCUITRY
11 435 R27 WAS 8SR, ADDED RN7-4 AT ZONE B8
U50 8272 FDC
U72 74LS175
U99 74LS74
U26 74LS08
U27 XTLO 8.000 MHz
U50 74LS00
U8 74S04
U90 74LS04
U92 74LS02
U52 74LS164
U51 74LS74
U70 74LS74
U71 74LS161
U93 74LS175
U94 74LS125
U1 74LS244
U2 74LS244
U3 74LS244
U4 74LS244
U5 74LS244
U6 74LS245
U87 74LS04
U89 74LS14
U91 FDC 9216
RN1 3.3K
RN2 4.7K
RN4 3.3K
RN7 3.3K
R21 33
R25 33
R26 33
R27 33
R5 33
RST 3.3K
RS8 3.3K
PCLK
DACK2
STEP
DIRECTION
HEAD 0
WRITE GATE
WRITE DATA
FDC INT
WRITE PROTECT
TRK000
INDEX
TC
DIR
RESET
WRT MOTOR CONTROL RES
DRIVE SEL 0
DRIVE SEL 1
CLR PARITY ERROR
STATUS
DB0-DB7
BA0-BA19
XBA0 J2-27
XBA1 J2-26
XBA2 J2-25
XBA3 J2-24
XBA4 J2-23
XBA5 J2-22
XBA6 J2-21
XBA7 J2-20
XBA8 J2-19
XBA9 J2-18
XBA10 J2-17
XBA11 J2-16
XBA12 J2-15
XBA13 J2-14
XBA14 J2-13
XBA15 J2-12
XBA16 J2-11
XBA17 J2-10
XBA18 J2-9
XBA19 J2-8
XCRTC INT J2-42
XPRINT J2-47
XSIOINT J2-45
XIOCHRDY J2-41
XALE J2-40
XDACK3 J2-34
XDACK1 J2-33
XDACK0 J2-32
XRESET J2-37
XDB0 J2-52
XDB1 J2-53
XDB2 J2-54
XDB3 J2-55
XDB4 J2-56
XDB5 J2-57
XDB6 J2-58
XDB7 J2-59
SCALE: —
SHEET 5 OF 7
SIZE D
CODE 101
DRAWING NO 110004-000
REV 11

256 K x 9
DRAM ARRAY
RAS0 - RAS3
DIN0-DIN8
DOUT0-DOUT8
RA0-RA7
WE
CAS
110004-000
SHEET 6 OF 7
SCALE: —

REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
04	330	FULL FAN CIRCUITRY ADDED				
10	393	PART OF CIRCUIT DESIGNATED "OPTIONAL"				
11	435	J6-1 WAS CONNECTED TO ANODE OF D8				

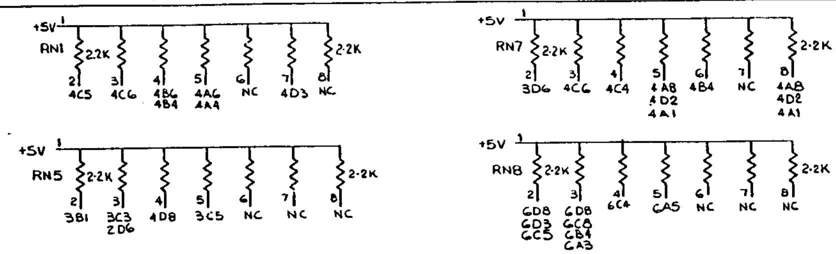


SCALE	SHEET 7 OF 7	SIZE D	CODE	DRAWING NO 110004-000	REV 11

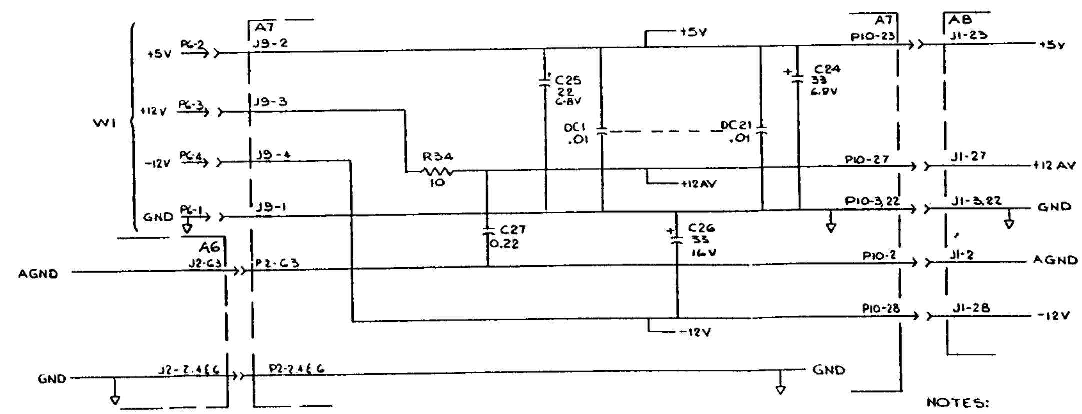
7.4 Display and I/O Board Rev 03

DIGITAL POWER AND GROUND TABLE

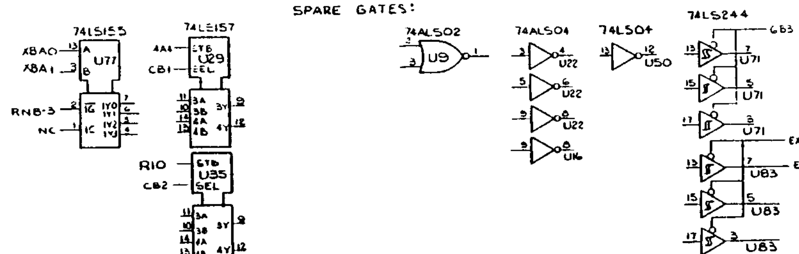
IC No	TYPE	POWER +5	POWER +12AV	POWER -12	GND	QTY
U9	74ALS02	14			7	1
U16, U22	74ALS04	14			7	2
U50	74LS04	14			7	1
U23, U45, U48, U51-U55, U67	74LS08	14			7	7
U5	74LS14	14			7	1
U65	74LS30	14			7	1
U24, U33	74ALS32	14			7	2
U32, U34, U61, U63	74LS32	14			7	4
U1, U8, U16-U20, U28, U85	74ALS74	14			7	7
U2, U17, U36, U37, U54, U64	74LS74	14			7	6
U38	74LS139	16			8	1
U13	74LS153	16			8	1
U77	74LS155	14			7	1
U29, U35	74LS157	16			8	2
U15, U31	74LS166	16			8	2
U78	74LS174	16			8	1
U46, U47, U66, U71, U79-U83, U73, U86-U88, U74	74LS244	20			10	14
U30, U59, U72, U85	74LS245	20			10	4
U60	74LS273	20			10	1
U2	74LS283	16			8	1
U14, U43, U44, U84	74LS374	20			10	4
U62	74ALS574	20			10	1
U76	75175	16			8	1
U3	2732A	24			12	1
U4	8255A-5	26			7	1
U21	8021-003	12			17	1
U75	CRT 9007	21			40	1
U25	PAL10L8	20			10	1
U10	PAL16L8	20			10	1
U26, U27, U39-U42, U55-U58	HM6116-3	24			12	10
U11	#SN5832IRS				8	1
U69, U68	µA9636A		8		4	2
U70	Z80A SIO/O	9			31	1
U6	PAL10H8	20			10	1
U12	XTLO	14			7	1



HIGHEST DESIGNATIONS USED												
C	D	DC	E	J	K	P	Q	R	RN	U	Y
C31	D7	D21	E3	J9	K1	P11	Q3	R34	RN8	U88	Y1
HIGHEST DESIGNATIONS NOT USED											
C5-C8											



SPARE GATES:



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, 1/4 W: CAPACITANCE VALUES ARE IN MICROFARADS (µF).
2. CIRCUIT COMPONENTS SHOWING THE SYMBOLS * OR ** ARE COMMON TO THE SAME IC PACKAGE.

REVISIONS

REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
99		PRELIMINARY RELEASE				
98		CIRCUIT & DESIG. CHANGES				
0A		CIRCUIT & DESIG CHANGES				
00	316	PRODUCTION RELEASE				
01	322	CIRCUIT UPDATE				
02	ATTI 322	ON SHT6 ZONE D2 DEL. C5-C8				
03	323	USED SPARE GATE U8 SHT 2 ZONE DC & U5 SHT 6 ZONE C2				
03	ATTI 323	IN ZONE A3 SHEET 6 USED SPARE U78 PIN 14 & 15				

REV	01	03	03	01	03	03	03
SHEET	7	6	5	4	3	2	1

NEXT ASS'Y	USED ON
100005-000	HYPERION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DRAWN: G. LEVEILLE, 29 MAY 1981

CHECKED: J.C. SULLIVAN

ENGINEER: J.C. SULLIVAN

SCALE: —

SHEET 1 OF 7

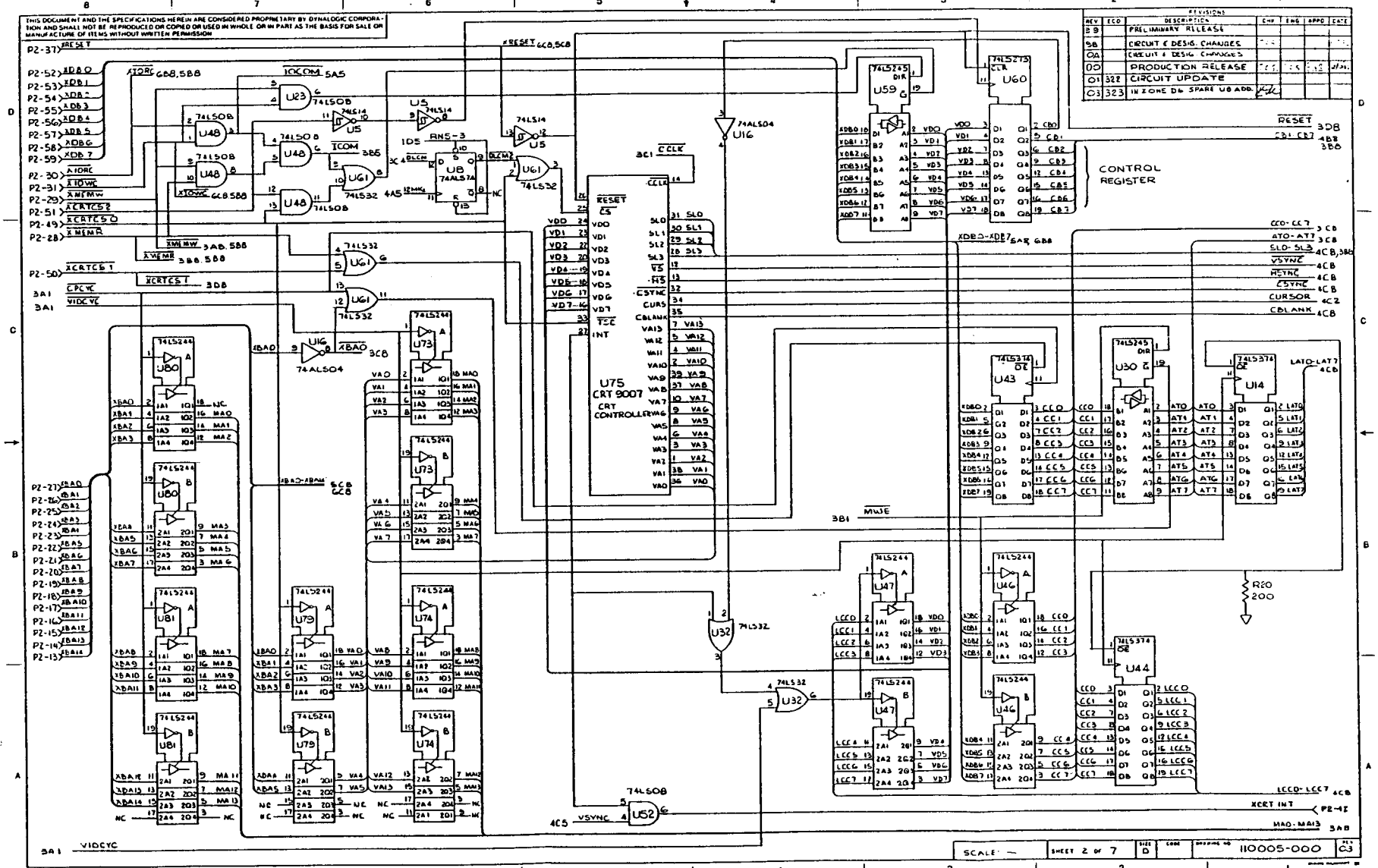
SIZE: D

Dynalogic Corporation
Ottawa – Canada

TITLE: DISPLAY AND I/O CARD - A7

DRAWING NO: 110005-000

REV: 03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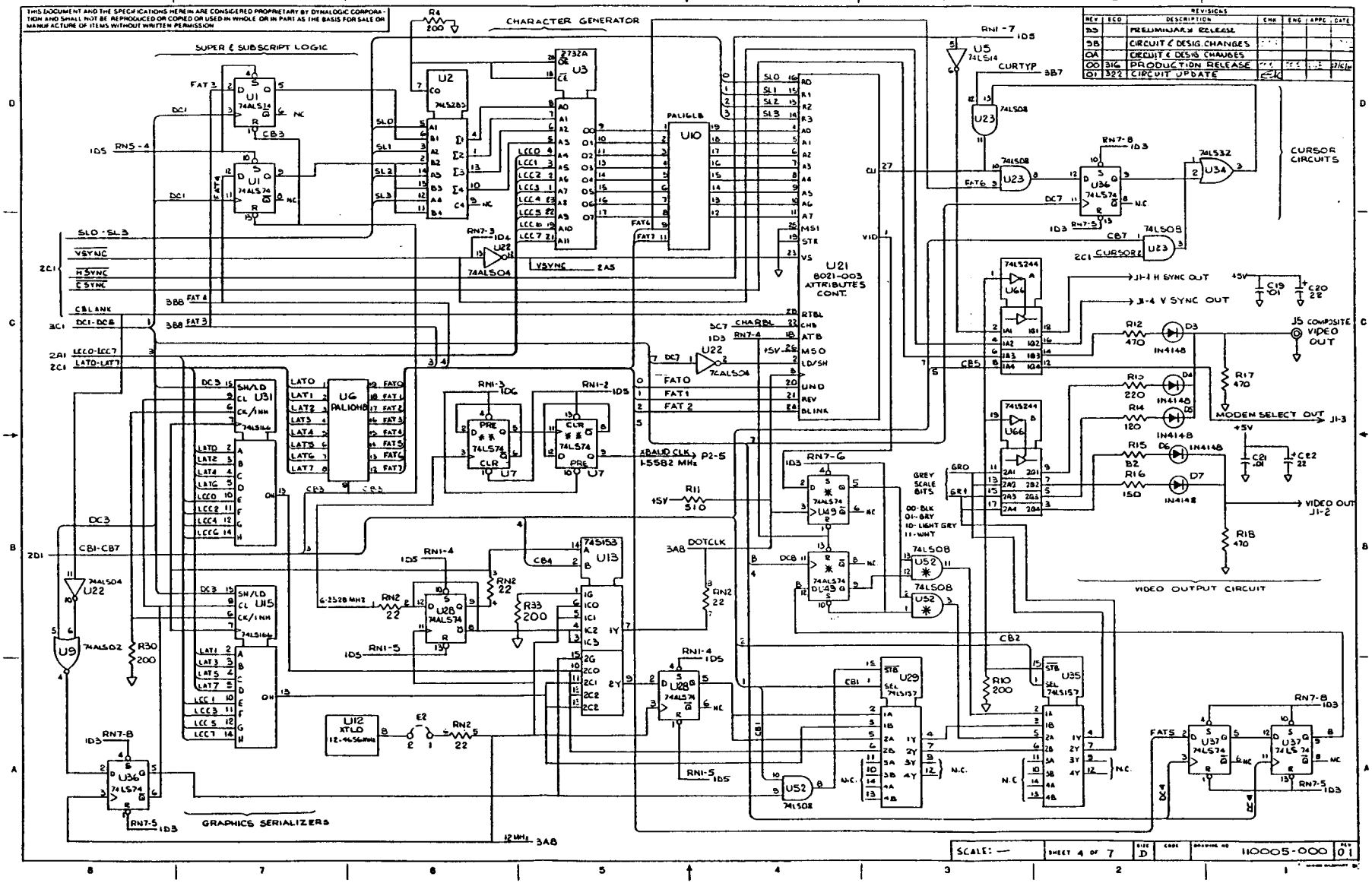
REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
88 | | PRELIMINARY RELEASE
9A | | CIRCUIT & DESIG. CHANGES
0A | | CIRCUIT & DESIG. CHANGES
00 | | PRODUCTION RELEASE
01 | 322 | CIRCUIT UPDATE
03 | 323 | IN ZONE D& SPARE U8 ADD.
CONTROL REGISTER
U75 CRT 9007 CRT CONTROLLER
SCALE: —
SHEET 2 OF 7
SIZE D
DRAWING NO 110005-000
REV C3

REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
99		PRELIMINARY RELEASE				
9B		CIRCUIT & DESIG CHANGES				
0A		CIRCUIT & DESIG CHANGES				
00		PRODUCTION RELEASE				
01	322	CIRCUIT UPDATE				
03	323	CIRCUIT UPDATE				

MEMORIES & DECODING

TIMING GENERATOR

SCALE: —	SHEET 3 OF 7	SIZE D	CODE	DRAWING NO 110005-000	REV 03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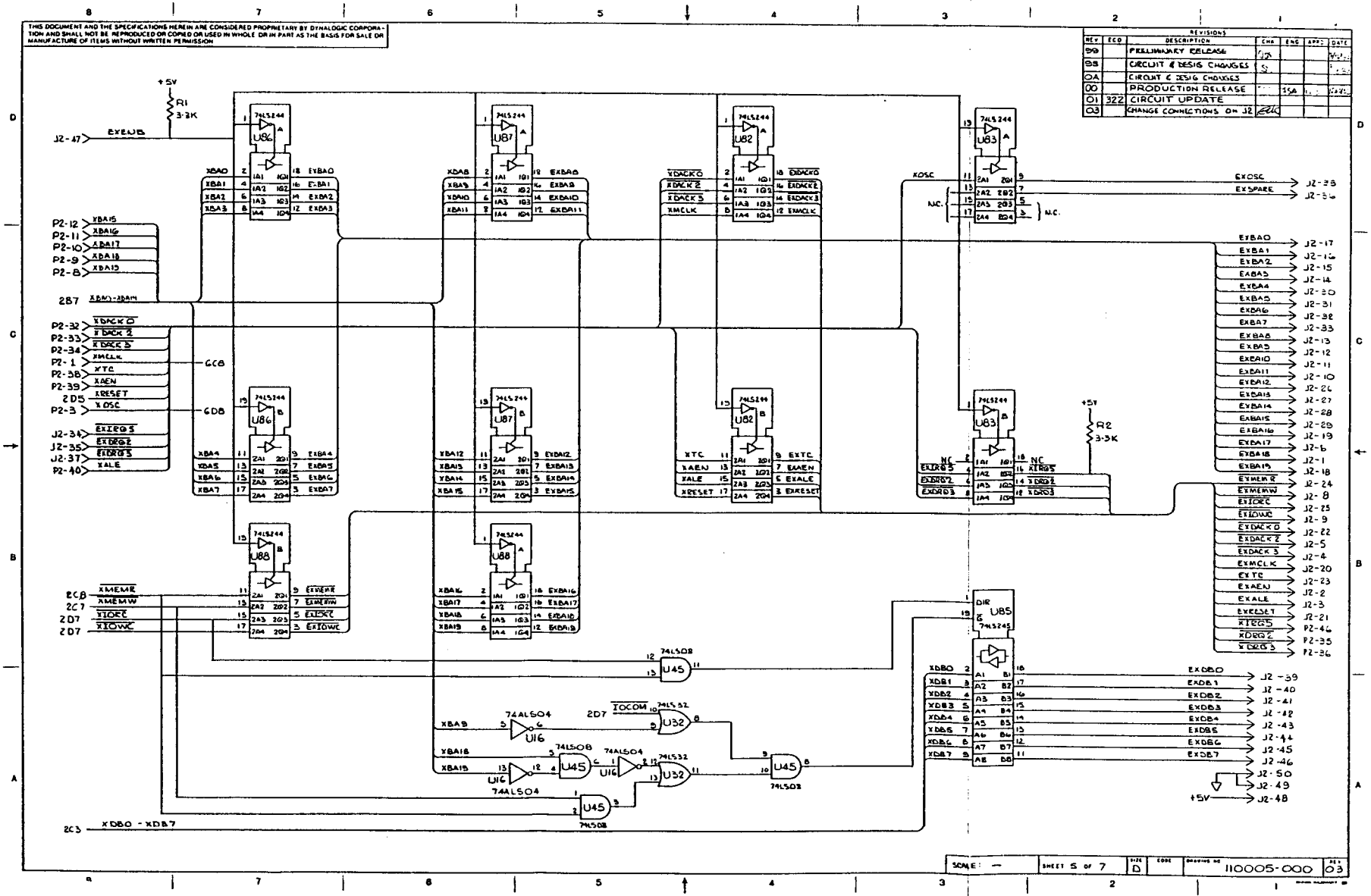
REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPR | DATE
PRELIMINARY RELEASE
CIRCUIT & DESIG. CHANGES
CIRCUIT & DESIG CHANGES
PRODUCTION RELEASE
CIRCUIT UPDATE
CHARACTER GENERATOR
SUPER & SUBSCRIPT LOGIC
GRAPHICS SERIALIZERS
CURSOR CIRCUITS
VIDEO OUTPUT CIRCUIT
U21 8021-003 ATTRIBUTES CONT.
PAL16L8
2732A
74LS283
74LS374
74LS244
74LS153
74LS157
74LS08
74LS04
74LS02
74LS32
74LS14
74LS174
74LS164
74LS166
XTLO 12.4545MHz
6.2528 MHz
12 MHz
DOTCLK
ABAUD CLK 1.5582 MHz
J1-1 H SYNC OUT
J1-4 V SYNC OUT
J5 COMPOSITE VIDEO OUT
MODEM SELECT OUT J1-3
VIDEO OUT J1-2
GREY SCALE BITS
00-BLK 01-GRY 10-LIGHT GRY 11-WHT
SCALE: —
SHEET 4 OF 7
SIZE D
DRAWING NO 10005-000
REV 01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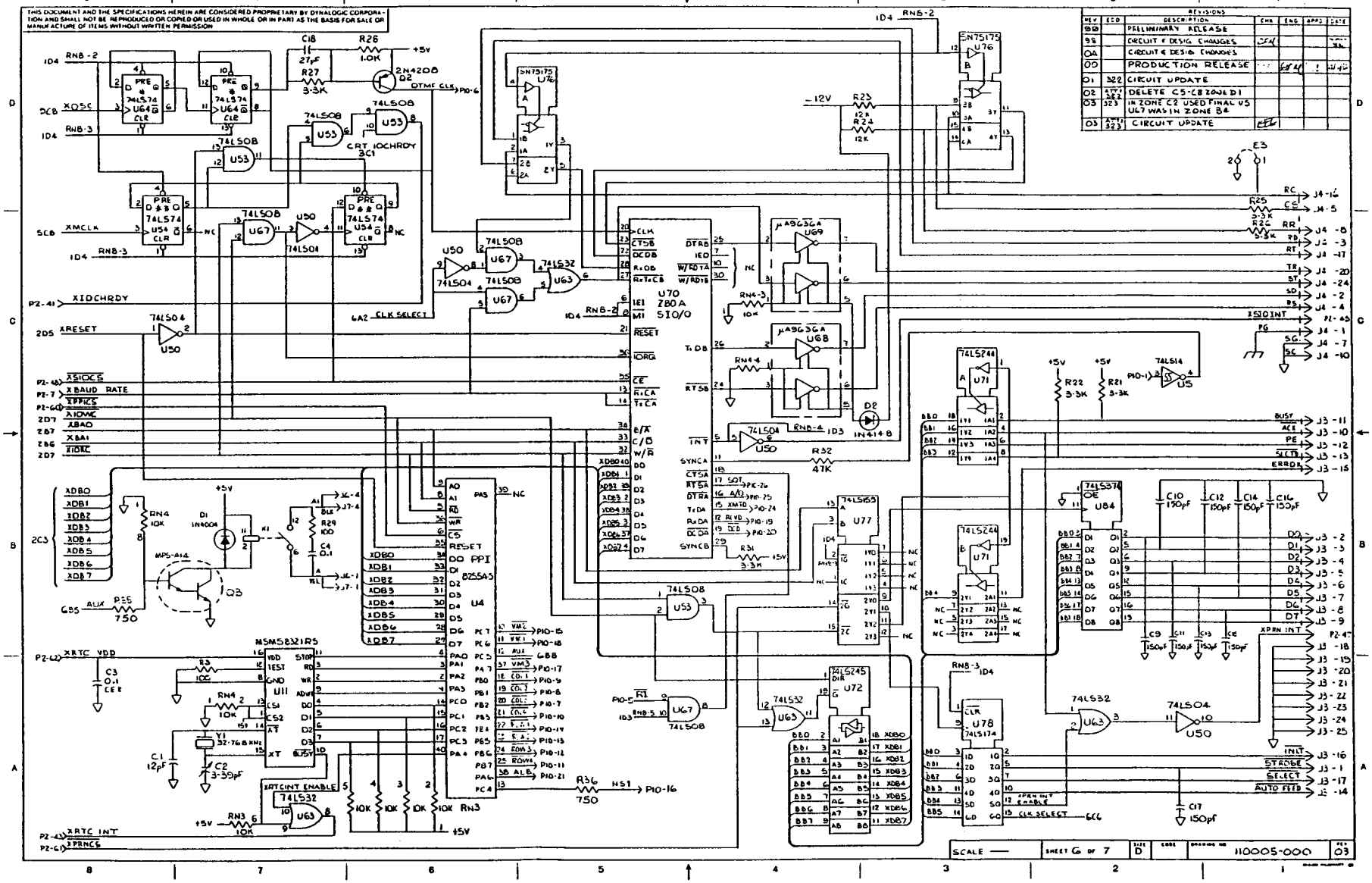
REVISIONS
REV | ECO | DESCRIPTION | CHG | ENG | APPD | DATE
99 | | PRELIMINARY RELEASE
98 | | CIRCUIT & DESIG CHANGES
0A | | CIRCUIT & DESIG CHANGES
00 | | PRODUCTION RELEASE | | 15A
01 | 322 | CIRCUIT UPDATE
03 | | CHANGE CONNECTIONS ON J2
+5V
R1
3.3K
J2-47
EXEWB
74LS244
U86
U87
U82
U83
XBA0
XBA1
XBA2
XBA3
EXBA0
EXBA1
EXBA2
EXBA3
XDA8
XBA9
XBA10
XBA11
EXBA8
EXBA9
EXBA10
EXBA11
XDACK0
XDACK2
XDACK3
XMCLK
EXDACK0
EXDACK2
EXDACK3
EXMCLK
XOSC
EXOSC
EXSPARE
N.C.
P2-12 XBA15
P2-11 XBA16
P2-10 XBA17
P2-9 XBA18
P2-8 XBA19
2B7 XBA0-XBA19
P2-32 XDACK0
P2-33 XDACK2
P2-34 XDACK3
P2-1 XMCLK
P2-38 XTC
P2-39 XAEN
2D5 XRESET
P2-3 XOSC
GC8
GD8
J2-34 EXIRQ5
J2-35 EXDRQ2
J2-37 EXDRQ3
P2-40 XALE
U86
U87
U82
U83
XBA4
XBA5
XBA6
XBA7
EXBA4
EXBA5
EXBA6
EXBA7
XBA12
XBA13
XBA14
XBA15
EXBA12
EXBA13
EXBA14
EXBA15
XTC
XAEN
XALE
XRESET
EXTC
EXAEN
EXALE
EXRESET
NC
XIRQ5
XDRQ2
XDRQ3
R2
3.3K
U88
EC8 XMEMR
2C7 XMEMW
2D7 XIORC
2D7 XIOWC
EXMEMR
EXMEMW
EXIORC
EXIOWC
XBA8
XBA9
XBA10
XBA11
EXBA8
EXBA9
EXBA10
EXBA11
74LS08
U45
74ALS04
U16
74LS32
U32
2D7 IOCOM
XBA9
XBA10
XBA11
74LS03
DIR
U85
74LS245
XDB0
XDB1
XDB2
XDB3
XDB4
XDB5
XDB6
XDB7
EXDB0
EXDB1
EXDB2
EXDB3
EXDB4
EXDB5
EXDB6
EXDB7
J2-39
J2-40
J2-41
J2-42
J2-43
J2-44
J2-45
J2-46
J2-50
J2-49
+5V J2-48
2C3 XDB0 - XDB7
EXBA0 J2-17
EXBA1 J2-16
EXBA2 J2-15
EXBA3 J2-14
EXBA4 J2-30
EXBA5 J2-31
EXBA6 J2-32
EXBA7 J2-33
EXBA8 J2-13
EXBA9 J2-12
EXBA10 J2-11
EXBA11 J2-10
EXBA12 J2-26
EXBA13 J2-27
EXBA14 J2-28
EXBA15 J2-29
EXBA16 J2-19
EXBA17 J2-6
EXBA18 J2-1
EXBA19 J2-18
EXMEMR J2-24
EXMEMW J2-8
EXIORC J2-25
EXIOWC J2-9
EXDACK0 J2-22
EXDACK2 J2-5
EXDACK3 J2-4
EXMCLK J2-20
EXTC J2-23
EXAEN J2-2
EXALE J2-3
EXRESET J2-21
XIRQ5 P2-46
XDRQ2 P2-35
XDRQ3 P2-36
SCALE: —
SHEET 5 OF 7
SIZE D
CODE
DRAWING NO 110005-000
REV 03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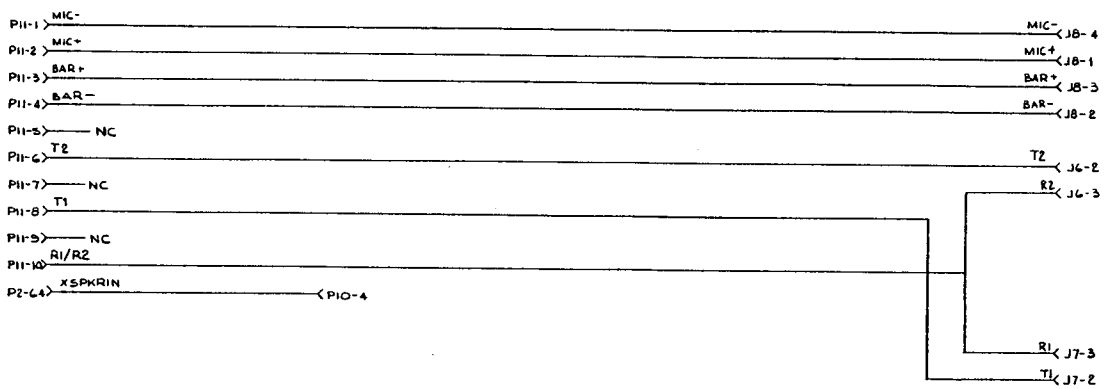
REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
00 | | PRELIMINARY RELEASE
01 | 322 | CIRCUIT UPDATE
02 | | DELETE C5-C8 ZONE D1
03 | 323 | IN ZONE C2 USED FINAL U5 U67 WAS IN ZONE B4
03 | | CIRCUIT UPDATE
U70 Z80A SIO/0
U4 8255A5
U11 MSM5832RS
U76 SN75175
U69 µA9636A
U68 µA9636A
U71 74LS244
U84 74LS374
U77 74LS165
U72 74LS245
U78 74LS174
RN3 10K
RN4 10K
RN8-2
RN8-3
RN4-3
RN4-4
RN4-A
RN8-5
RN8-A
XOSC
XMCLK
XIOCHRDY
XRESET
XSIOCS
XBAUD RATE
XPICS
XIOWC
XBAO
XBA1
XIORC
XRTC VDD
XRTC INT
XPRNCS
XSIOINT
XPRN INT
CLK SELECT
E3
R25 3.3K
R26 3.3K
R22 3.3K
R21 3.3K
R23 12K
R24 12K
R32 47K
R31 3.3K
R36 750
R35 750
R29 100
C18 27pF
R27 3.3K
R28 1.0K
2N4208 Q2
IN4148 D2
IN4004 D1
MPS-A14 Q3
Y1 32.768 KHz
C1 12pF
C2 3-39pF
C3 0.1
C4 0.1
C9 150pF
C10 150pF
C11 150pF
C12 150pF
C13 150pF
C14 150pF
C15 150pF
C16 150pF
C17 150pF
74LS08 U53
74LS08 U67
74LS04 U50
74LS32 U63
74LS74 U54
74LS14 U5
CRT IOCHRDY 3C1
XRTCINT ENABLE
PRE-26
PRE-25
PRE-24
PRE-19
PRE-20
BUSY
ACK
PE
SLCT
ERROR
INIT
STROBE
SELECT
AUTO FEED
SCALE —
SHEET 6 OF 7
SIZE D
DRAWING NO 110005-000
REV 03

REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
00		PRODUCTION RELEASE	---	[illegible]		1 JAN
01	322	CIRCUIT UPDATED	KBH			

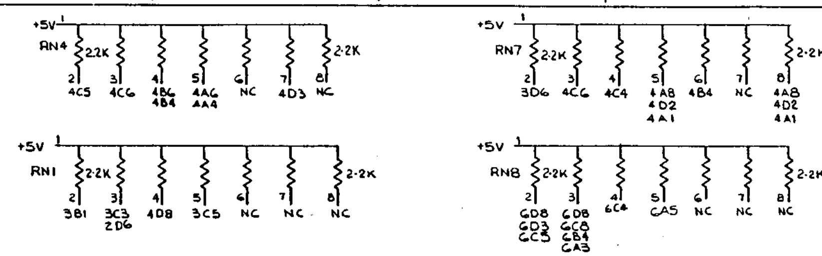


SCALE: ---	SHEET 7 OF 7	SIZE D	CODE	DRAWING NO 110005-000	REV 01

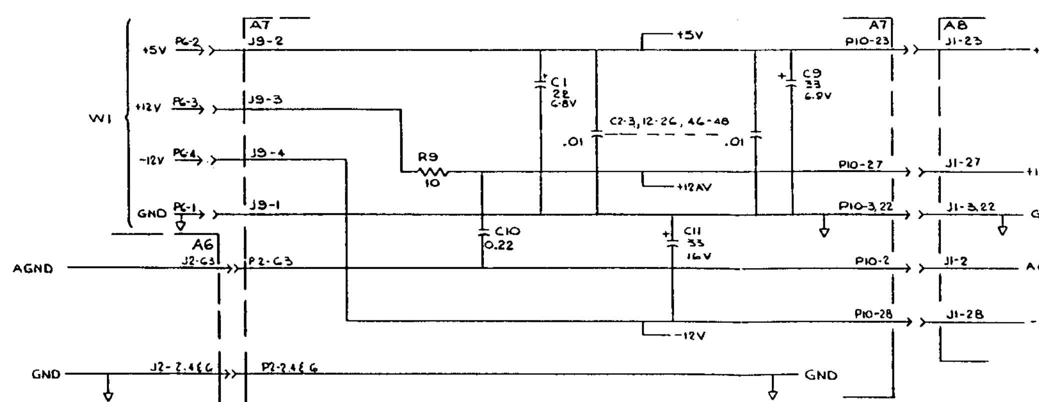
7.5 Display and I/O Board Rev 04

DIGITAL POWER AND GROUND TABLE

IC No	TYPE	POWER +5	POWER 12AV	POWER -12	GND	QTY
U9	74ALS02	14			7	1
U16, U22	74ALS04	14			7	2
U50	74LS04	14			7	1
U23, U45, U48, U51-U55, U67	74LS08	14			7	7
U5	74LS14	14			7	1
U65	74LS30	14			7	1
U24, U33	74ALS32	14			7	2
U32, U34, U61, U63	74LS32	14			7	4
U1, U8, U18, U19-U20, U28, U39	74ALS74	14			7	7
U7, U17, U36, U37, U56, U64	74LS74	14			7	6
U38	74LS139	16			8	1
U13	74LS153	16			8	1
U77	74LS155	14			7	1
U29, U35	74LS157	16			8	2
U15, U31	74LS166	16			8	2
U78	74LS174	16			8	1
U46, U47, U66, U71, U79-U83, U73, U86-U88, U74	74LS244	20			10	14
U30, U59, U72, U85	74LS245	20			10	4
U60	74LS273	20			10	1
U2	74LS283	16			8	1
U14, U43, U44, U84	74LS374	20			10	4
U62	74ALS574	20			10	1
U76	75175	16			8	1
U3	2732A	24			12	1
U4	8255A-5	26			7	1
U21	8021-003	12			17	1
U75	CRT 9007	21			40	1
U25	PAL12L6	20			10	1
U10	PAL16L8	20			10	1
U26, U27, U39-U42, U55-U58	HM6116-3	24			12	10
U11	MSM5832RS				8	1
U69, U68	µA9636A		8		4	2
U70	Z80A SIO/0	9			31	1
U6	PAL10H8	20			10,11	1
U12	XTLO	14			7	1



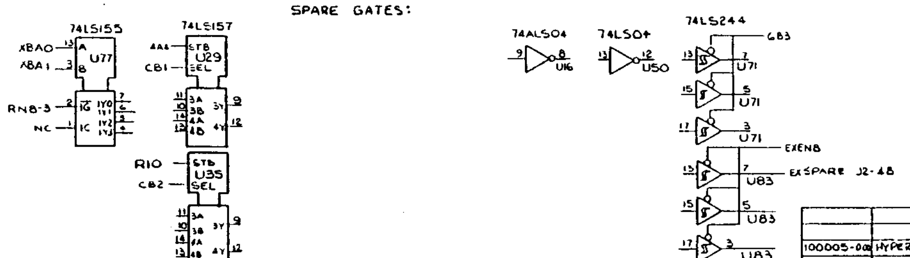
HIGHEST DESIGNATIONS USED											
C	D		E	J	K	P	Q	R	RN	U	Y
C48	D7		E3	J9	K1	P11	Q3	R36	RN8	U88	Y1
HIGHEST DESIGNATIONS NOT USED											
C34											



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, 1/4 W; CAPACITANCE VALUES ARE IN MICROFARADS (µF).
2. CIRCUIT COMPONENTS SHOWING THE SYMBOLS * OR ** ARE COMMON TO THE SAME IC PACKAGE.
3. SCHEMATIC 110005-000-04 IS TO BE USED WITH PWA 100005-000-04 AND PWB 600004-000-02 ONLY.

SPARE GATES:



REVISIONS

REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
99		PRELIMINARY RELEASE				
98		CIRCUIT & DESIG. CHANGES	[illegible]			[illegible]
0A		CIRCUIT & DESIG CHANGES				
00	316	PRODUCTION RELEASE	[illegible]	[illegible]	[illegible]	[illegible]
01	322	CIRCUIT UPDATE	[illegible]			
02	ATTI 322	ON SHT6 ZONE D2 DEL. C5-C8	[illegible]			
03	323	USED SPARE GATE U8 SHT2 ZONE DC & U5 SHT.6 ZONE C2	[illegible]		[illegible]	[illegible]
03	ATTI 323	IN ZONE A3 SHEET 6 USED SPARE U78 PIN 14 & 15	[illegible]		[illegible]	[illegible]
04	357	CONNECTIONS CHANGED/ ADDED.		[illegible]	[illegible]	[illegible]

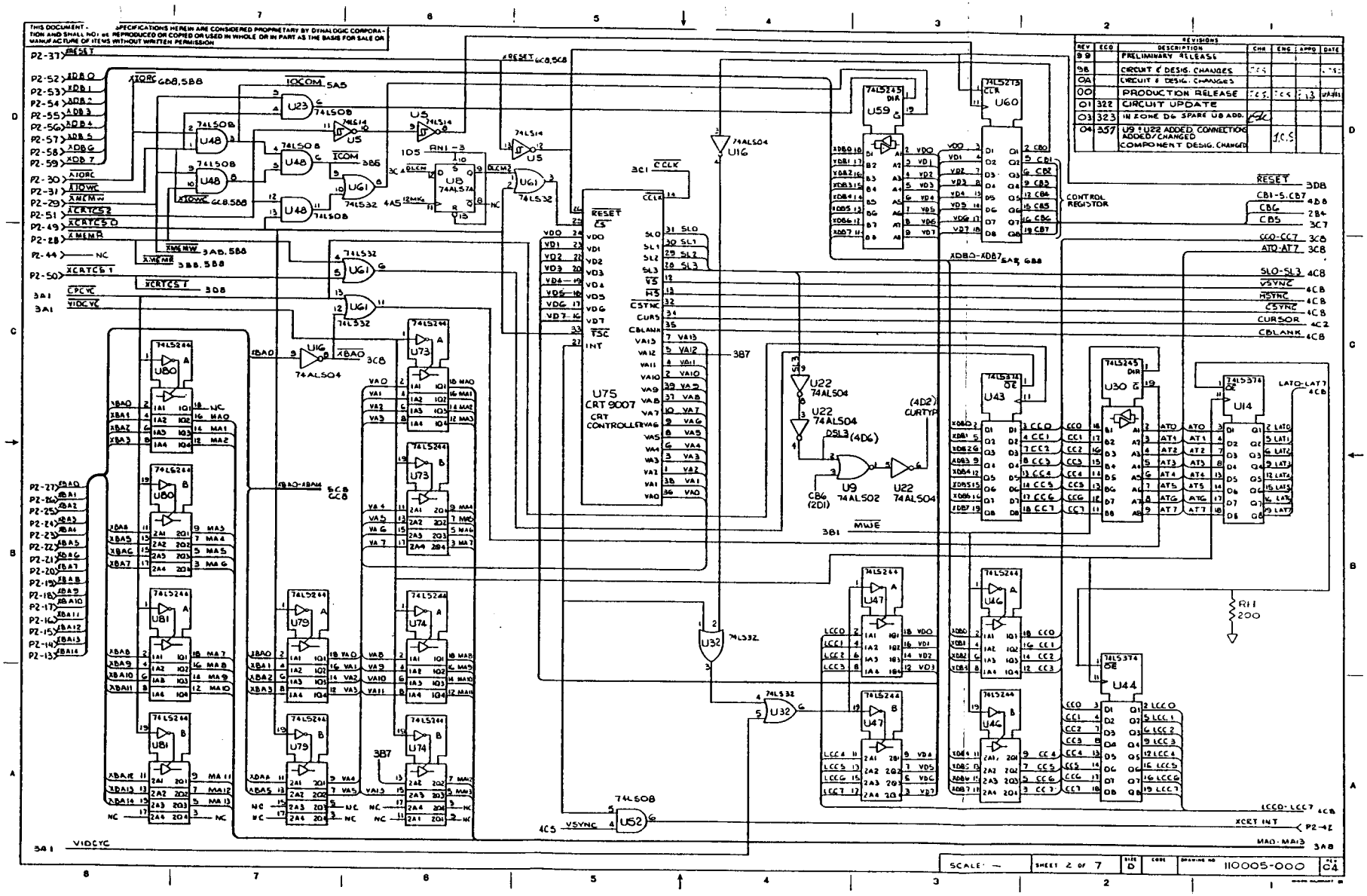
REV	04	04	04	04	04	04	04
SHEET	7	6	5	4	3	2	1

NEXT ASS'Y	100005-000
USED ON	HYPERION
DRAWN	G. LEVEILLE, 29 MAY 1981
CHECKED	J.C. SULLIVAN
ENGINEER	J.C. SULLIVAN
SCALE	—
SHEET	1 OF 7
SIZE	D

Dynalogic Corporation
Ottawa – Canada

TITLE: DISPLAY AND I/O CARD - A7

DRAWING NO 110005-000 REV 04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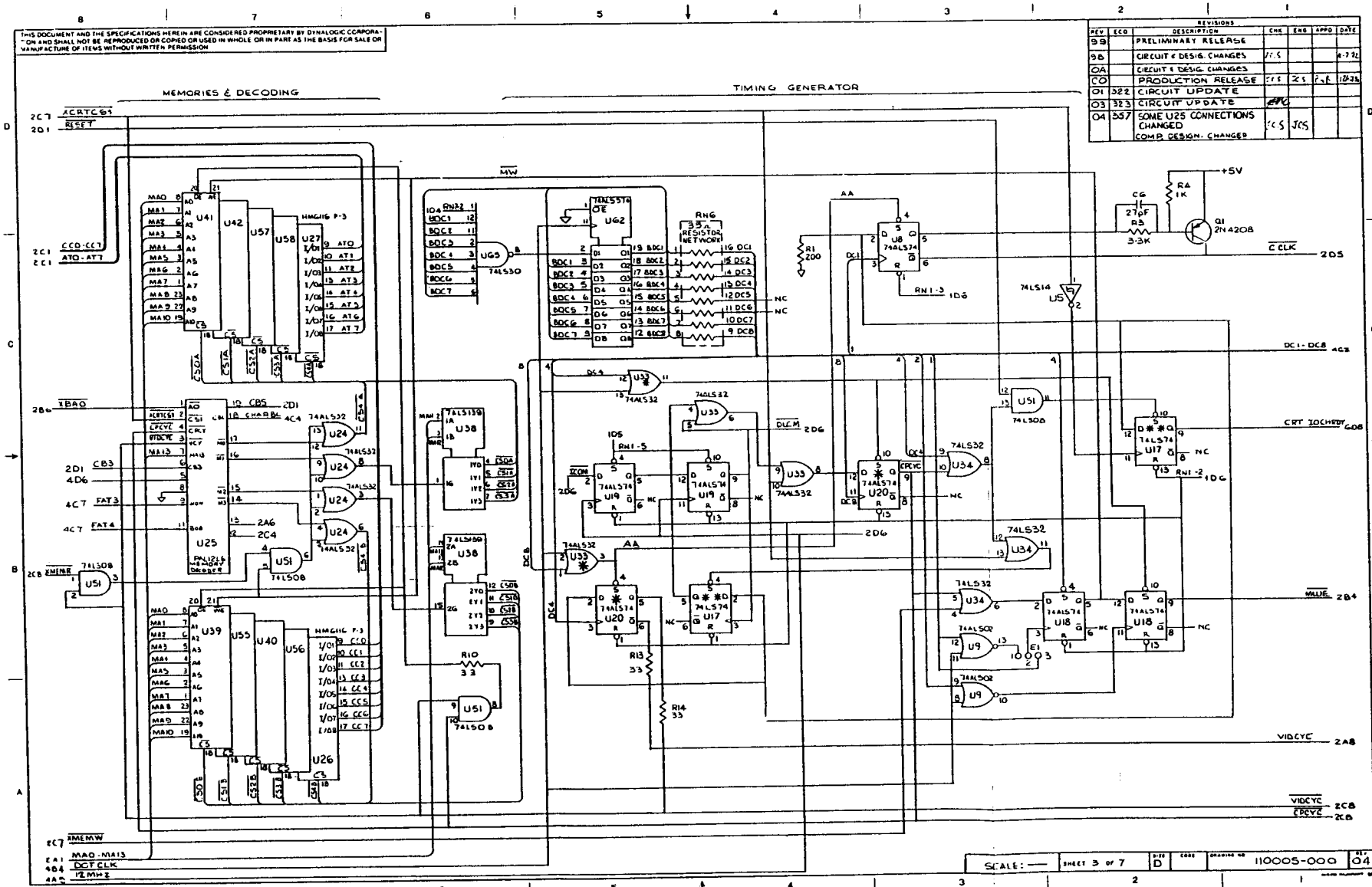
REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
89 | | PRELIMINARY RELEASE
98 | | CIRCUIT & DESIG. CHANGES
0A | | CIRCUIT & DESIG. CHANGES
00 | | PRODUCTION RELEASE
01 | 322 | CIRCUIT UPDATE
03 | 323 | IN ZONE D6 SPARE U8 ADD.
04 | 357 | U9 \ U22 ADDED, CONNECTIONS ADDED/CHANGED, COMPONENT DESIG. CHANGED
U75 CRT 9007 CRT CONTROLLER
CONTROL REGISTOR
U9 74ALS02
U22 74ALS04
U32 74LS32
U52 74LS08
U5 74LS14
U8 74ALS74A
U16 74ALS04
U23 74LS08
U48 74LS08
U61 74LS32
U59 74LS245 DIR
U60 74LS273 CLR
U43 74LS273
U30 74LS245 DIR
U14 74LS374
U44 74LS374
U80 74LS244
U60 74LS244
U81 74LS244
U73 74LS244
U79 74LS244
U74 74LS244
U47 74LS244
U46 74LS244
RESET
CCLK
VIDCYC
XCRTINT
R11 200
SCALE: —
SHEET 2 OF 7
SIZE D
DRAWING NO 110005-000
REV C4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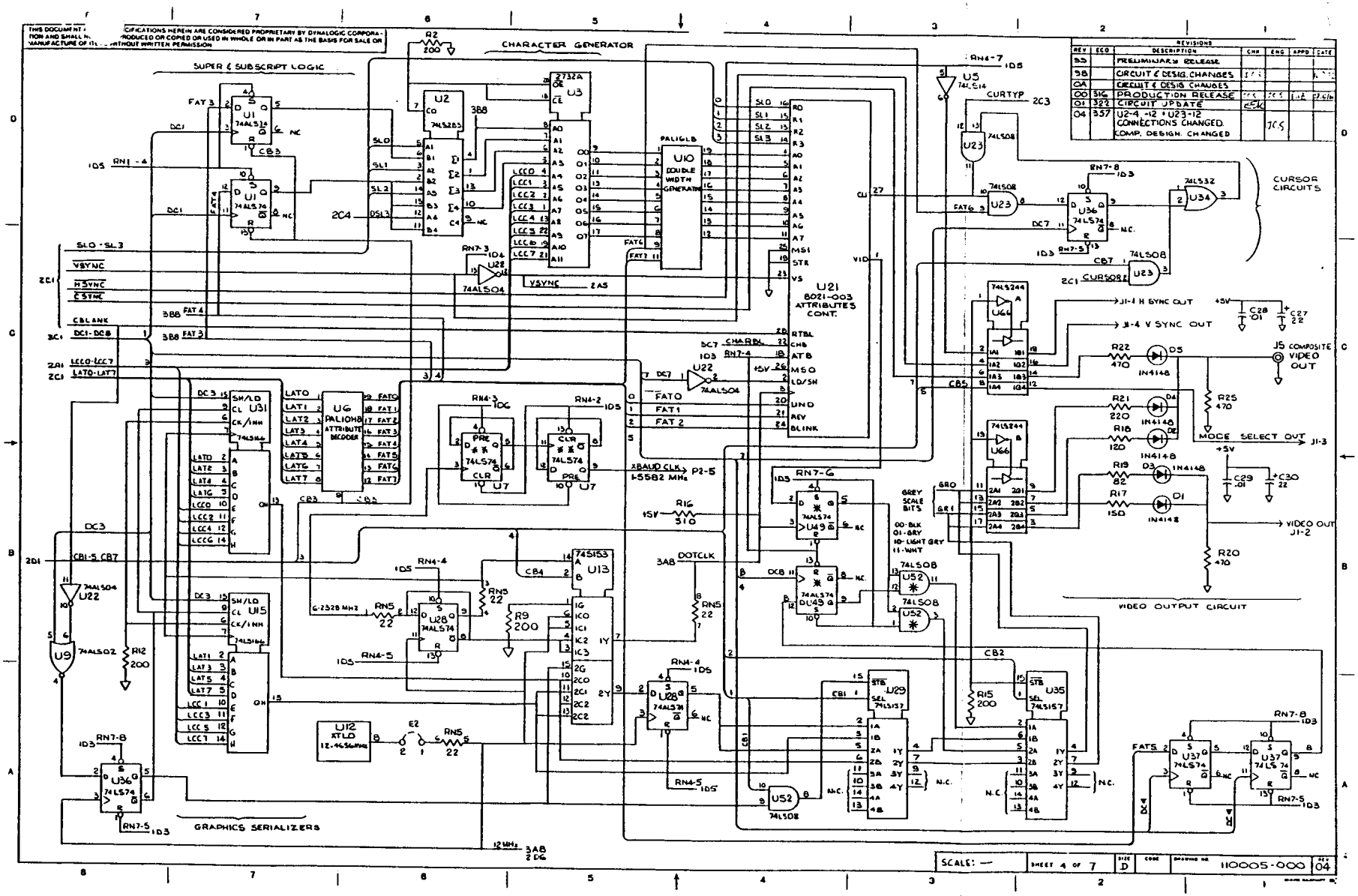
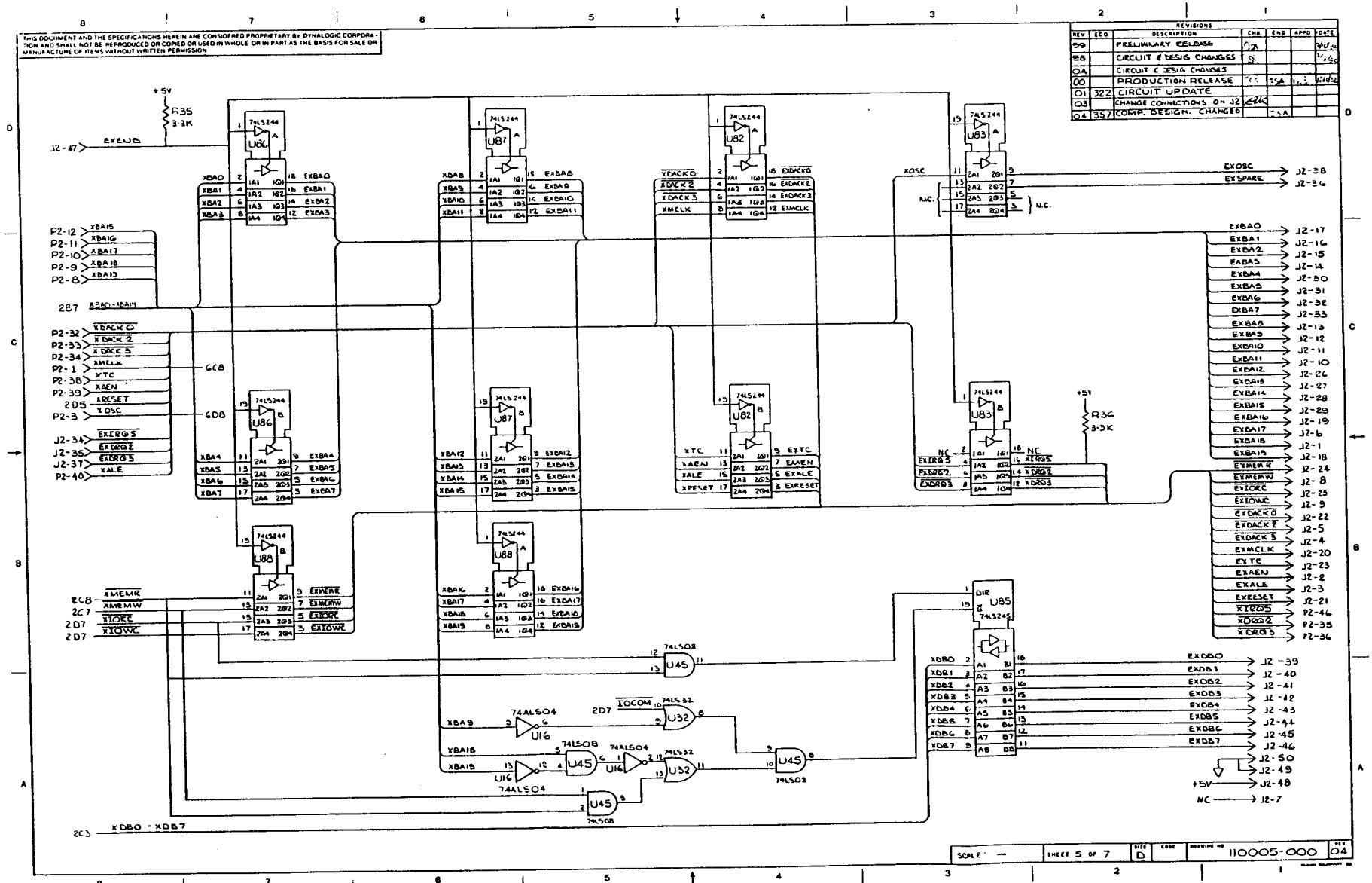
REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
99 | | PRELIMINARY RELEASE
98 | | CIRCUIT & DESIG. CHANGES
0A | | CIRCUIT & DESIG. CHANGES
CO | | PRODUCTION RELEASE
01 | 322 | CIRCUIT UPDATE
03 | 323 | CIRCUIT UPDATE
04 | 357 | SOME U25 CONNECTIONS CHANGED
COMP. DESIGN. CHANGES
MEMORIES & DECODING
TIMING GENERATOR
ACRTC6T
RESET
CCO-CC7
ATO-AT7
RMENW
MAO-MA13
DOT CLK
12 MHz
MW
RNG
RESISTOR NETWORK
+5V
C CLK
DC1-DC8
CRT IOCHRDY
MWE
VIDCYC
CPCYC
SCALE: —
SHEET 3 OF 7
SIZE D
DRAWING NO 110005-000
REV 04



REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
99		PRELIMINARY RELEASE				
98		CIRCUIT & DESIG. CHANGES				
04		CIRCUIT & DESIG CHANGES				
00	316	PRODUCTION RELEASE				
01	322	CIRCUIT UPDATE				
04	357	U2-4 -12 + U23-12 CONNECTIONS CHANGED. COMP. DESIGN. CHANGED		JCS		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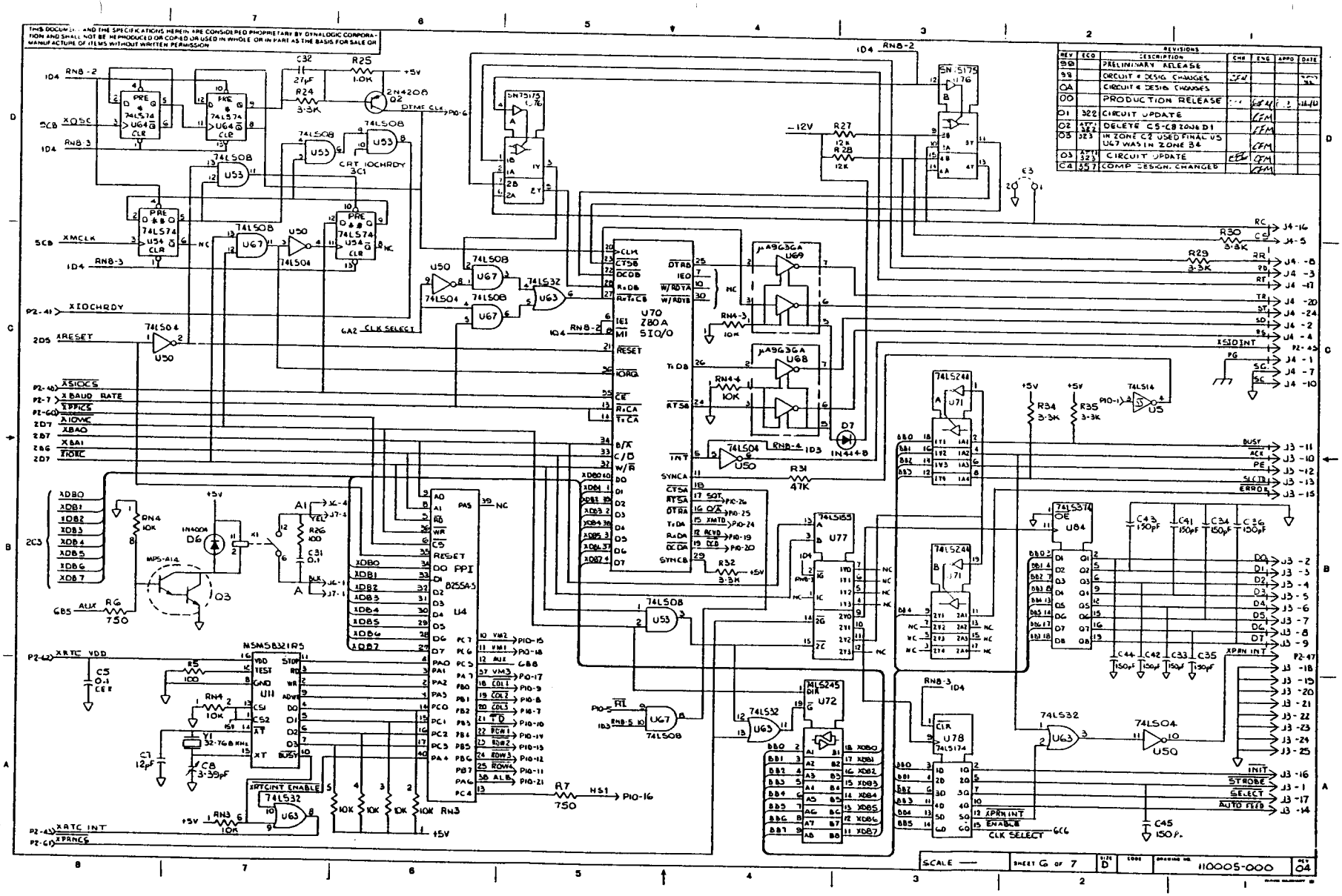
REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
99 | | PRELIMINARY RELEASE
98 | | CIRCUIT & DESIG CHANGES
0A | | CIRCUIT & DESIG CHANGES
00 | | PRODUCTION RELEASE
01 | 322 | CIRCUIT UPDATE
03 | | CHANGE CONNECTIONS ON J2
04 | 357 | COMP. DESIGN. CHANGED
+5V
R35 3.3K
J2-47 EXBUS
XBA0 - XBA19
XDB0 - XDB7
U86 U87 U82 U83 U88 U85 U45 U16 U32
74LS244 74LS245 74LS08 74ALS04 74LS32
EXOSC
EXSPARE
R36 3.3K
SCALE —
SHEET 5 OF 7
SIZE D
DRAWING NO 110005-000
REV 04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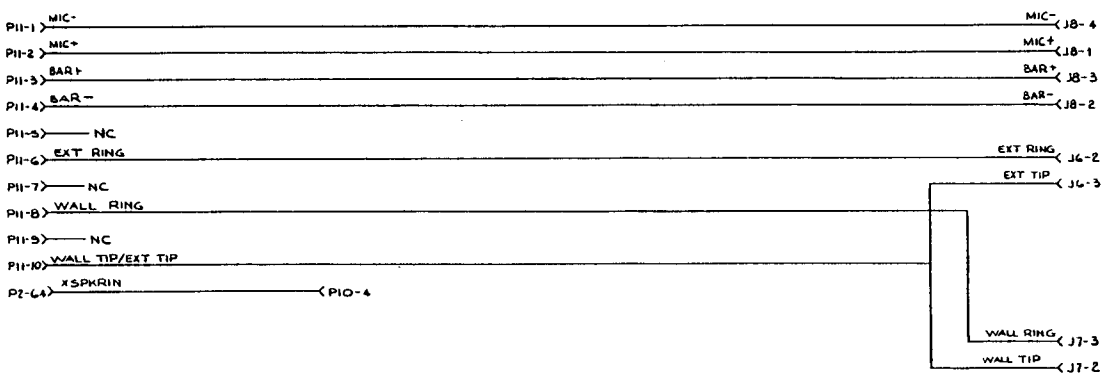
REVISIONS
REV ECO DESCRIPTION CHK ENG APPD DATE
99 PRELIMINARY RELEASE
99 CIRCUIT & DESIG CHANGES
0A CIRCUIT & DESIG CHANGES
00 PRODUCTION RELEASE
01 322 CIRCUIT UPDATE
02 DELETE C5-C8 ZONE D1
03 323 IN ZONE C2 USED FINAL U5 U67 WAS IN ZONE B4
03 323 CIRCUIT UPDATE
04 357 COMP DESIGN. CHANGES
U70 Z80A SIO/O
PPI 8255A5
MSM5832RS
SCALE
SHEET 6 OF 7
SIZE B
110005-000
REV 04

REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
00		PRODUCTION RELEASE	JCC	CFM	PAE	7/7/81
01	322	CIRCUIT UPDATED	KBM	CFM		
04	357	COMP. DESIGN. CHANGED		CFM		



SCALE: —	SHEET 7 OF 7	SIZE D	CODE	DRAWING NO 110005-000	REV 04

7.6 Display and I/O Board Rev 08

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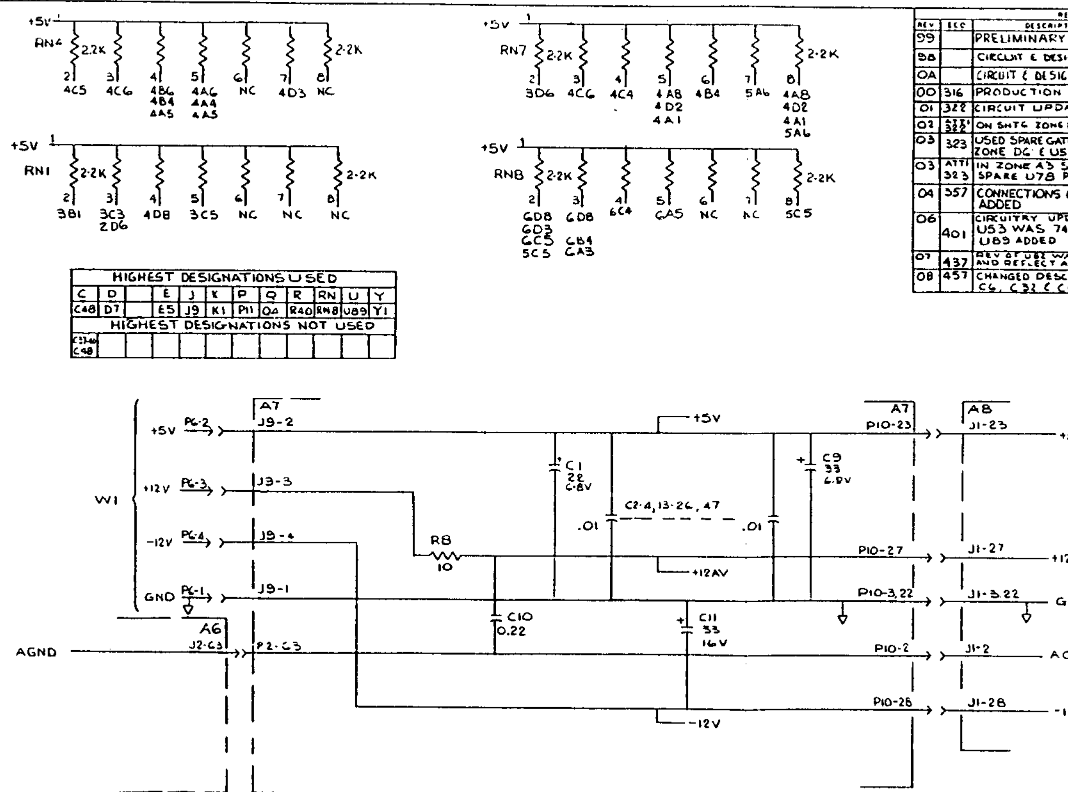
DIGITAL POWER AND GROUND TABLE

IC No	TYPE	POWER +5	POWER +12AV	POWER -12	GND	QTY
U7, U17, U36, U37, U53, U54, U64	74LS74	14			7	7
U9	74ALS02	14			7	1
U16, U22	74ALS04	14			7	2
U50	74LS04	14			7	1
U23, U45, U48, U51, U52, U67	74LS08	14			7	6
U5	74LS14	14			7	1
U65	74LS30	14			7	1
U24, U33	74ALS32	14			7	2
U32, U34, U61, U63	74LS32	14			7	4
U1, U8, U18, U20, U21, U49	74ALS74	14			7	7
U38	74LS139	16			8	1
U13	74LS153	16			8	1
U77	74LS155	14			7	1
U29, U35	74LS157	16			8	2
U15, U31	74LS166	16			8	2
U78	74LS174	16			8	1
U46, U47, U66, U71, U79-U81, U73, U83, U86-U88, U74	74LS244	20			10	14
U30, U59, U72, U85	74LS245	20			10	4
U60	74LS273	20			10	1
U2	74LS283	16			8	1
U14, U43, U44, U84	74LS374	20			10	4
U62	74ALS574	20			10	1
U76	75175	16			8	1
U3	2732A	24			12	1
U4	8255A-5	26			7	1
U21	8021-003	12			17	1
U75	CRT 9007	21			40	1
U25	PAL12L6	20			10	1
U10	PAL16L8	20			10	1
U26, U27, U39-U42, U55-U58	HM6116-3	24			12	10
U11	MSM5832RS				8	1
U69, U68	μA9636A		8		4	2
U70	Z80A SIO/O	9			31	1
U82	PAL14L4	20			10	1
U6	PAL10H8	20			10	1
U12	XTLO	14			7	1
U89	74S86	14			7	1



HIGHEST DESIGNATIONS USED

C	D		E	J	K	P	Q	R	RN	U	Y
C48	D7		E5	J9	K1	P11	Q4	R40	RN8	U89	Y1

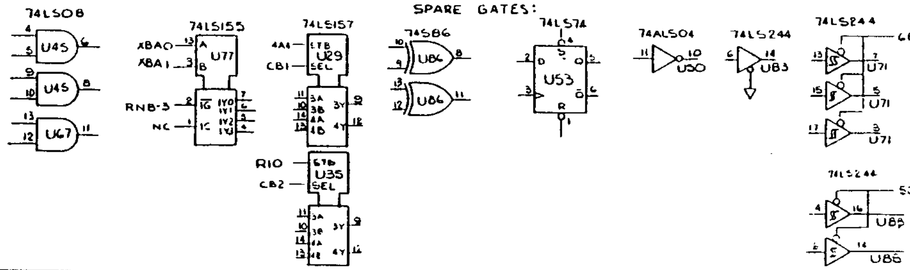
HIGHEST DESIGNATIONS NOT USED

C13-46 C48											

REVISIONS

REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
99		PRELIMINARY RELEASE				
98		CIRCUIT & DESIG. CHANGES				
0A		CIRCUIT & DESIG CHANGES				
00	316	PRODUCTION RELEASE				
01	322	CIRCUIT UPDATE				
02	322	ON SHT 6 ZONE D2 DEL. C5-C8				
03	323	USED SPARE GATE U8 SHT 2 ZONE D6 & U5 SHT. 6 ZONE C2				
03	ATTI 323	IN ZONE A3 SHEET 6 USED SPARE U78 PIN 14 & 15				
04	357	CONNECTIONS CHANGED/ ADDED				
06	401	CIRCUITRY UPDATED U53 WAS 74LS08 U89 ADDED				
07	437	REV OF U82 WAS 06, AND REFLECT ASSY DWG REV				
08	457	CHANGED DESCRIPTION OF C6, C32 & C46				

SPARE GATES:



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, 1/4 W; CAPACITANCE VALUES ARE IN MICROFARADS (μF).
2. CIRCUIT COMPONENTS SHOWING THE SYMBOLS * OR ** ARE COMMON TO THE SAME IC PACKAGE.
3. SCHEMATIC 110005-000-08 IS TO BE USED WITH PWA 100005-000-08 AND PWB DRAWING 200004-000-04. (BOARD REV IS STILL AT 03).

06	06	06	C6	06	06	08	REV
7	6	5	4	3	2	1	SHEET

Dynalogic Corporation
Ottawa – Canada

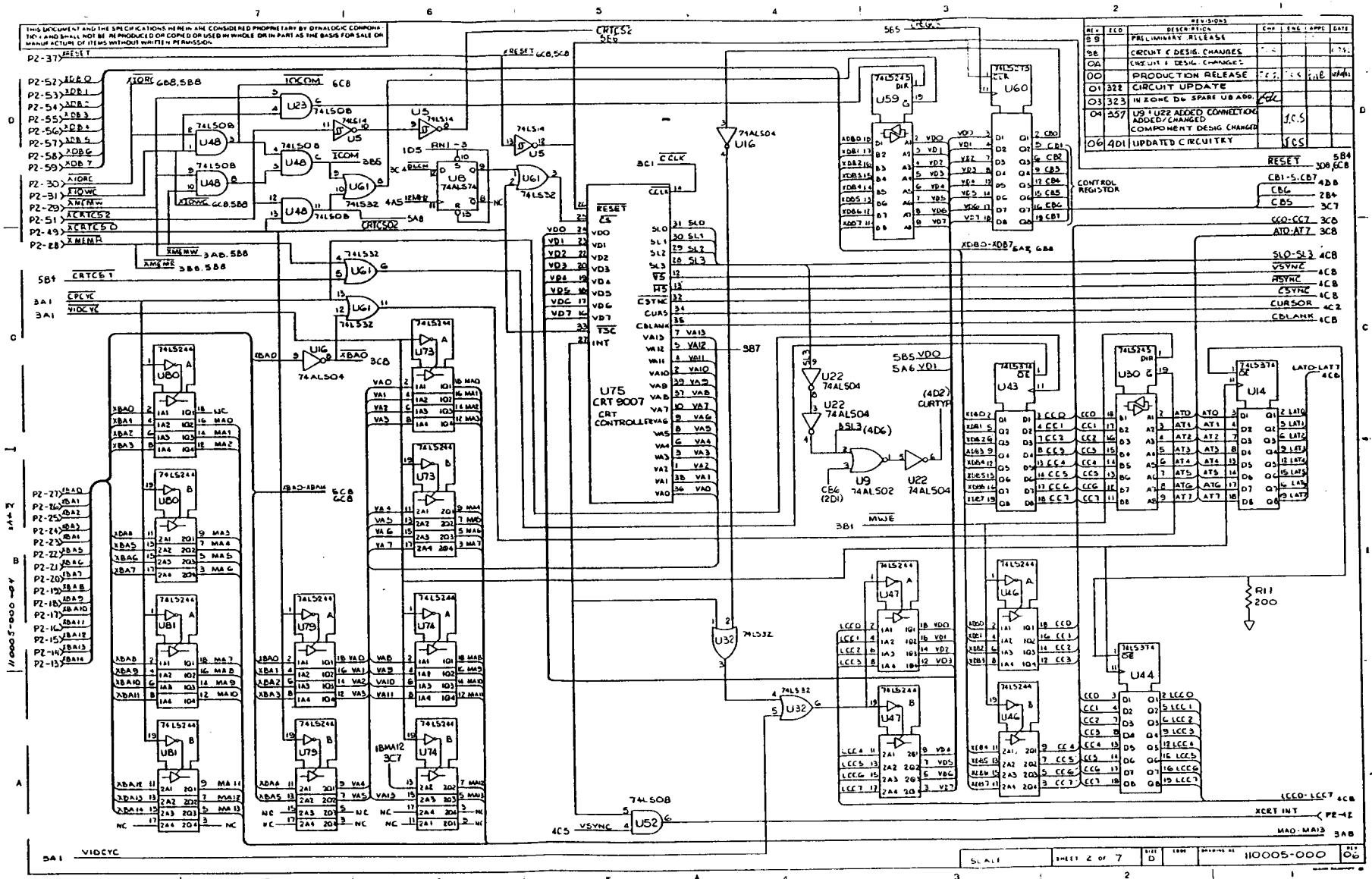
TITLE: DISPLAY AND I/O CARD - A7

DRAWN: G. LEVEILLE 29 MAY 1981
CHECKED: J. C. SULLIVAN
ENGINEER: J. C. SULLIVAN
APPROVED

NEXT ASSY: 100005-000
USED ON: HYPERION

SCALE: —
SHEET 1 OF 7
SIZE: D
DRAWING No: 110005-000
REV: 08

110005-000-08
EA41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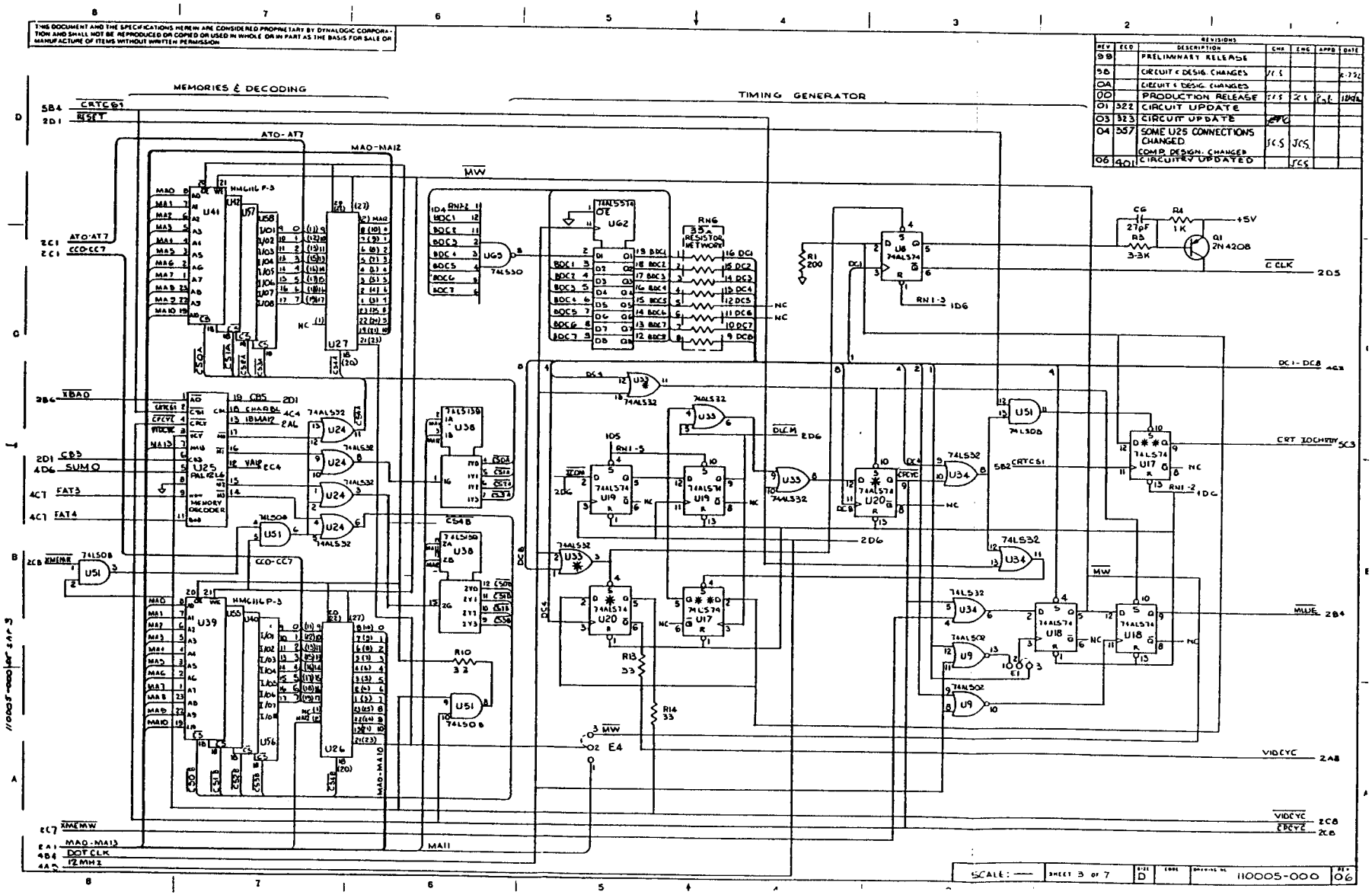
REVISIONS
REV ECO DESCRIPTION
PRELIMINARY RELEASE
CIRCUIT & DESIG. CHANGES
CIRCUIT & DESIG. CHANGES
PRODUCTION RELEASE
CIRCUIT UPDATE
IN ZONE D6 SPARE U8 ADD.
U59 & U22 ADDED CONNECTIONS ADDED/CHANGED COMPONENT DESIG CHANGED
UPDATED CIRCUITRY
U75 CRT 9007 CRT CONTROLLER
74LS244
74LS245
74LS374
74ALS504
74LS32
74ALS08
74LS14
74ALS74
74LS08
74ALS02
CONTROL REGISTOR
SCALE
SHEET 2 OF 7
SIZE D
DRAWING NO 110005-000
REV 06



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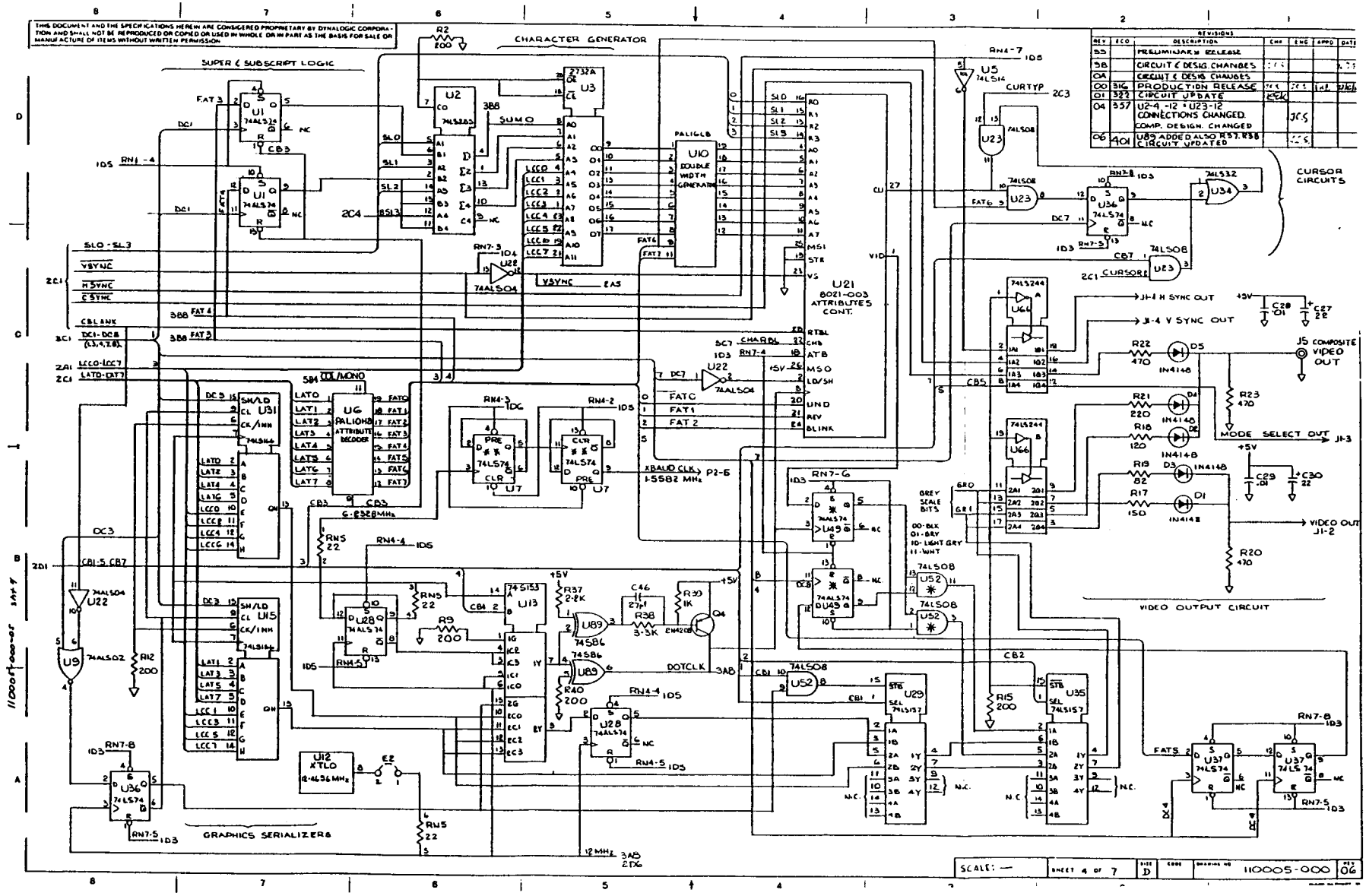
REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
98		PRELIMINARY RELEASE				
98		CIRCUIT & DESIG. CHANGES	JCS			6-7-84
0A		CIRCUIT & DESIG. CHANGES				
00		PRODUCTION RELEASE	JCS	JCS	PAT	10/4/84
01	322	CIRCUIT UPDATE				
03	323	CIRCUIT UPDATE				
04	357	SOME U25 CONNECTIONS CHANGED COMP. DESIGN. CHANGED	JCS	JCS		
06	401	CIRCUITRY UPDATED		JCS		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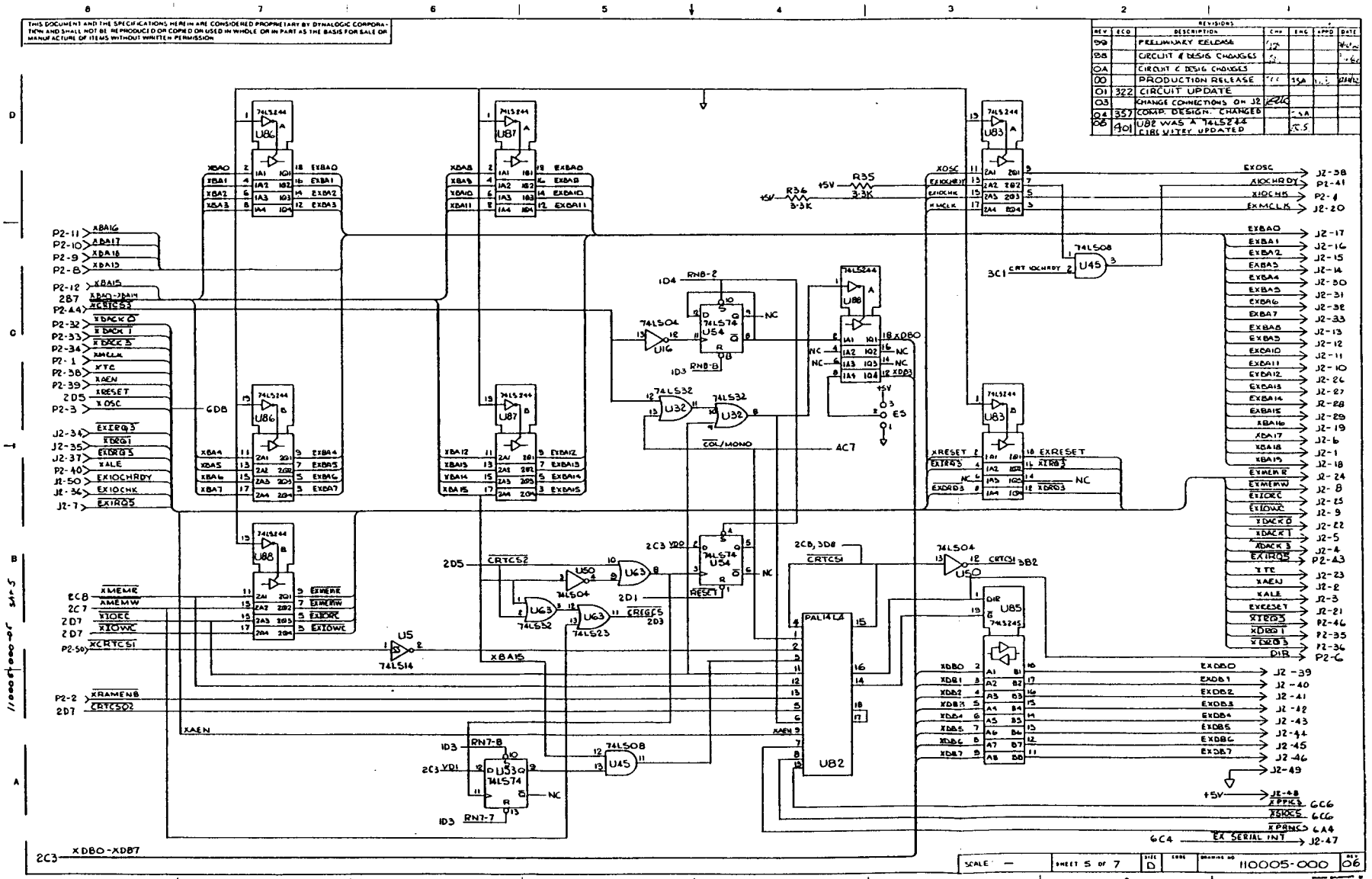
REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
55 | | PRELIMINARY RELEASE
5B | | CIRCUIT & DESIG. CHANGES
0A | | CIRCUIT & DESIG CHANGES
00 | 316 | PRODUCTION RELEASE
01 | 323 | CIRCUIT UPDATE
04 | 357 | U2-4 -12 & U23-12 CONNECTIONS CHANGED. COMP. DESIGN. CHANGED
06 | 401 | U89 ADDED ALSO R57, R58 CIRCUIT UPDATED
CHARACTER GENERATOR
SUPER & SUBSCRIPT LOGIC
GRAPHICS SERIALIZERS
CURSOR CIRCUITS
VIDEO OUTPUT CIRCUIT
U1 74ALS74
U2 74S283
U3 2732A OR
U5 74LS14
U7 74LS74
U8 PAL16H8 ATTRIBUTE DECODER
U9 74ALS02
U10 PAL16L8 DOUBLE WIDTH GENERATOR
U12 X'TLO 12.4636 MHz
U13 74S153
U21 8021-003 ATTRIBUTES CONT.
U22 74ALS04
U23 74LS08
U28 74ALS74
U29 74LS157
U31 SH/LD CK/INH 74LS166
U34 74LS32
U35 74LS157
U36 74LS74
U37 74LS74
U45 74ALS74
U49 74ALS74
U52 74LS08
U66 74LS244
U89 74S86
XBAUD CLK 1.5582 MHz P2-6
12 MHz 3AB 2D6
J1-4 H SYNC OUT
J1-4 V SYNC OUT
J5 COMPOSITE VIDEO OUT
MODE SELECT OUT J1-3
VIDEO OUT J1-2
GREY SCALE BITS
00-BLK 01-GRY 10-LIGHT GRY 11-WHT
SCALE: —
SHEET 4 OF 7
SIZE D
DRAWING NO 110005-000
REV 06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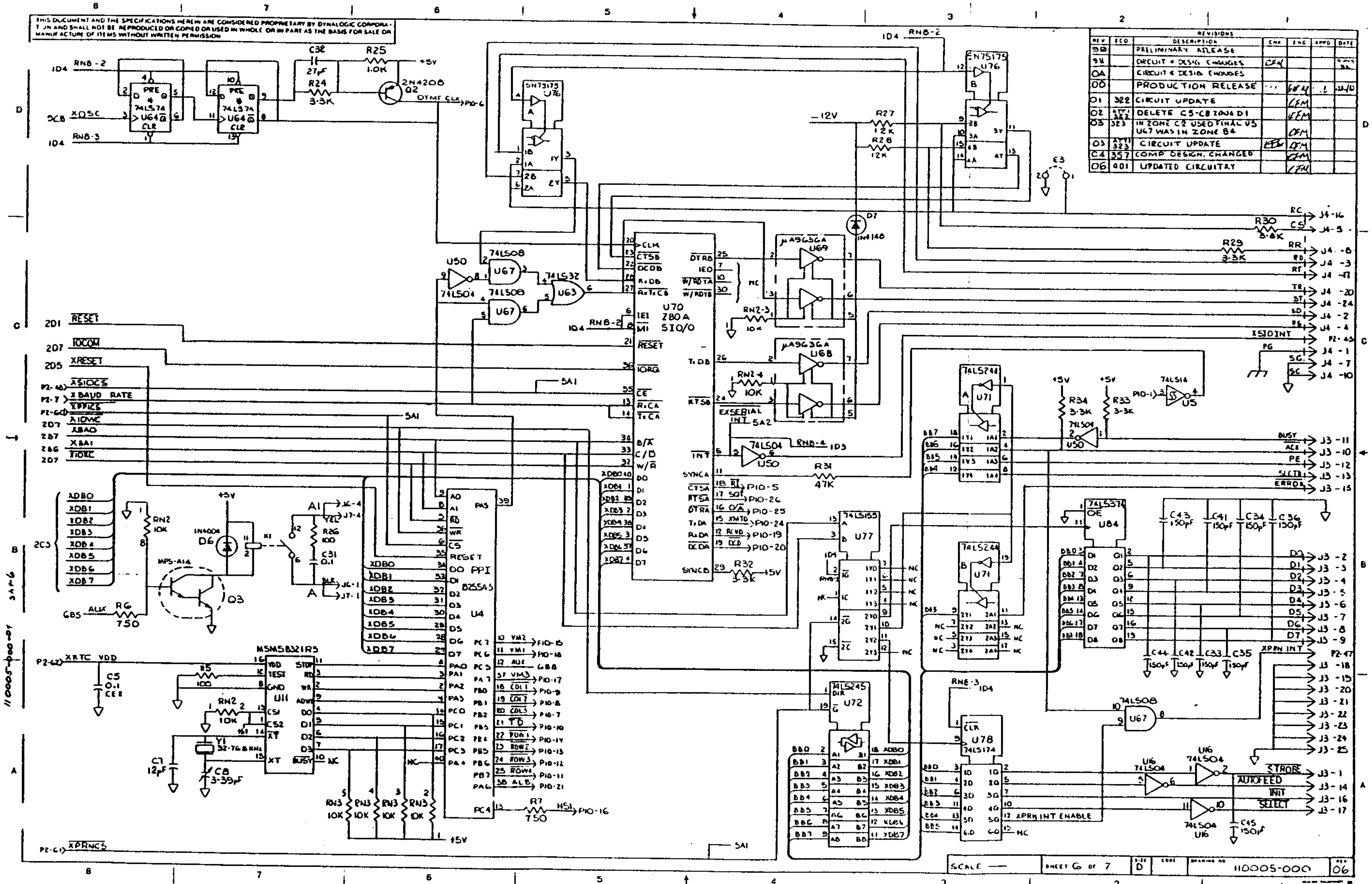
REVISIONS
REV ECO DESCRIPTION CHK ENG APPD DATE
00 PRELIMINARY RELEASE
05 CIRCUIT & DESIG CHANGES
0A CIRCUIT & DESIG CHANGES
00 PRODUCTION RELEASE
01 322 CIRCUIT UPDATE
03 CHANGE CONNECTIONS ON J2
04 357 COMP. DESIGN. CHANGES
06 401 U82 WAS A 74LS244 CIRCUITRY UPDATED
74LS244
74LS245
74LS74
74LS04
74LS08
74LS32
74LS52
74LS123
74LS14
PAL14L4
U82
U83
U85
U86
U87
U88
U45
U50
U54
U63
U16
U32
U33
U5
RN7-8
RN7-7
RN8-8
RN8-7
R35 3.3K
R36 8.3K
+5V
XDSC
XIOCHRDY
XIOCHK
XMCLK
XBA0
XBA1
XBA2
XBA3
XBA4
XBA5
XBA6
XBA7
XBA8
XBA9
XBA10
XBA11
XBA12
XBA13
XBA14
XBA15
XBA16
XBA17
XBA18
XBA19
XDB0
XDB1
XDB2
XDB3
XDB4
XDB5
XDB6
XDB7
XRESET
XDACK0
XDACK1
XDACK3
XDRQ1
XDRQ3
XIORC
XIOWC
XMEMR
XMEMW
XREFRQ
XTC
XALE
XAEN
XCRTCS1
XCRTCS2
XRAMCS3
XRAMEN
XRAMCS2
XRAMCS1
XRAMCS0
XPPICS
XSIOCS
XPANCS
EX SERIAL INT
RESET
COL/MONO
ES
NC
SCALE —
SHEET 5 OF 7
SIZE D
DRAWING NO 110005-000
REV 06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REVISIONS
REV | ECO | DESCRIPTION
98 | | PRELIMINARY RELEASE
9A | | CIRCUIT & DESIG. CHANGES
OA | | CIRCUIT & DESIG. CHANGES
00 | | PRODUCTION RELEASE
01 | 322 | CIRCUIT UPDATE
02 | | DELETE C5-C8 ZONE D1
03 | 323 | IN ZONE C2 USED FINAL U5 U67 WAS IN ZONE B4
03 | | CIRCUIT UPDATE
C4 | 357 | COMP. DESIGN. CHANGED
06 | 401 | UPDATED CIRCUITRY
U70 Z80A SIO/O
U4 8255A5 PPI
U11 MSM5832IRS
U64 74LS74
U76 SN75175
U69 µA9636A
U68 µA9636A
U67 74LS08
U63 74LS32
U50 74LS04
U71 74LS244
U77 74LS155
U84 74LS374
U72 74LS245
U78 74LS174
U16 74LS04
U5 74LS14
Q2 2N4208
Q3 MPS-A14
D6 1N4004
D7 1N4148
Y1 32.768 KHz
RESET
IOCOM
XRESET
XSIOCS
XBAUD RATE
XPPICS
XIOWC
XBA0
XBA1
IORC
XRTC VDD
XPRNCS
XPRN INT
APRN INT ENABLE
STROBE
AUTOFEED
INIT
SELECT
BUSY
ACK
PE
SLCT
ERROR
XSIOINT
SCALE —
SHEET 6 OF 7
SIZE D
110005-000
REV 06

REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
00		PRODUCTION RELEASE	[illegible]	[illegible]	[illegible]	[illegible]
01	322	CIRCUIT UPDATED	[illegible]	[illegible]		
04	357	COMP. DESIGN CHANGED		[illegible]		
06	401	UPDATED CIRCUITRY				

P11-1 MIC- → MIC- J8-4
P11-2 MIC+ → MIC+ J8-1
P11-3 BAR+ → BAR+ J8-3
P11-4 BAR- → BAR- J8-2
P11-5 — NC
P11-6 EXT RING → EXT RING J6-2
P11-7 — NC
P11-8 WALL RING → WALL RING J7-3
P11-9 — NC
P11-10 WALL TIP/EXT TIP → WALL TIP J7-2
EXT TIP J6-3
P2-C4 XSPKRIN → P10-4

110005-000 SHT 7

SCALE	SHEET	SIZE	CODE	DRAWING NO	REV
—	7 OF 7	D		110005-000	06

7.7 Modem Board Rev 03

REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
0A		PRELIMINARY RELEASE				
0B		J1 WAS P10; J2 WAS P9				
0C		MPS-A14 WAS MPS-AG4				
00	317	PRODUCTION RELEASE	[illegible]	[illegible]	[illegible]	[illegible]
01	324	CIRCUIT CHANGES PRODUCTION RELEASE	[illegible]			
02	324 ATT.1	C34-C37 & D9-10 ADDED C18 C29 R22 R35 & R37 REMOVED.	[illegible]		[illegible]	[illegible]
03	346	RESISTOR VALUES & JUMPERS ADDED	[illegible]		[illegible]	[illegible]

DIGITAL POWER AND GROUND TABLE

IC No	TYPE	POWER +5V	POWER -12V	GND	QTY
U9	74HC942 (TMS99532)			19 (18)	1 (1)
U8	MX5089	1		6	1
Q5	MC79L05AC		2	1	1

ANALOG POWER AND GROUND TABLE

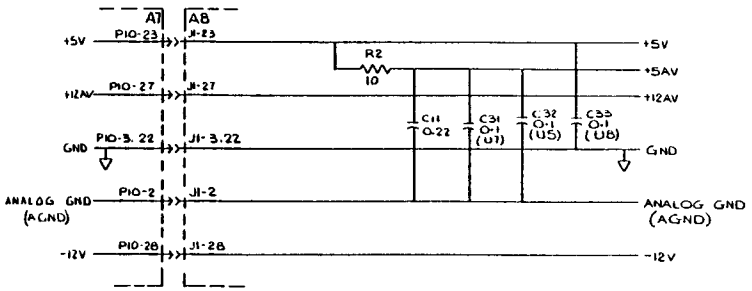
IC No.	TYPE	POWER +5AV	POWER	AGND	QTY
U6	MC14566			7	1
U5, U7	MC3403	4		11	2

HIGHEST DESIGNATIONS USED

C	D	E	K	P	R	T	U	Y	Q
C37	D10	E3	K1	P10	R44	T1	U9	Y1	Q5

HIGHEST DESIGNATIONS NOT USED

C18 C29					R16 R22 R35 R36 R37 R41				Q2



NOTES:
1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, 1/4 W; CAPACITANCE VALUES ARE IN MICROFARADS (μF).

							03	03	REV
							2	1	SHEET
									SHEET INDEX

100012-000	HYPERION
NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS ± 1/32, DECIMALS .X ± .03, .XX ± .010, ANGLES ± 2°
PARTS TO BE FREE FROM BURRS AND SHARP EDGES
UNLESS OTHERWISE SPECIFIED ALL MACHINE SURFACES
MATERIAL
FINISH

DRAWN G.LEVEILLE
CHECKED
ENGINEER
APPROVED
MFG
INITIAL APPLICATION

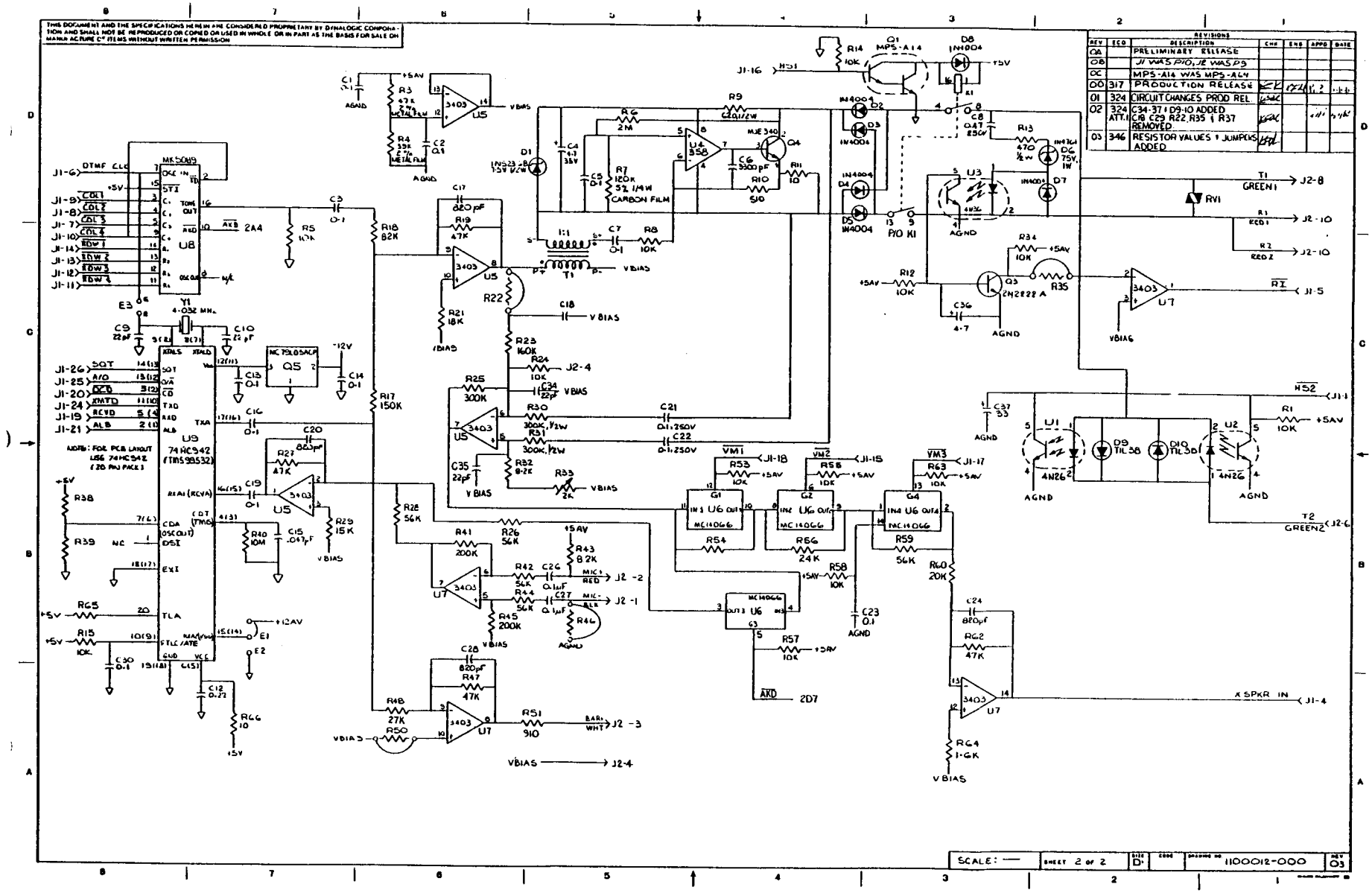
SHEET 1 OF 2

Dynalogic Corporation
Ottawa – Canada

TITLE: SCHEMATIC DIAGRAM MODEM CARD A8

SIZE D | CODE | DRAWING NO. 1100012-000 | REV 03

7.8 Modem Board Rev 04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REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
0A | | PRELIMINARY RELEASE
0B | | J1 WAS P10, J2 WAS P9
0C | | MPS-A14 WAS MPS-A64
00 | 317 | PRODUCTION RELEASE
01 | 324 | CIRCUIT CHANGES PROD REL
02 | 324 | C34-37 & D9-10 ADDED ATT. IC C28 C29 R22, R35 & R37 REMOVED
03 | 346 | RESISTOR VALUES & JUMPERS ADDED
MK50H3
U8
74HC942 (TMS99532)
U5
3403
U6
MC14066
U7
Q1 MPS-A14
Q2 MJE340
Q3 2N2222A
Q5 MC79L05ACP
D1 IN523-8 15V 1/2W
D8 IN4004
D2 IN4004
D3 IN4004
D4 IN4004
D5 IN4004
D7 IN4004
D9 TIL38
D10 TIL38
U1 4N26
U2 4N26
U3
T1
T2
RV1
Y1 4.032 MHz
J1-16
J1-6 DTMF CLK
J1-9 COL 1
J1-8 COL 2
J1-7 COL 3
J1-10 COL 4
J1-14 ROW 1
J1-13 ROW 2
J1-12 ROW 3
J1-11 ROW 4
J1-26 SQT
J1-25 A/D
J1-20 DCD
J1-24 XMTD
J1-19 RCVD
J1-21 ALB
J2-8
J2-10
J1-5
J1-4
J2-4
J2-2
J2-1
J2-3
J1-18
J1-15
J1-17
J1-3
J2-6
2A4
2D7
P/O K1
AGND
VBIAS
+5V
+12V
-12V
SCALE: —
SHEET 2 OF 2
SIZE D
DRAWING NO 1100012-000
REV 03

7.9 Modem Board Rev 07

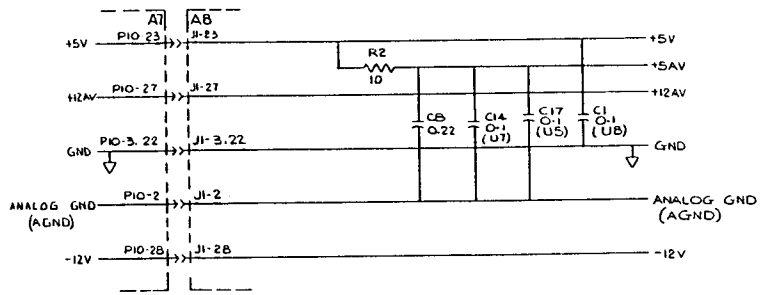
REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
0A		PRELIMINARY RELEASE				
0B		J1 WAS A01; J2 WAS P5				
0C		MP5-A14 WAS MP5-AG 4				
00	317	PRODUCTION RELEASE	KEK	DFH		
01	324	CIRCUIT CHANGES PRODUCTION RELEASE.	KEK	DFH		
02	324 ATT.1	C34-C37 & D9-10 ADDED C18, C29 R22 R35 & R37 REMOVED.	KEK	DFH	4/11/85	
03	346	RESISTOR VALUES & JUMPERS ADDED.	KEK	DFH		
04	356	COMPONENT DESIGNATION CHANGED. CIRCUIT UPDATED NOTE 2 WAS ADDED		CJH	8:12	31-JUL
05	408	R41 WAS 6.150 V RMS 200 VDC C88 WAS 80% 100V 8500PF	KEK		GM	05APR 85
06	439	REFLECT CHANGES MADE TO PWB	KEK	KEK	4/5	24 DEC 85
07	458	CHANGES TO C32	KEK	EH		18 DEC 86

DIGITAL POWER AND GROUND TABLE					
IC No	TYPE	POWER +5V	POWER -12V	GND	QTY
U2	74HC942 (TMS99532)			19 (18)	1 (1)
U1	MK5089	1		6	1
Q1	MC79L05AC		2	1	1

ANALOG POWER AND GROUND TABLE					
IC No.	TYPE	POWER +5AV	POWER	A GND	QTY
U5	MC14066			7	1
U3,U4	MC3403	4		11	2

HIGHEST DESIGNATIONS USED										
C	D	E	K	P	R	T	U	Y	Q	
C37	D10	E3	K1	P10	R64	T1	U9	Y1	Q4	
HIGHEST DESIGNATIONS NOT USED										
					R56 R57					

COMPONENT AVAILABLE ON PCB (NO CONNECTIONS)										
C	D	E	K	P	R	T	U	Y	Q	
C10 C11					R7 R10 R28 R50					
COMPONENTS AVAILABLE ON PCB (WITH CONNECTIONS)										
C26 C3					R3 R4 R1 R37					



NOTES:
1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS. 1/4 W; CAPACITANCE VALUES ARE IN MICROFARADS (μF).
2. SCHEMATIC 110012-000-C7 IS TO BE USED WITH PWA 100012-000-07 AND PWB DRAWING 200014-000-02 ONLY. (BOARD REV IS STILL AT 01).

FIELD SERVICE FILE

PS	DT	REV	SHEET
2	1	SHEET	INDEX

Dynalogic Corporation
Ottawa – Canada

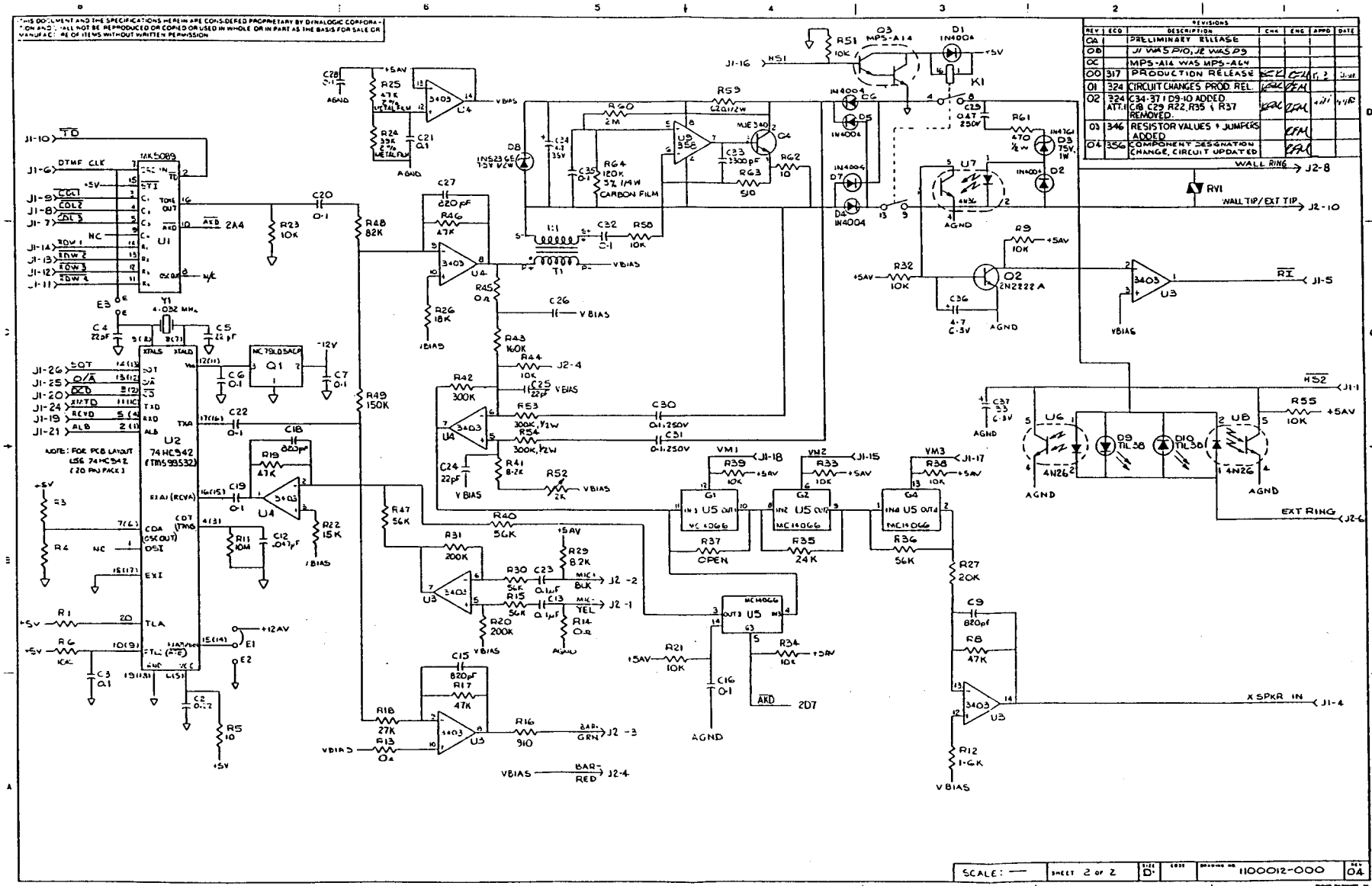
SCHEMATIC DIAGRAM
MODEM CARD A&

110012-000 C7

100012-000 HYPERION
NEXT ASSY USED ON

SHEET 1 OF 2

110012-000-01 SH1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REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
OA | | PRELIMINARY RELEASE
OB | | J1 WAS P10, J2 WAS P9
OC | | MPS-A14 WAS MPS-A64
00 | 317 | PRODUCTION RELEASE
01 | 324 | CIRCUIT CHANGES PROD REL
02 | 324 ATT.1 | C34-37 & D9-10 ADDED. C18, C29, R22, R35 & R37 REMOVED.
03 | 346 | RESISTOR VALUES & JUMPERS ADDED
04 | 356 | COMPONENT DESIGNATION CHANGE, CIRCUIT UPDATED
WALL RING → J2-8
WALL TIP/EXT TIP → J2-10
EXT RING → J2-6
XSPKR IN → J1-4
RI → J1-5
HS1
HS2
TD
DTMF CLK
COL1
COL2
COL3
ROW1
ROW2
ROW3
ROW4
NC
U1
U2
74HC942
(TMS99532)
NOTE: FOR PCB LAYOUT USE 74HC942 (20 PIN PACK)
Y1
4.032 MHz
U3
U4
U5
U6
U7
U8
Q1
Q2
2N2222A
T1
1:1
K1
RV1
D1 IN4004
D2 IN4004
D3 75V 1W
D4 IN4004
D5 IN4004
D6 IN4004
D7 IN4004
D8 INS2365 TSV VCM
D9 TIL38
D10 TIL38
Q3 MPS-A14
Q4 MJE340
4N26
MC14066
AGND
VBIAS
+5V
+12V
-12V
SCALE: —
SHEET 2 OF 2
SIZE D
1100012-000
REV 04

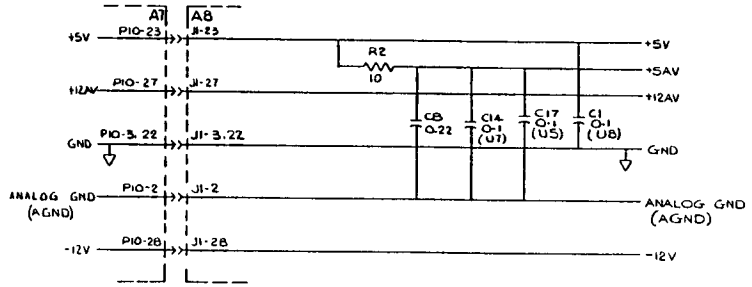
REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
OA		PRELIMINARY RELEASE				
OB		J1 WAS P10; J2 WAS P5				
OC		MP5-A18 WAS MP5-A64				
00	317	PRODUCTION RELEASE				
01	324	CIRCUIT CHANGES PRODUCTION RELEASE.				
02	324 ATT.1	C34-C37 & D9-10 ADDED C18, C29, R22, R35 & R37 REMOVED.				
03	346	RESISTOR VALUES & JUMPERS ADDED.				
04	356	COMPONENT DESIGNATION CHANGED. CIRCUIT UPDATED. NOTE 2 WAS ADDED.				

DIGITAL POWER AND GROUND TABLE					
IC No	TYPE	POWER		GND	QTY
		-5V	-12V		
U2	74HC942 (TMS99532)			19 (18)	1 (1)
U1	MK5089	1		6	1
Q1	MC79105AC		2	1	1

ANALOG POWER AND GROUND TABLE					
IC No.	TYPE	POWER		AGND	QTY
		+5AV			
U5	MC14066			7	1
U3,U4	MC3403	4		11	2

HIGHEST DESIGNATIONS USED											
C	D	E	K	P	R	T	U	Y	Q		
C37	D10	E3	K1	P10	R64	T1	U9	Y1	Q4		
HIGHEST DESIGNATIONS NOT USED											
					R56 R57						

COMPONENT AVAILABLE ON PCB (NO CONNECTIONS)										
C	D	E	K	P	R	T	U	Y	Q	
C10 C11					R7 R16 R28 R50					
COMPONENTS AVAILABLE ON PCB (WITH CONNECTIONS)										
C26 C3					R5 R6 R1 R37					



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, 1/4 W; CAPACITANCE VALUES ARE IN MICROFARADS (μF).
2. SCHEMATIC 1100012-000-04 IS TO BE USED WITH PWA 1000012-000-04 AND PWB 2000014-000-01 ONLY.

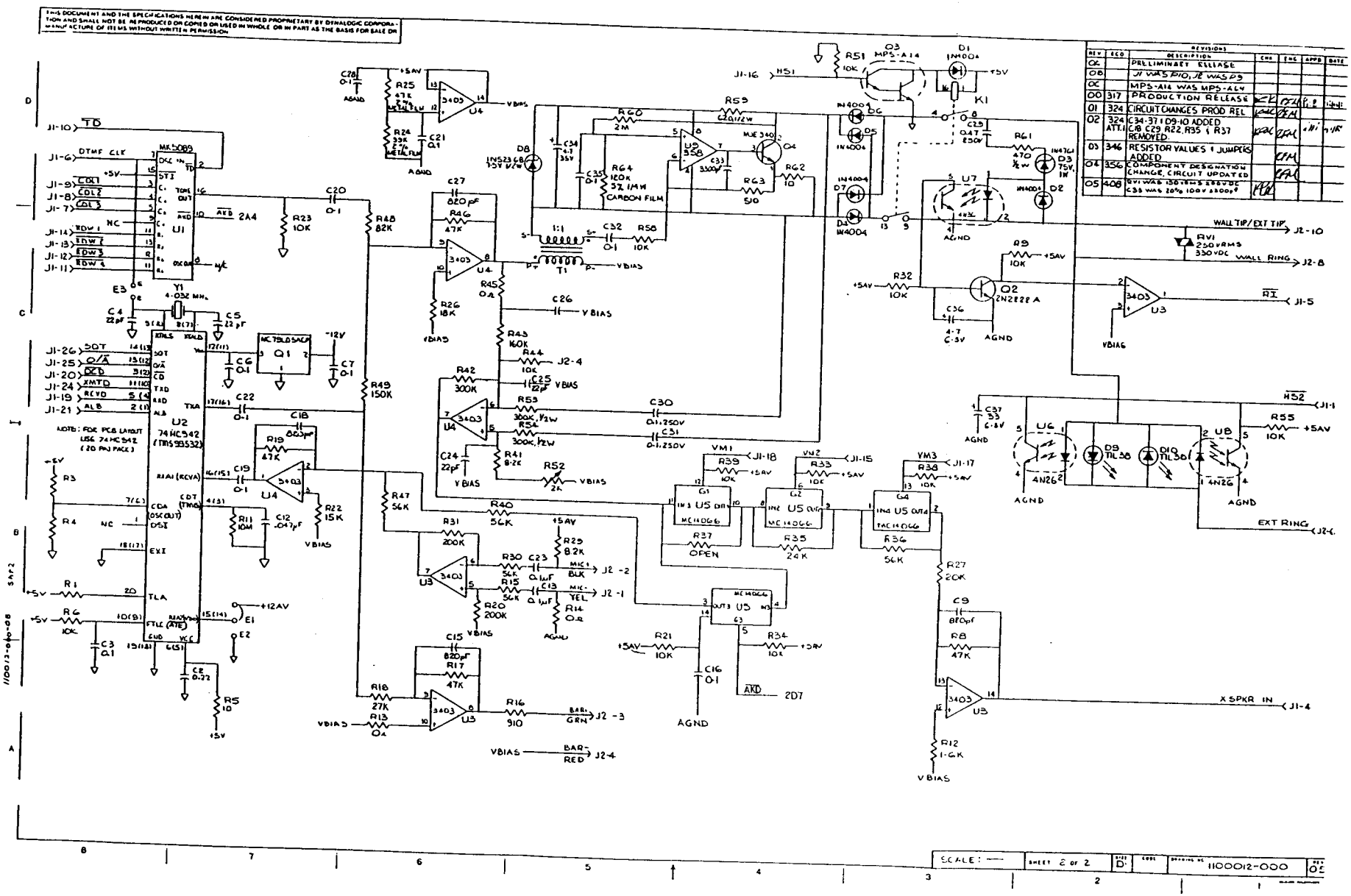
						04	REV
						2 | 1	SHEET | INDEX
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES							
1000012-000	HYPERION						
NEXT ASSY	USED ON						

Dynalogic Corporation
Ottawa – Canada

TITLE: SCHEMATIC DIAGRAM MODEM CARD A8

SIZE: D | CODE | DRAWING NO: 1100012-000 | REV: 04

SHEET 1 OF 2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REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
OA | | PRELIMINARY RELEASE
OB | | J1 WAS P10, J2 WAS P9
OC | | MPS-A14 WAS MPS-A14
00 | 317 | PRODUCTION RELEASE
01 | 324 | CIRCUIT CHANGES PROD REL
02 | 324 ATT.1 | C34-37 & D9-10 ADDED C18 C29 R22, R35 & R37 REMOVED.
03 | 346 | RESISTOR VALUES & JUMPERS ADDED
04 | 356 | COMPONENT DESIGNATION CHANGE, CIRCUIT UPDATED
05 | 408 | D1 WAS 150 mA 2 800 VDC C35 WAS 20% 100 V 3300 pF
MK5089
DTMF CLK
COL1
COL2
COL3
ROW1
ROW2
ROW3
ROW4
XMTD
RCVD
ALB
XTAL1
XTAL2
MC75L05ACP
74HC942 (TMS99532)
NOTE: FOR PCB LAYOUT USE 74HC942 (20 PIN PACK)
MC14066
WALL TIP/EXT TIP
WALL RING
EXT RING
XSPKR IN
AGND
VBIAS
+5V
+12V
-12V
1100012-000
SCALE: —
SHEET 2 OF 2
SIZE D

7.10 Disk Drive

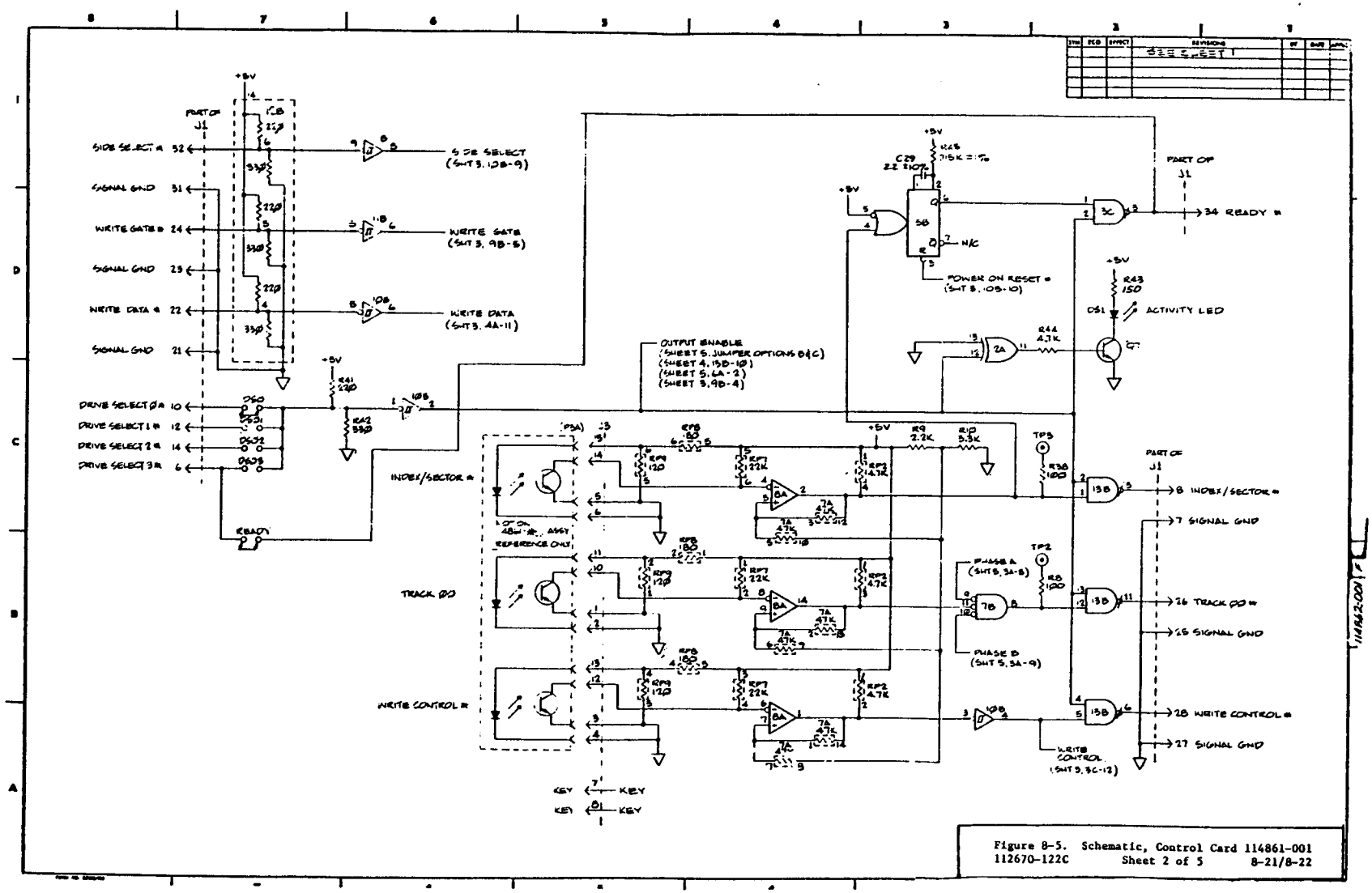


Figure 8-5. Schematic, Control Card 114861-001
112670-122C Sheet 2 of 5 8-21/8-22

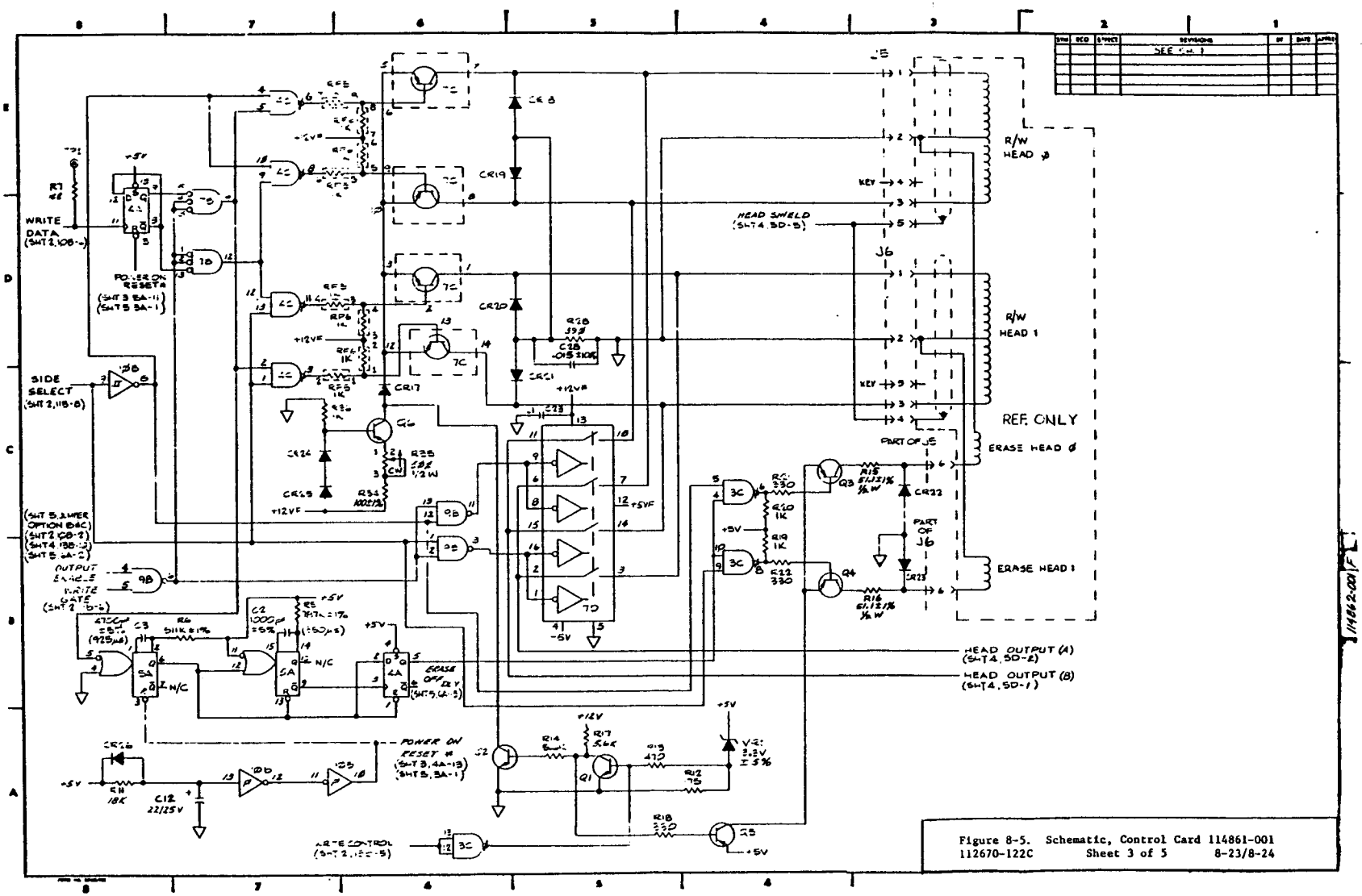


Figure 8-5. Schematic, Control Card 114861-001
112670-122C Sheet 3 of 5 8-23/8-24

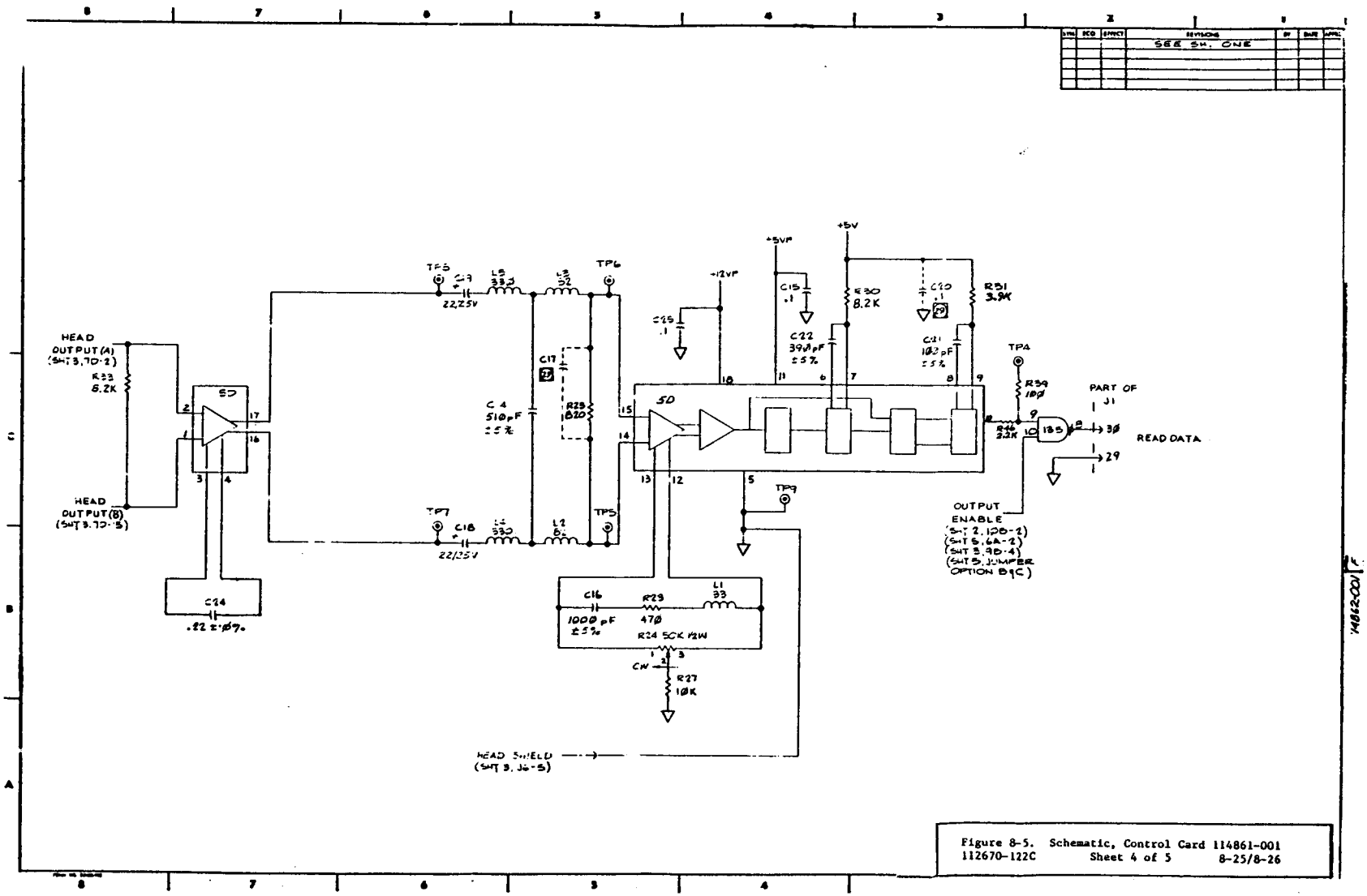


Figure 8-5. Schematic, Control Card 114861-001
112670-122C Sheet 4 of 5 8-25/8-26

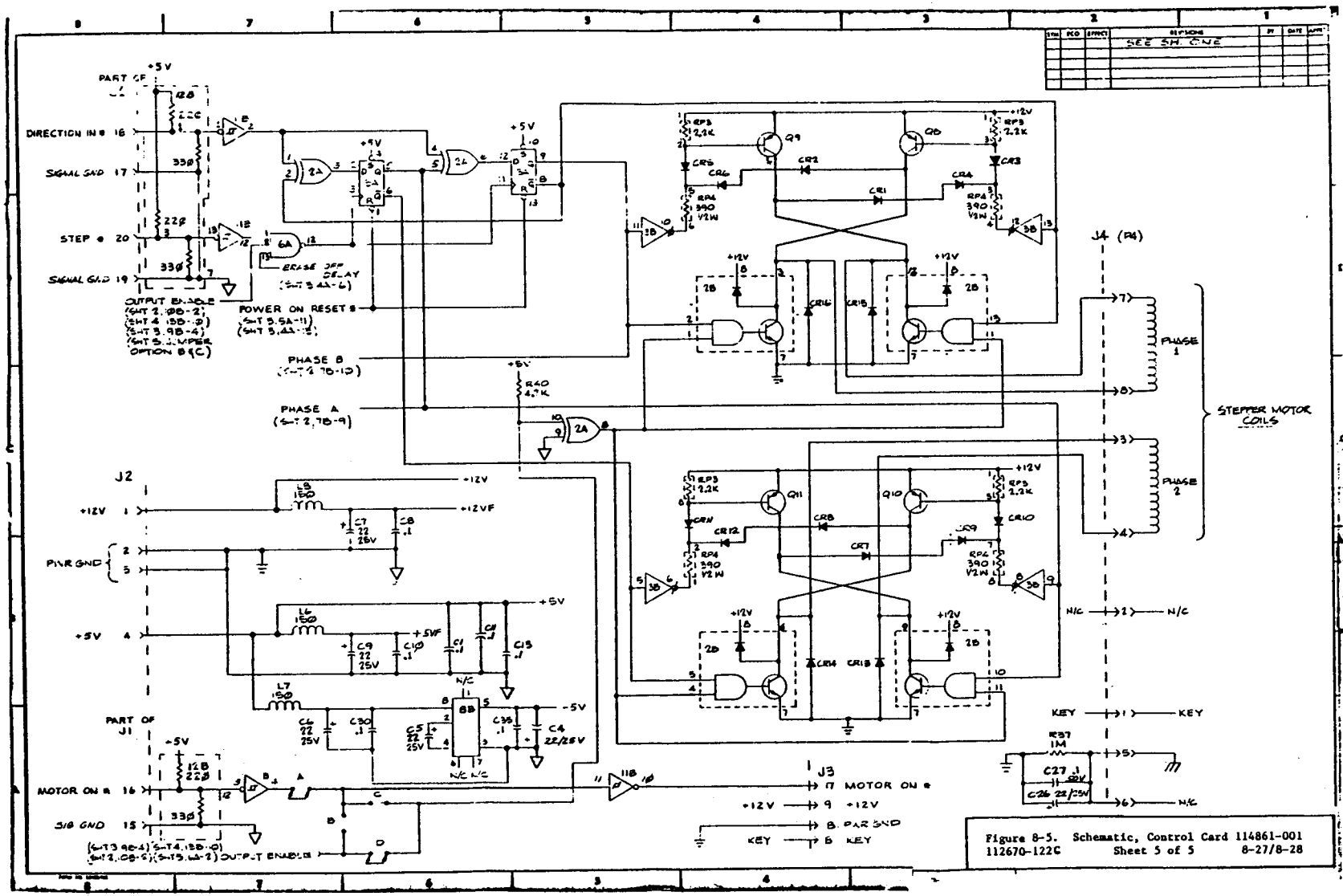
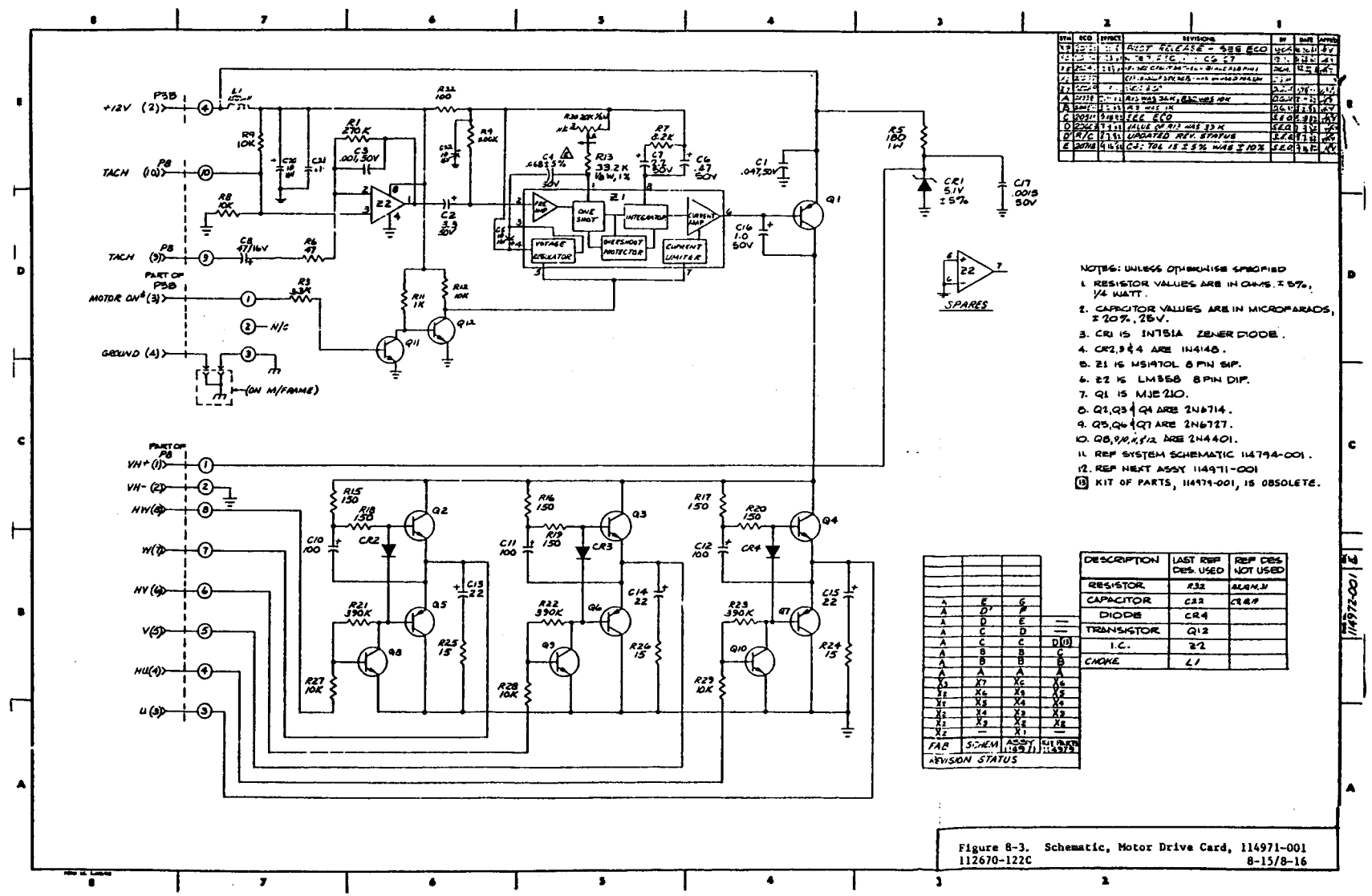


Figure 8-5. Schematic, Control Card 114861-001
112670-122C Sheet 5 of 5 8-27/8-28



STA	ECO	BY/DATE	REVISIONS	BY	DATE	APPVD
1			INITIAL RELEASE - 526 ECO			
2			ADD Z1 ETC. - C6 C7			
3						
4						
A						
B						
C			SEE ECO			
D			VALUE OF R13 WAS 33K			
E			UPDATED REF. STATUS			

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 WATT.
2. CAPACITOR VALUES ARE IN MICROFARADS, ±20%, 25V.
3. CR1 IS IN751A ZENER DIODE.
4. CR2,3 & 4 ARE IN4148.
5. Z1 IS MS1470L 8 PIN SIP.
6. Z2 IS LM358 8 PIN DIP.
7. Q1 IS MJE210.
8. Q1,Q3 & Q4 ARE 2N6714.
9. Q5,Q6 & Q7 ARE 2N6727.
10. Q8,9,10,11,12 ARE 2N4401.
11. REF SYSTEM SCHEMATIC 114794-001.
12. REF NEXT ASSY 114971-001
13. KIT OF PARTS, 114979-001, IS OBSOLETE.

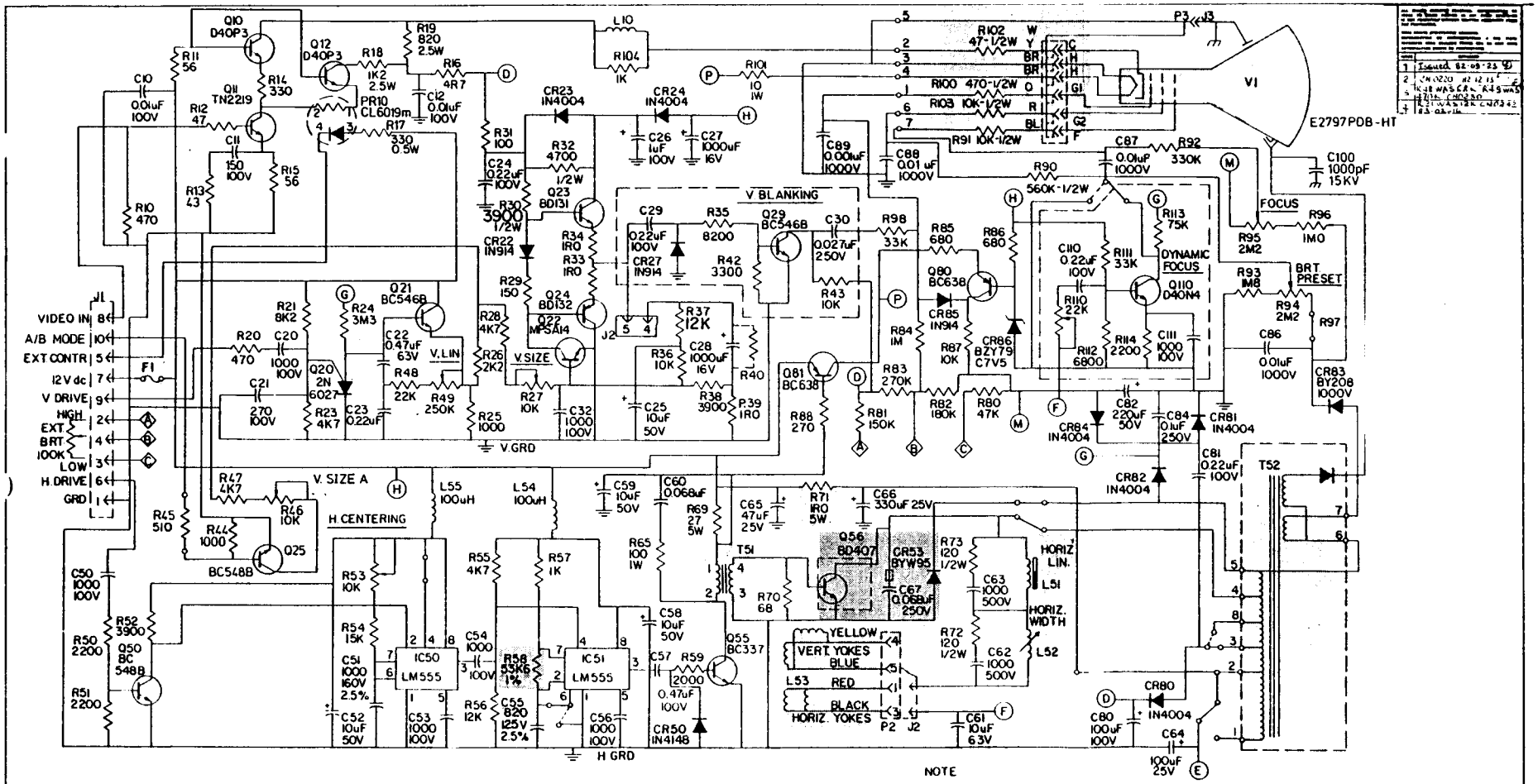
DESCRIPTION	LAST REF DES. USED	REF DES NOT USED
RESISTOR	R32	
CAPACITOR	C33	
DIODE	CR4	
TRANSISTOR	Q12	
I.C.	Z2	
CHOKE	L1	

FAB	SCHEM	ASSY (189)	KIT (189)
REVISION STATUS			

114971-001

Figure 8-3. Schematic, Motor Drive Card, 114971-001
112670-122C 8-15/8-16

7.11 CRT



IMPORTANT SAFETY NOTICE

FOR THE CONTINUED SAFE OPERATION OF THIS PRODUCT, IT IS IMPERATIVE THAT COMPONENTS SHOWN IN THE SHADED AREAS BE REPLACED ONLY WITH THOSE SPECIFIED IN THE PARTS LIST OF THIS MANUAL. USE OF SUBSTITUTE REPLACEMENT PARTS, WHICH DO NOT HAVE THE SAME SAFETY CHARACTERISTICS AS SPECIFIED, MAY CREATE SHOCK, FIRE, X-RADIATION AND OTHER HAZARDS.

FOR MAXIMUM RELIABILITY AND PERFORMANCE, ALL OTHER PARTS MUST BE REPLACED BY THOSE HAVING IDENTICAL SPECIFICATIONS.

UNDER NO CIRCUMSTANCES MAY THE ORIGINAL DESIGN BE MODIFIED OR ALTERED WITHOUT PERMISSION FROM PHILIPS ELECTRONICS LTD.

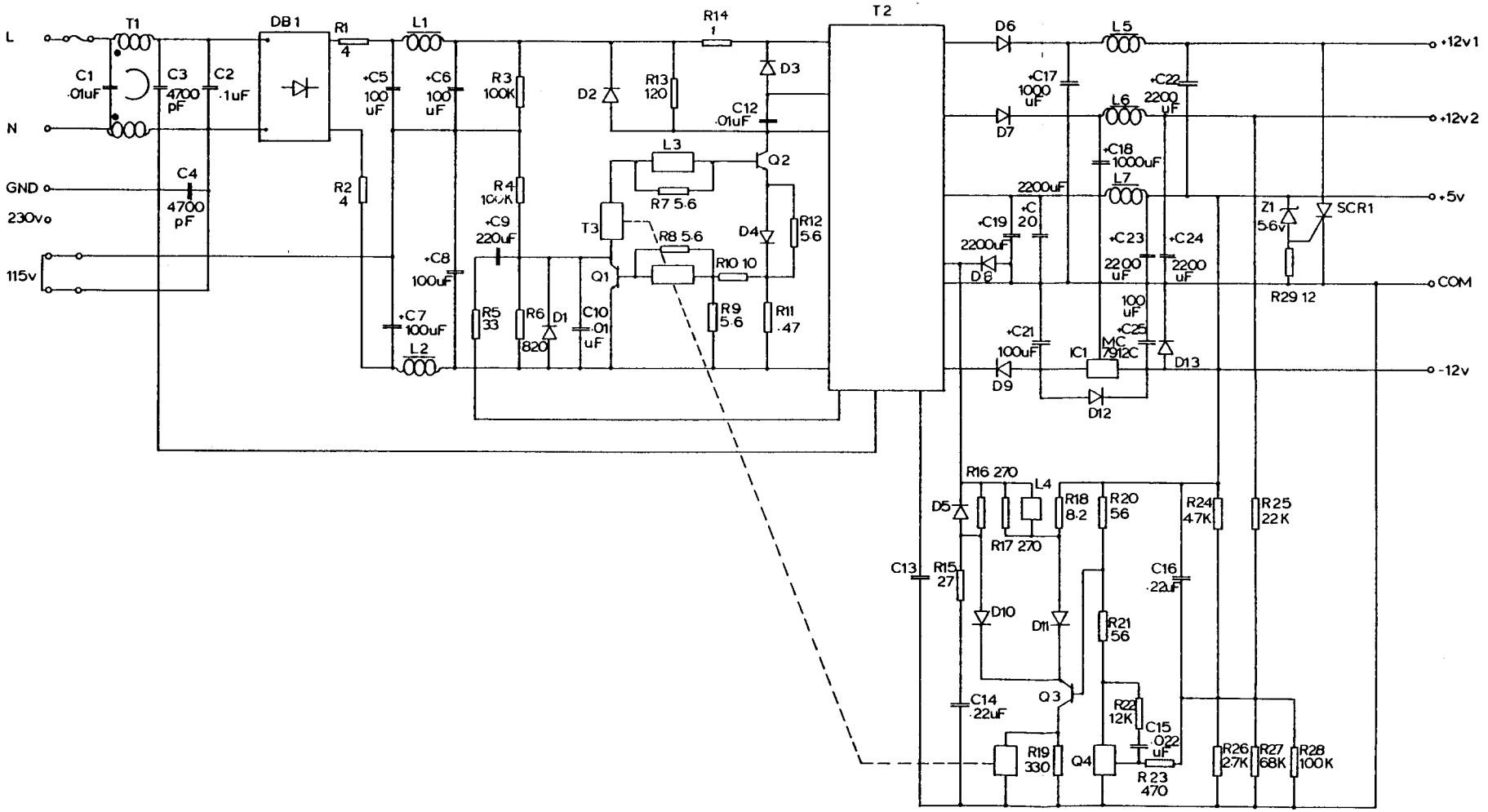
SK 8999

M07P90

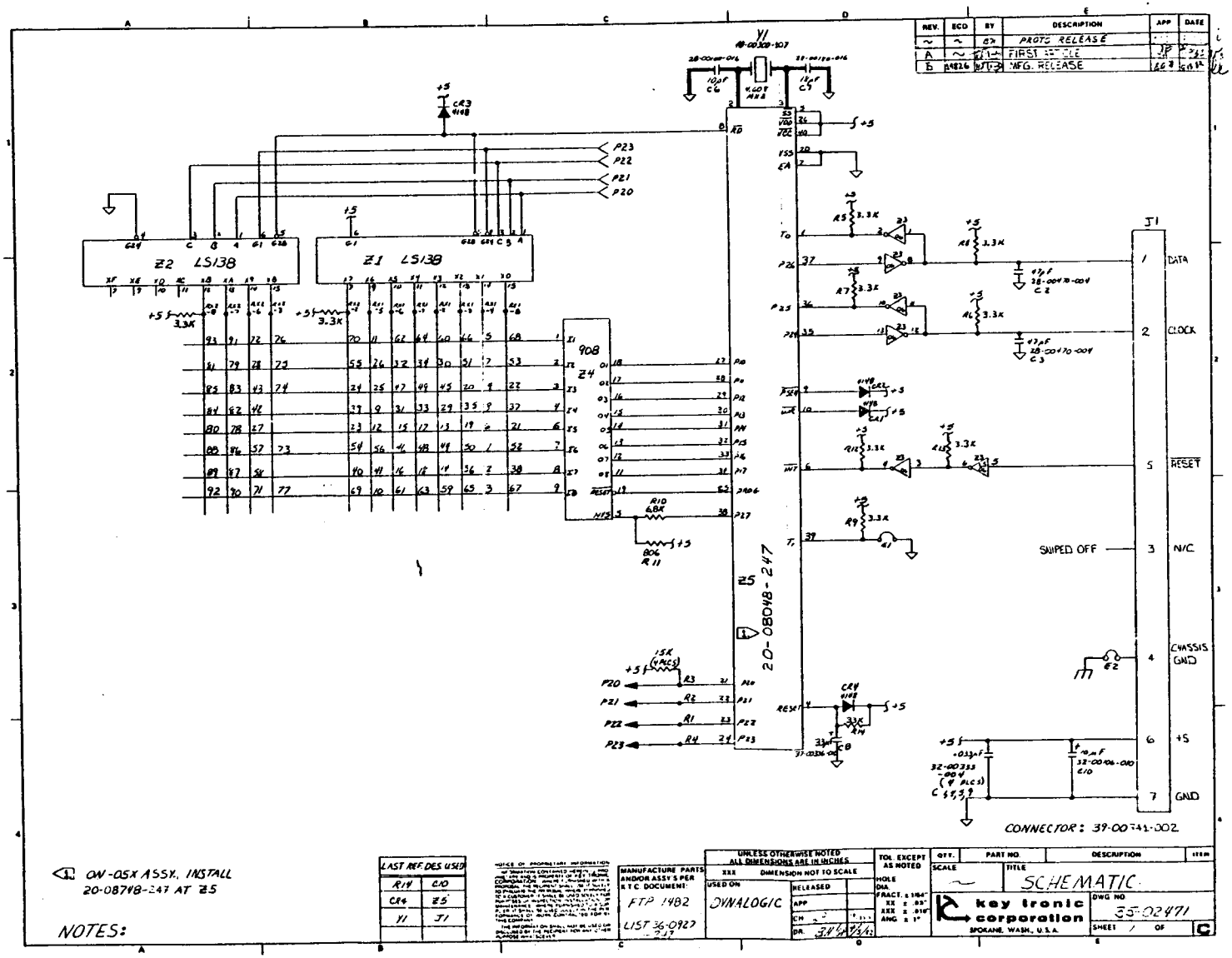
D SCHEMATIC DIAGRAM 7" 90° MONITOR

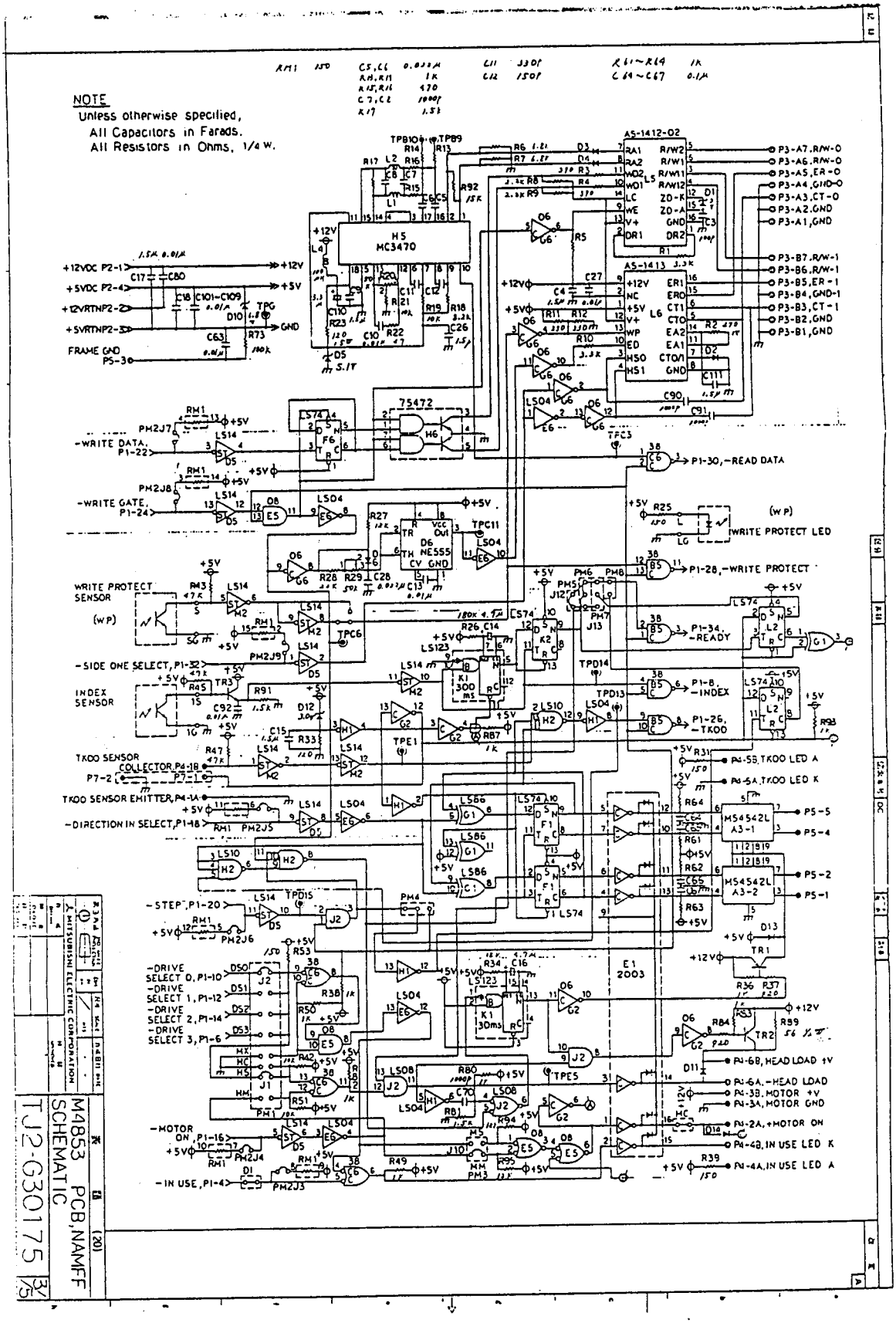
5107 991 00674

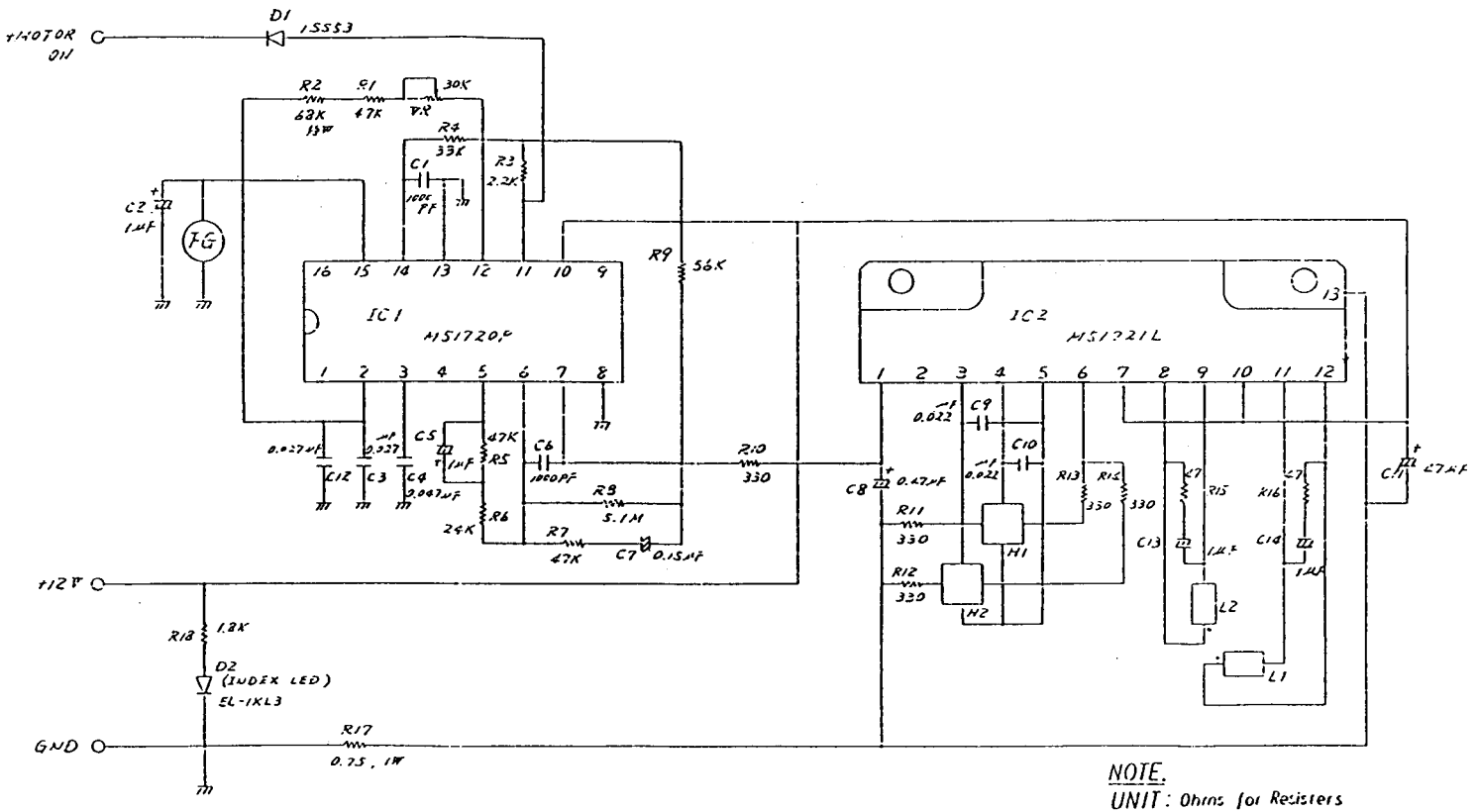
7.12 Power Supply


L
N
GND
230vo
115v
T1
C1 .01uF
C3 4700 pF
C2 .1uF
C4 4700 pF
DB1
R1 4
R2 4
L1
+C5 100 uF
+C6 100 uF
+C8 100uF
+C7 100uF
L2
R3 100K
R4 100K
+C9 220uF
R5 33
R6 820
D1
C10 .01 uF
D2
R13 120
R14 1
D3
C12 .01uF
L3
Q2
R7 5.6
T3
R8 5.6
R10 10
Q1
D4
R12 5.6
R9 5.6
R11 .47
T2
D6
L5
+12v1
+C17 1000 uF
D7
L6
+C22 2200 uF
+12v2
+C18 1000uF
2200uF
L7
+5v
+C19 2200uF
D8
+C 20
+C23 2200 uF
+C24 2200 uF
Z1 5.6v
SCR1
R29 12
COM
100 uF
+C21 100uF
D9
IC1 MC 7912C
+C25
D13
-12v
D12
R16 270
L4
D5
R17 270
R18 8.2
R20 56
R24 47K
R25 22K
C13
R15 27
D10
D11
C16 .22uF
R21 56
C14 .22uF
Q3
R22 12K
C15 022 uF
R19 330
Q4
R23 470
R26 2.7K
R27 68K
R28 100K

7.13 Keyboard


Z2 LS138
Z1 LS138
Z4 908
Z5 20-08048-247
J1
DATA
CLOCK
RESET
N/C
SWIPED OFF
CHASSIS GND
+5
GND
CONNECTOR: 39-00741-002
SCHEMATIC
key tronic corporation
SPOKANE, WASH., U.S.A.
DWG NO 35-02471
DYNALOGIC
FTP 1482
LIST 36-0927
NOTES:
1. ON-05X ASSY, INSTALL 20-08048-247 AT Z5


NOTE
Unless otherwise specified,
All Capacitors in Farads.
All Resistors in Ohms, 1/4 W.
M5 MC3470
75472
AS-1412-02
AS-1413
+12VDC P2-1
+5VDC P2-4
+12VRTNP2-2
+5VRTNP2-3
FRAME GND PS-3
-WRITE DATA, P1-22
-WRITE GATE, P1-24
WRITE PROTECT SENSOR
-SIDE ONE SELECT, P1-32
INDEX SENSOR
TK00 SENSOR COLLECTOR, P4-1B
TK00 SENSOR EMITTER, P4-1A
-DIRECTION IN SELECT, P1-18
-STEP, P1-20
-DRIVE SELECT 0, P1-10
-DRIVE SELECT 1, P1-12
-DRIVE SELECT 2, P1-14
-DRIVE SELECT 3, P1-6
-MOTOR ON, P1-16
-IN USE, P1-4
P1-30, -READ DATA
P1-28, -WRITE PROTECT
P1-34, -READY
P1-8, -INDEX
P1-26, -TK00
P3-A7, R/W-0
P3-A6, R/W-0
P3-A5, ER-0
P3-A4, GND-0
P3-A3, CT-0
P3-A2, GND
P3-A1, GND
P3-B7, R/W-1
P3-B6, R/W-1
P3-B5, ER-1
P3-B4, GND-1
P3-B3, CT-1
P3-B2, GND
P3-B1, GND
P4-5B, TK00 LED A
P4-5A, TK00 LED K
P4-6B, HEAD LOAD +V
P4-6A, -HEAD LOAD
P4-3B, MOTOR +V
P4-3A, MOTOR GND
P4-2A, +MOTOR ON
P4-4B, IN USE LED K
P4-4A, IN USE LED A
WRITE PROTECT LED
PS-5
PS-4
PS-2
PS-1
MITSUBISHI ELECTRIC CORPORATION
M4853 PCB, NAMFF
SCHEMATIC
TJ2-G30175



NOTE.
UNIT : Ohms for Resisters
Rotation speed : 300RPM

MITSUBISHI ELECTRIC CORPORATION

M4853 SPINDLE MOTOR ASSY SCHEMATIC

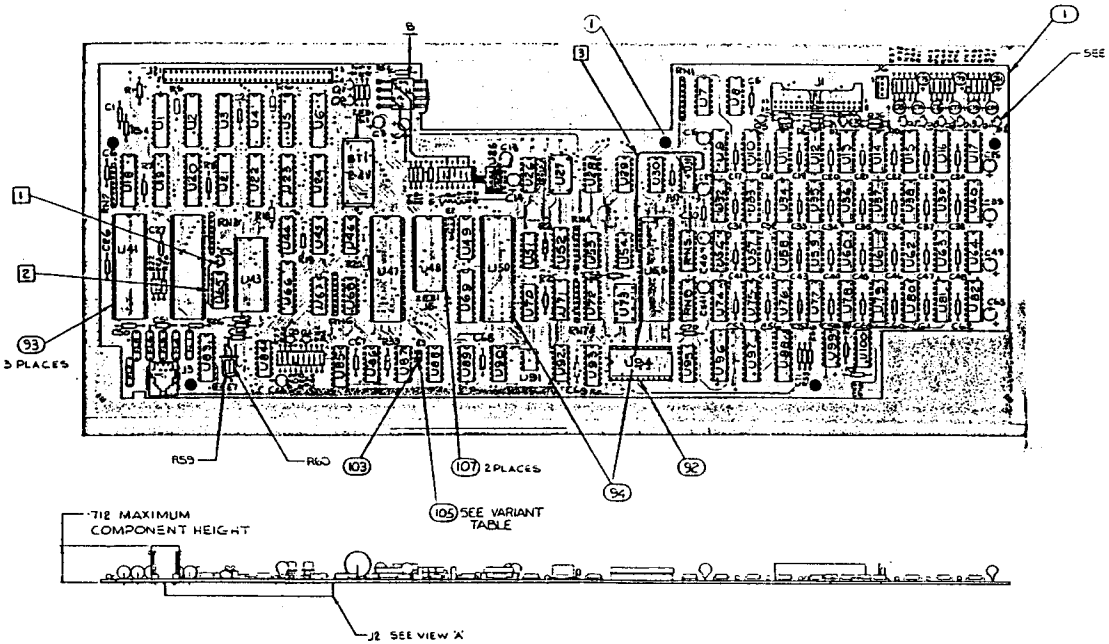
T12-G30175 5/

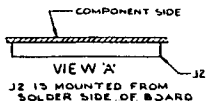
PLASTIC PACKAGE
TO-92

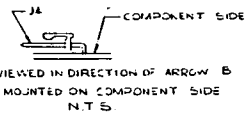
DETAIL 'A'
INSTALL PLASTIC PACKAGE OPPOSITE TO WHAT IS INDICATED ON SILKSCREEN (FOR Q1 TO Q2, Q5, Q10 ETC)
NTS

METAL PACKAGE
TO-18

DETAIL 'B'
INSTALL METAL PACKAGE AS SHOWN ABOVE FOR Q1 TO Q6, Q8, Q10 ETC
NTS







REVISIONS						
REV	ECO	ZONE	DESCRIPTION	CHK	ENG	APPD	DATE
01	315		PRODUCTION RELEASE				
02	321		TRACKS CUT 12 JUMPERS ADDED R35 Q5 ADDED				
03	320		JUMPERS 4 NOTE 5 ADDED				
04	330		FAN CIRCUITRY ADDED C33 DELETED				
05	345		9 JUMPERS ADDED				
06	347		NOTE 5 ADDED E5-1 E5-2 JUMPER E5-1 E5-3 ADDED				
07	378		PIN OF C1, 2, 5, 6, 15, C22, 23 & C44 - 71 CHANGED				
08	387		ADDED JUMPER				
09	392		ADDED JUMPERS 1 & 2				
10	393		ADDED U99 & U100, R55-58 DELETE R55, R54, Q5, Q6 AND Q7				
11	436		ITEM 104 AT E5-2, E5-3 ITEM 120 ADDED AT E5-1, E5-3				
12	45		VARIANT TABLE ADDED				
13	468		ADDED JUMPERS E6, E7 & E8.				
14	511		JUMPER ADDED TO U31-12. TRACK CUT AT U31-12. ADDED Q5, Q6 R55, R54, D5 & D7			W.L.S.	
14.1	521		U46 WAS BIOS RELEASE 53				
14.2	527	87,88	R55 & R60 ADDED, C44 CHANGED FROM [illegible]				

NOTES:
1. FOR ITEM No'S REFER TO BILL OF MATERIAL 100004-000 SHEET 2.
2. REFERENCE SCHEMATIC DIAGRAM 110004-000-14
3. OBSERVE POLARITY OF CAPACITORS, DIODES AND BATTERY BT1.
4. MARK ASSEMBLY REVISION AND SERIAL No.___ DURING ASSEMBLY IN WHITE EPOXY INK.
5. PWA 100004-000 IS TO BE USED WITH SCHEMATIC 110004-000 AND PWB DRAWING 200003-000.

PART NUMBER	DISK DRIVE	JUMPER PLUS ITEM #105
100004-001	SINGLE DRIVE	YES
100004-000	DOUBLE DRIVE	NO

VARIANT TABLE

JUMPER TABLE					
WIRE NO.	FROM	TO	REMARKS	100001-000 NEXT ASSY	HYPERION USED ON
1	U31-12	U53-9	TRACK CUT		
2	E5-1	E5-3	ITEM 120		
3	E5-2	U65-7	ITEM 120		
3	U31-12	U55-7	ITEM 120		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS: ±
DECIMALS: .XX ± .XXX ±
ANGLES: ±
METRIC: .XX ± .XXX ±
PARTS TO BE FREE OF BURRS BREAK ALL EDGES .010

DRAWN G. LEVEILLE
CHECKED
ENGINEER
APPROVED
SCALE: 1/1
SHEET 1 OF 2
SIZE D

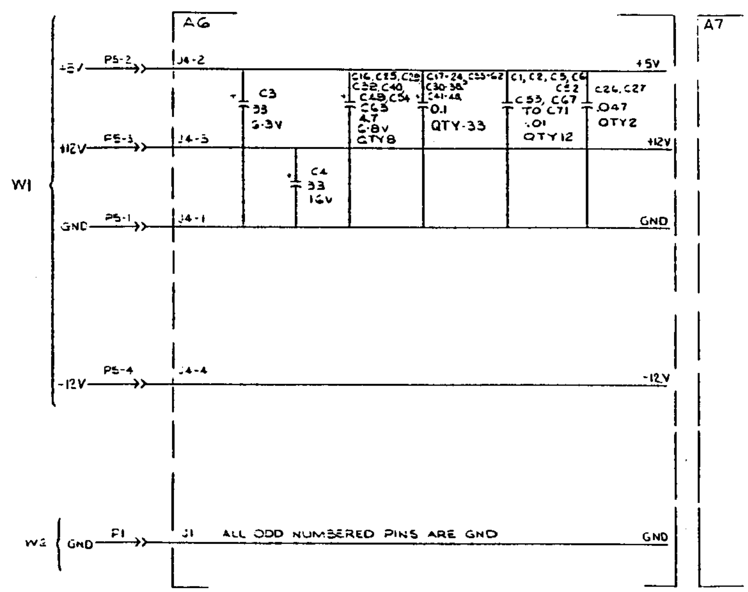
Dynalogic
Dynalogic Into-Tech Corporation
Ottawa Canada

TITLE
PWA
SYSTEM CARD AG

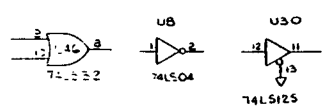
CODE
DRAWING NO. 100004-000
REV 14.2

POWER AND GROUND TABLE

IC No.	TYPE	POWER	GROUND	QTY
U55	Am29645	10	30	1
U91	FDC9216B	8	4	1
U9-U17, U32-U40, U56-U64, U74-U82	2164A-20	8	16	36
U22-U24	PAL10L8	20	10	3
U73	RCLL-13XX	14	7	1
U47	8237A-5	31	20	1
U42	8087	40	1,20	1
U41	8088	40	1,20	1
U94	8253A-5	24	12	1
U43	8259A-5	28	14	1
U50	8272	40	20	1
U83	8284A	18	9	1
U18	8288	20	10	1
U48	2764A-3	28	14	1
U71	74LS161A	16	8	1
U52	74LS195A	16	8	1
U95	74LS280	14	7	1
U96	74LS322A	20	10	1
U49	74LS670	16	8	1
U72 U85, U93	74LS175	16	8	3
U19-U21, U69	74LS373	20	10	4
U65	74LS30	14	7	1
U53	74LS00	14	7	1
U92	74LS02	14	7	1
U87, U90	74LS04	14	7	2
U26, U54, U84	74LS08	14	7	3
U7, U68, U89	74LS14	14	7	3
U46	74LS32	14	7	1
U100	74LS373	14	7	1
U30, U64, U88	74LS125	14	7	3
U1-U5, U97, U98	74LS244	20	10	7
U6, U66	74LS245	20	10	2
U45	74ALS74	14	7	1
U25	LM386	6	4	1
U44	74ALS00	14	7	1
U8	74S04	14	7	1
U28 U29 U31 U50 U70 U27 U29	74LS74	14	7	7



SPARE GATES



HIGHEST DESIGNATIONS USED										
ET	C	D	E	FL	J	Q	R	RN	U	Y
ET1	C81	D8	E8	FL6	J6	Q13	R60	RN5	U100	Y1
HIGHEST DESIGNATIONS NOT USED										
	C29 C15	D1 C2	E4			Q5 Q6	R14 R53 R12			

REVISIONS

REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
9A		PRELIMINARY RELEASE				
9B		CIRCUIT & DESIG. CHANGES				
0A		CIRCUIT & DESIG. CHANGES				
00	315	PRODUCTION RELEASE				
01	321	CIRCUIT UPDATE				
02	ATT3 321	SHT 5 ZONE C5 & A6 U3 WAS 74LS04	KSL			
03	320	FAN CIRCUITRY JUMPERS ADDED				
04	330	FULL FAN CIRCUITRY ADDED				
05	345	R14 DELETED. R10, R12 & R13 VALUES CHANGED. R11 & R13 GROUNDED.				
06	347	NOTE 2 ADDED; SHT2 - JUMPER OPTION ADDED; SHT4 - R16 WAS JUMPER				
07	373	SHT 1 - R53 ADDED TO NOT USED COLUMN; SHT2 - RESISTOR BETWEEN Q2-BASE (Q1-COLLECTOR) WAS R35				
08	392	ADDED JUMPER FROM E5-1 TO E6-3				
10	393	ADDED U85 CU150 UPDATED CIRCUITRY				
11	435	SHT 2, 5 & 7 IMPROPER DESIGNATIONS SHEET 2 E5 REJUMPER				
12	461	C8, C10 CHANGED.				
13	468	JUMPERS E6, E7 AND E8 ADDED				
14	511	U31-12 CONNECTION CHANGED. ADDED Q5, Q7, R35, R54, Q5 & Q7			MLS	
14.2	527	ANALOG GND REMOVED. HIGHEST RESISTOR DESIG WAS R58. R59 & R60 ADDED. C64 CHANGED FROM 12pf TO 27pf				

NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, 1/4 W; CAPACITANCE VALUES ARE IN MICROFARADS.
2. SCHEMATIC 110004-000 IS TO BE USED WITH PWA 100004-000 AND PWB DRAWING 200003-000.

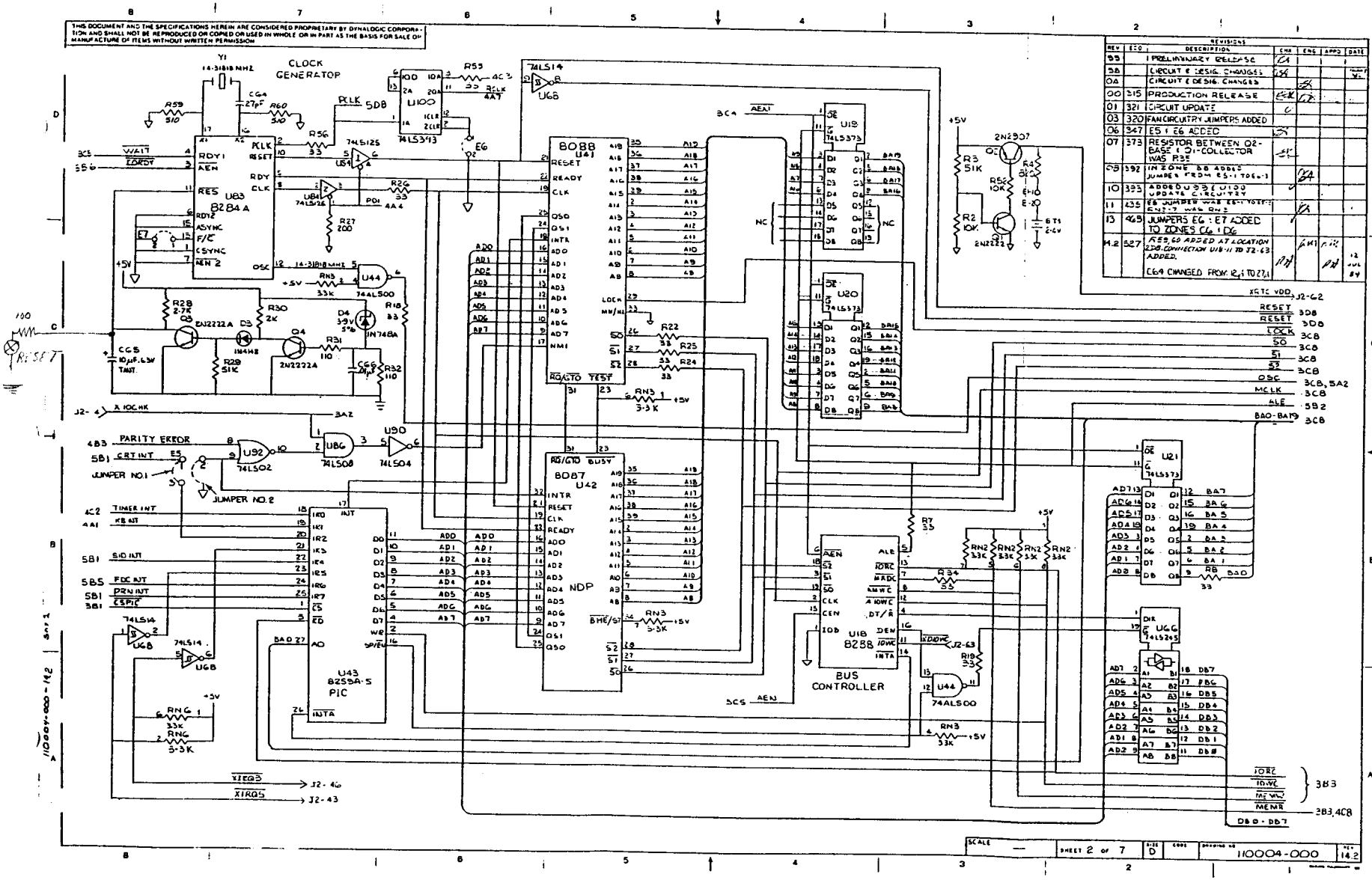
NEXT ASS'Y	USED ON
100004-000	HYPERION

Drawn: GL/KSK
Sheet 1 of 7

Dynalogic Corporation
Ottawa - Canada

SCHEMATIC DIAGRAM
SYSTEM CARD A6

Size: D
Drawing No. 110004-000
Rev. 14.2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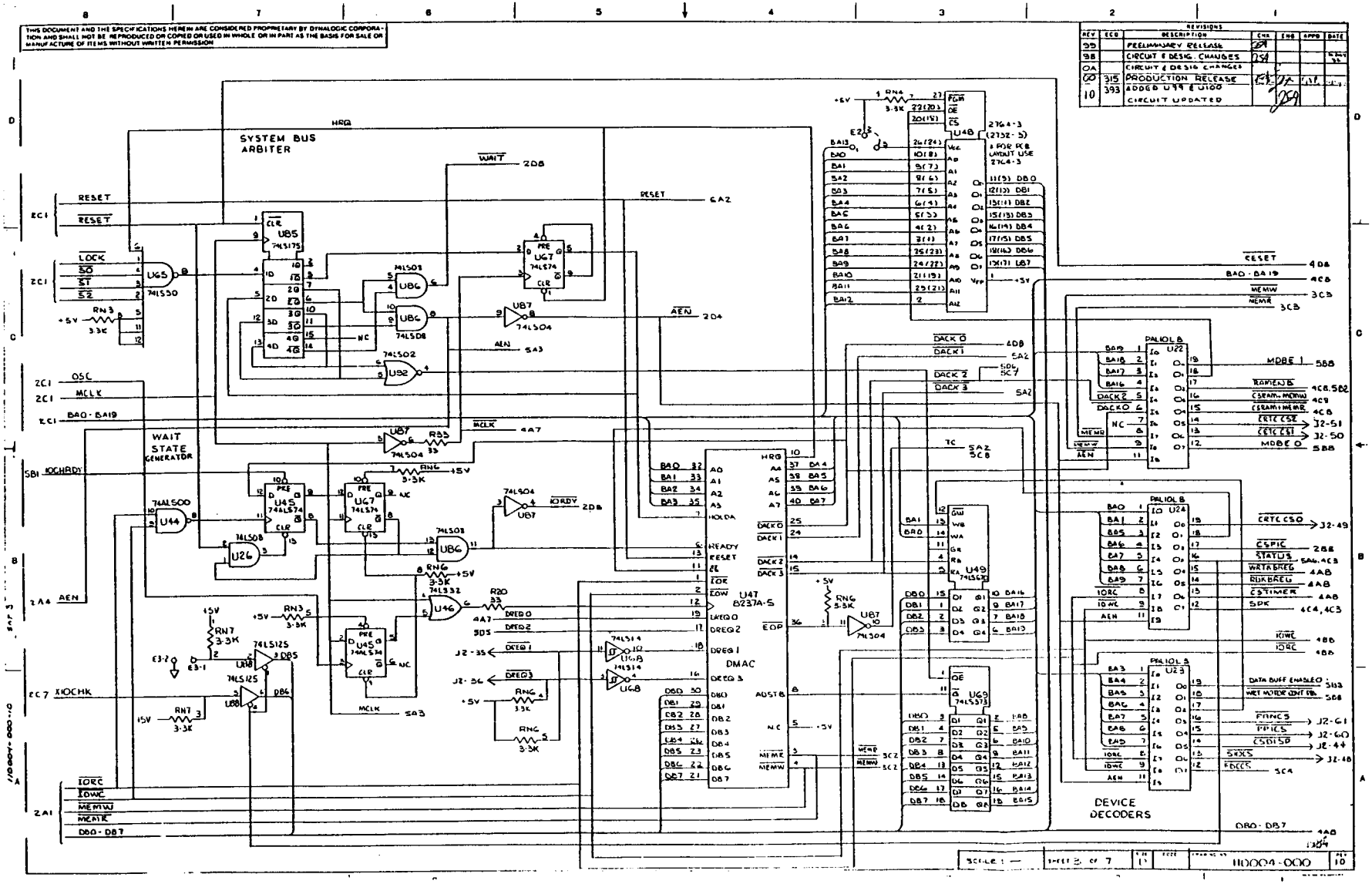
REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
PRELIMINARY RELEASE
CIRCUIT & DESIG. CHANGES
CIRCUIT & DESIG. CHANGED
00 315 PRODUCTION RELEASE
01 321 CIRCUIT UPDATE
03 320 FAN CIRCUITRY JUMPERS ADDED
06 347 E5 & E6 ADDED
07 373 RESISTOR BETWEEN Q2-BASE & Q1-COLLECTOR WAS R35
08 392 IN ZONE B8 ADDED JUMPER FROM E5-1 TO E5-3
10 393 ADDED U38 & U100 UPDATE CIRCUITRY
11 435 E8 JUMPER WAS E5-1 TO E5-3 NOW E5-2 TO E5-3
13 465 JUMPERS E6 : E7 ADDED TO ZONES C6 & D6
14.2 527 R59, 60 ADDED AT LOCATION 2.2K CONNECTION U18-11 TO J2-63 ADDED. C69 CHANGED FROM 12μf TO 27μf
CLOCK GENERATOR
Y1 14.31818 MHZ
C64 27pF
R59 510
R60 540
R56 33
RCLK 5D8
74LS125
74LS393
U100
R55 4K3
RCLK 4A7
74LS14 U68
WAIT
EORDY
RDY1
AEN
RES
U83 82B4A
RDY2
ASYNC
F/C
CSYNC
AEN 2
OSC
14.31818 MHZ
R26 33
U84 74LS126
PD1 4A4
R27 200
+5V
RN3 33K
U44 74LS00
R28 2.7K
R30 2K
Q3 2N2222A
D3 1N4448
Q4 2N2222A
R29 51K
R31 110
D4 3.9V 5% 1N748A
R18 33
C65 10μF, 6.3V TANT.
C66 .01μF
R32 110
RESET
100
J2-4 A IOCHK
3A2
4B3 PARITY ERROR
5B1 CRT INT
JUMPER NO.1
JUMPER NO.2
U92 74LS02
U86 74LS08
U90 74LS04
4C2 TIMER INT
4A1 KB INT
5B1 SIO INT
5B5 FDC INT
5B1 PRN INT
5B1 ESPIC
74LS14 U68
74LS14 U68
RN6 33K
RN6 5-3K
U43 8259A-5 PIC
INT
IR0 IR1 IR2 IR3 IR4 IR5 IR6 IR7
D0 D1 D2 D3 D4 D5 D6 D7
CS RD WR SP/EN
BAD 27 A0
INTA
XIRQ3 → J2-46
XIRQ5 → J2-43
U41 8088
RESET READY CLK SS0 QS1 INTR AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 NMI
A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8
LOCK MN/MX
S0 S1 S2
RQ/GT0 TEST
R22 33
R25 33
R24 33
RN3 3-3K +5V
U42 8087 NDP
INTR RESET CLK READY AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 QS1 QS0
BUSY
BHE/S7
U18 74LS373
U20 74LS373
U21 74LS373
NC
3C4 AEN
3C5 AEN
U18 8288 BUS CONTROLLER
AEN CEN IOB
ALE MADC AMWC AIOWC DT/R DEN IOWC INTA
R7 33
RN2 33K
R34 33
R19 33
U44 74LS00
U66 74LS245
DIR
R8 330
R4 470
R5 10K
R3 51K
R2 10K
2N2907
2N2222
6T1 2.6V
XBTC VDD → J2-62
RESET 3D8
RESET 3D8
LOCK 3C8
S0 3C8
S1 3C8
S2 3C8
OSC 3C8, 5A2
MCLK 3C8
ALE 5B2
BA0-BA19 3C8
IOBZ
IOWC
MEMW
MEMR
383, 4C8
DB0 - DB7
SCALE —
SHEET 2 of 7
SIZE D
DRAWING NO 110004-000
REV 14.2



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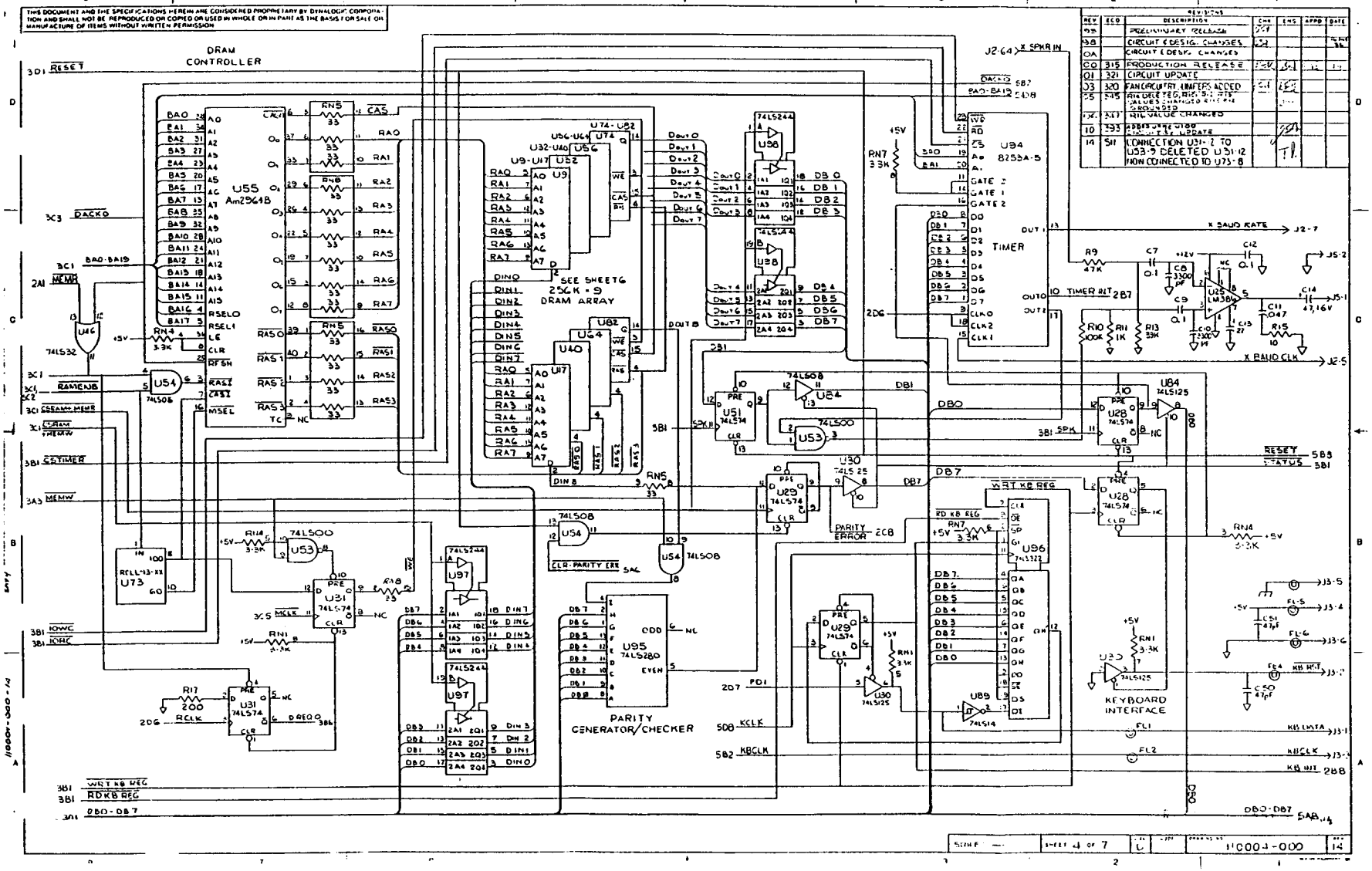
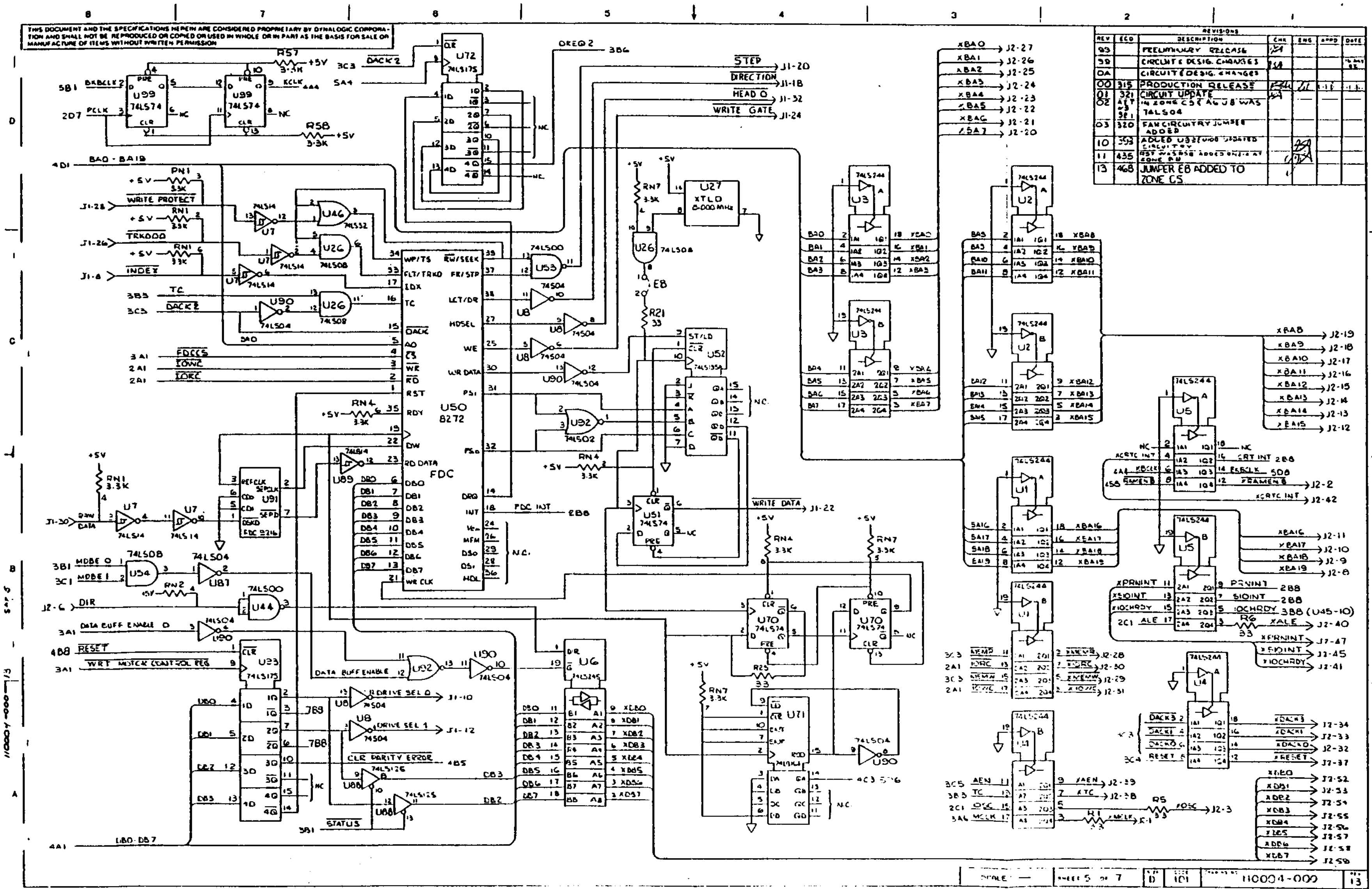
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
95		PRELIMINARY RELEASE				
98		CIRCUIT & DESIG. CHANGES				
0A		CIRCUIT & DESIG CHANGES				
00	315	PRODUCTION RELEASE				
10	393	ADDED U99 & U100 CIRCUIT UPDATED				


DRAM CONTROLLER
U55 Am2964B
U54 74LS08
U46 74LS32
U73 RCLL-13-XX
U31 74LS74
U53 74LS00
U97 74LS244
U74-U82
U32-U40 U56
U9-U17 U52
SEE SHEET6
256K-9 DRAM ARRAY
U51 74LS74
U38 74LS244
U84 74LS244
U84 74LS125
U28 74LS74
U29 74LS74
U30 74LS 25
U95 74LS280 EVEN
PARITY GENERATOR/CHECKER
U94 8253A-5
TIMER
U96 74LS323
U89 74LS14
U30 74LS125
U23 74LS125
KEYBOARD INTERFACE
U25 LM386
RESET
DACKO
MEMR
MEMW
IOWC
IORC
RCLK
DREQ0
PDI
KCLK
KBCLK
PARITY ERROR
CLR PARITY ERR
WRT KB REG
RD KB REG
RESET STATUS
X SPKR IN
X BAUD RATE
X BAUD CLK
TIMER INT
KB DATA
KB INT
DB0-DB7
BA0-BA19
SHEET 4 OF 7
11000-000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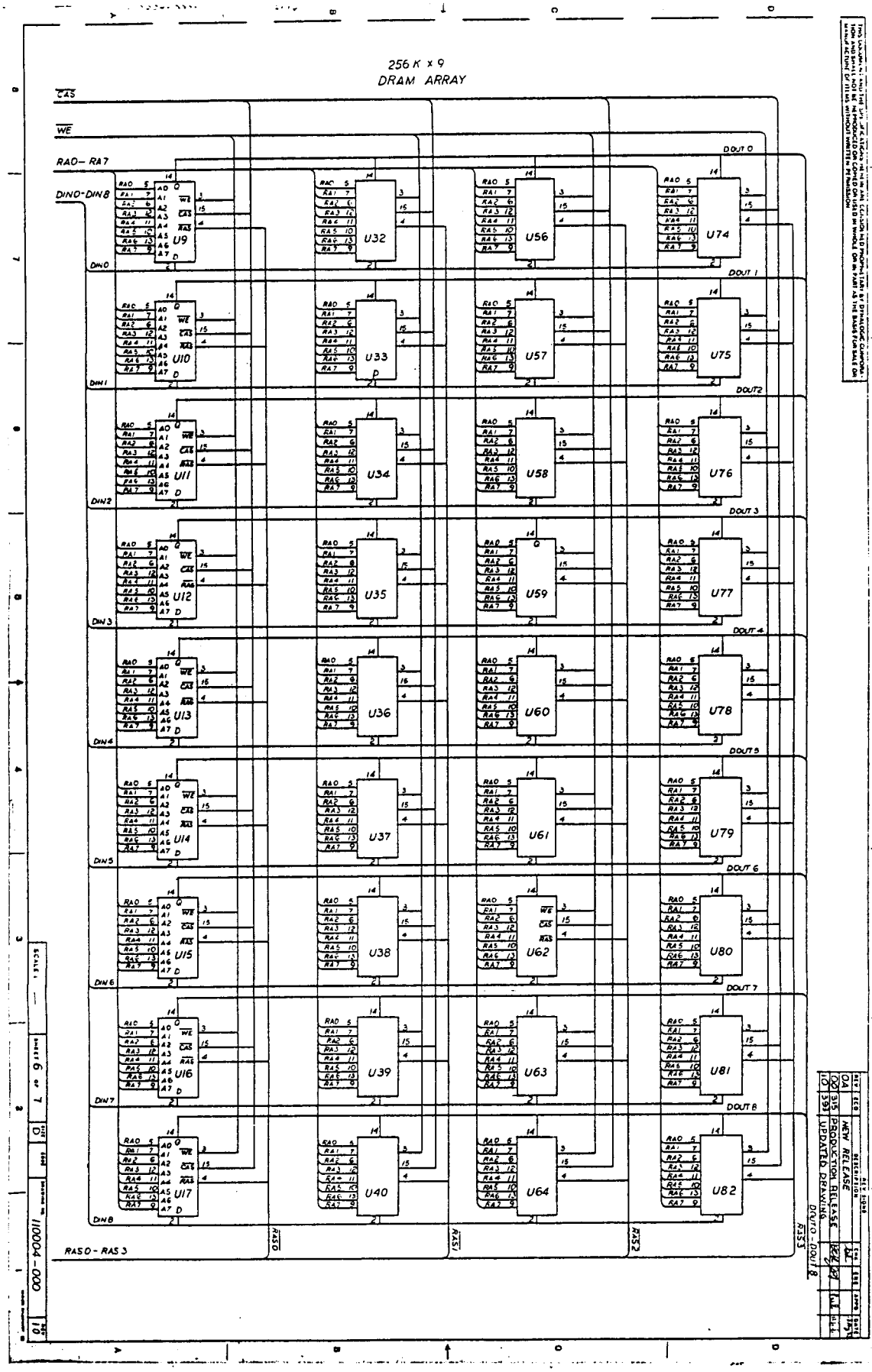
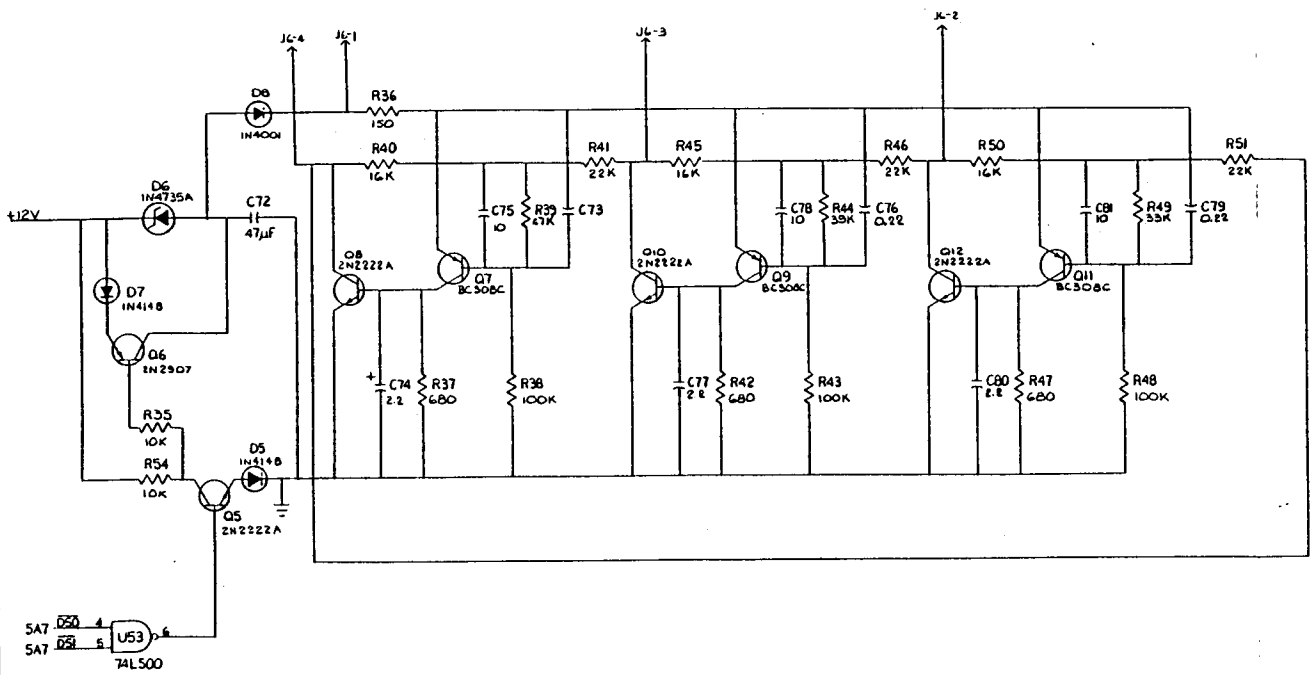
REVISIONS
REV ECO DESCRIPTION
93 PRELIMINARY RELEASE
99 CIRCUIT DESIG. CHANGES
0A CIRCUIT DESIG. CHANGES
00 315 PRODUCTION RELEASE
01 321 CIRCUIT UPDATE
03 320 FAN CIRCUITRY JUMPER ADDED
10 353
11 435
13 468 JUMPER EB ADDED TO ZONE C5
U50 8272 FDC
U27 XTLO 8.000 MHz
WRITE PROTECT
TRK000
INDEX
STEP
DIRECTION
HEAD 0
WRITE GATE
WRITE DATA
FDC INT
DATA BUFF ENABLE
DRIVE SEL 0
DRIVE SEL 1
CLR PARITY ERROR
STATUS
RESET
WRT MOTOR CONTROL REG
DATA BUFF ENABLE 0
SHEET 5 OF 7
D 101 110004-009 13

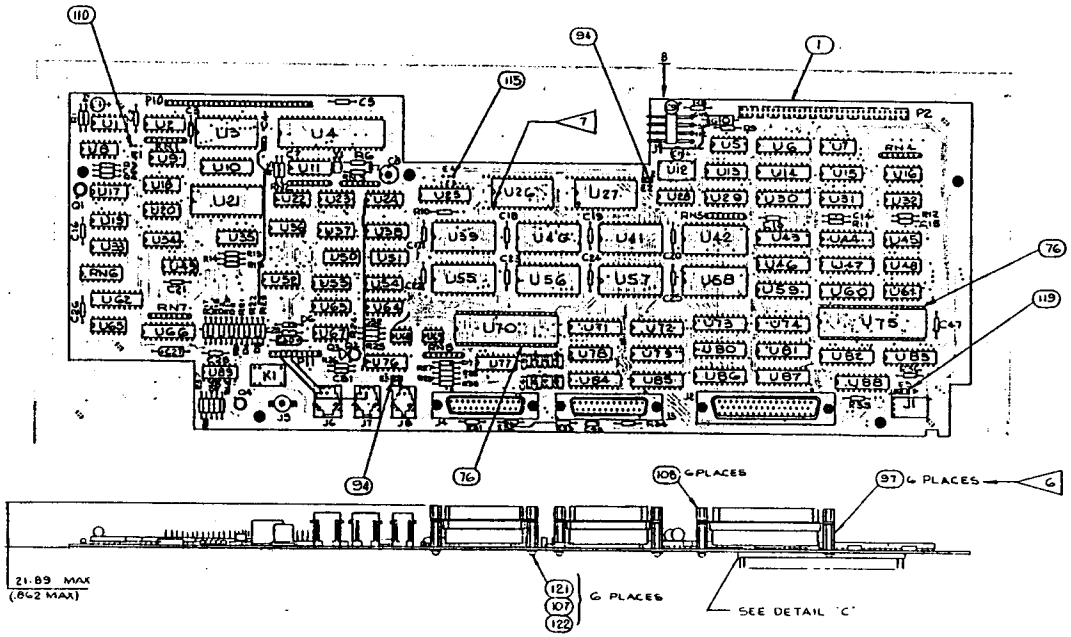

256 K x 9
DRAM ARRAY
CAS
WE
RA0 - RA7
DIN0 - DIN8
RAS0 - RAS3
DOUT 0
DOUT 1
DOUT 2
DOUT 3
DOUT 4
DOUT 5
DOUT 6
DOUT 7
DOUT 8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U32
U33
U34
U35
U36
U37
U38
U39
U40
U56
U57
U58
U59
U60
U61
U62
U63
U64
U74
U75
U76
U77
U78
U79
U80
U81
U82
RAS0
RAS1
RAS2
RAS3
SCALE: —
SHEET 6 OF 7
SIZE D
DRAWING NO. 1100004-000
REV 10
REV ECO DESCRIPTION DATE APPR
0A 335 NEW RELEASE 2/87 RK
10 1591 PRODUCTION RELEASE 2/87 RK
UPDATED DRAWING DOUT0-DOUT8 RAS3

REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
04	330	FULL FAN CIRCUITRY ADDED				
10	393	PART OF CIRCUIT DESIGNATED "OPTIONAL"				
11	455	J4-1 WAS CONNECTED TO ANODE OF D8				
12	511	ADDED FAN CIRCUITRY OPTION				

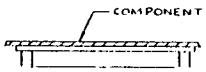


SCALE	SHEET 7 OF 7	SIZE D	CODE	DRAWING NO 110004-000	REV 14

REVISIONS							
REV	ECO	ZONE	DESCRIPTION	CHK	ENG	APPD	DATE
01	316		PRODUCTION RELEASE				
02	322		TRACKS CUTS, JUMPERS WIRES ADDED 2 CIRCUIT JUMPER DELETED AT E1				
03	323		CIRCUIT UPDATED C20 & C21 WERE TANT.				
03	ATT #1 323		JUMPER 15 & 14 ADDED				
04	357		CHANGED COMPONENT DESIGNATIONS UPDATED CIRCUITRY				
05	377		PIN OF C2-4, C12-26, C28,29 C44-48 CHANGED ALSO DELETED				
06	401		U89 ADDED WITH Q4				
07	437	BS	ITEM 121 WAS 105 ADDED ITEM 122 QTY 6				
08	457		DELETED ITEM 89, ADDED ITEM 123 CHANGED DESCRIPTION ON C56				
09	471		PWB REVISED SEE ECO FOR DETAILS.				



VIEWED IN DIRECTION OF ARROW B
N.T.S.



DETAIL 'C'
P2 IS MOUNTED FROM SOLDER SIDE OF BOARD
N.T.S

NOTES:

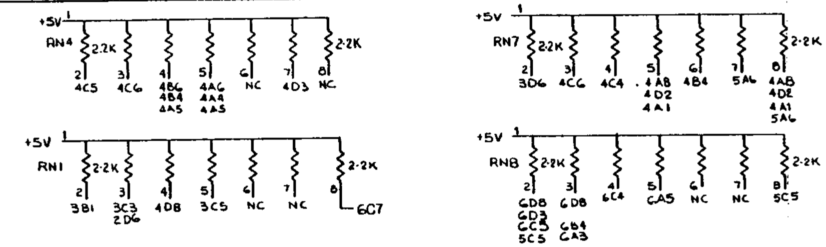
1. FOR ITEM No'S REFER TO BILL OF MATERIAL 100005-000-09 SHEETS 2, 3, AND 4.
2. REFERENCE SCHEMATIC DIAGRAM 110005-000.
3. OBSERVE POLARITY OF CAPACITORS, DIODES AND BATTERY BT1.
4. MARK ASSEMBLY REVISION AND SERIAL No.____ DURING ASSEMBLY IN WHITE EPOXY INK.
5. PWA 100005-000-09 IS TO BE USED WITH SCHEMATIC 110005-000-09 AND PWB DRAWING 200004-000-06.
6. ADD SMALL AMOUNT OF SEALANT ADHESIVE P/N 900885-000, AS REQUIRED TO ITEM 97 AT END SEATING ON PWB.
7. AT IC LOCATIONS U26 AND U27, WHEN INSERTING A 24 PIN IC, PIN 1 IS LOCATED AT PIN 3 ON PWB AS INDICATED BY DOT. WHEN USING A 28 PIN IC PIN 1 IS LOCATED AT SQUARE PAD POSITION.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: FRACTIONS ± DECIMALS .XX ± .X ± ANGLES ± MFG .XX ± .X ±	DRAWN G. LEVEILLE	Dynalogic			
	CHECKED	Dynalogic Info-Tech Corporation Ottawa Canada			
	ENGINEER	TITLE PWA DISPLAY & I/O CARD A7			
	APPROVED				
	SCALE 1/1				
	SHEET 1 OF 4	SIZE D	CODE	DRAWING NO 100005-000	REV 09

100005-000-09 SHT 1 OF 4

DIGITAL POWER AND GROUND TABLE

IC No	TYPE	POWER +5	POWER +12AV	POWER -12	GND	QTY
U7, U17, U36, U37, U53, U54, U64	74LS74	14			7	7
U9	74ALS02	14			7	1
U16, U22	74ALS04	14			7	2
U50	74LS04	14			7	1
U23, U45, U48, U51, U52, U67	74LS08	14			7	6
U5	74LS14	14			7	1
U65	74LS30	14			7	1
U24, U33	74ALS32	14			7	2
U32, U34, U61, U63	74LS32	14			7	4
U1, U8, U18-U20, U31, U49	74ALS74	14			7	7
U38	74LS139	16			8	1
U13	74LS153	16			8	1
U77	74LS155	14			7	1
U29, U35	74LS157	16			8	2
U15, U81	74LS166	16			8	2
U78	74LS174	16			8	1
U46, U47, U66, U71, U79-U81, U75, U83, U86-U88, U74	74LS244	20			10	14
U30, U59, U72, U85	74LS245	20			10	4
U60	74LS273	20			10	1
U2	74LS283	16			8	1
U14, U43, U44, U84	74LS374	20			10	4
U62	74ALS574	20			10	1
U76	75175	16			8	1
U3	2732A	24			12	1
U4	8255A-5	26			7	1
U21	8021-003	12			17	1
175	CRT 9007	21			40	1
U75	PAL12L6	20			10	1
U10	PAL16L8	20			10	1
U26, U27, U39-U47, U55-U58	HM6116-3	24			12	10
U11	N5N5B321R5				8	1
U69, U68	μA9636A		8		4	2
U70	Z80A SIO/O	9			31	1
U82	PAL14L4	20			10	1
U6	PAL10H8	20			10	1
U12	XTLO	14			7	1
U89	74S86	14			7	1

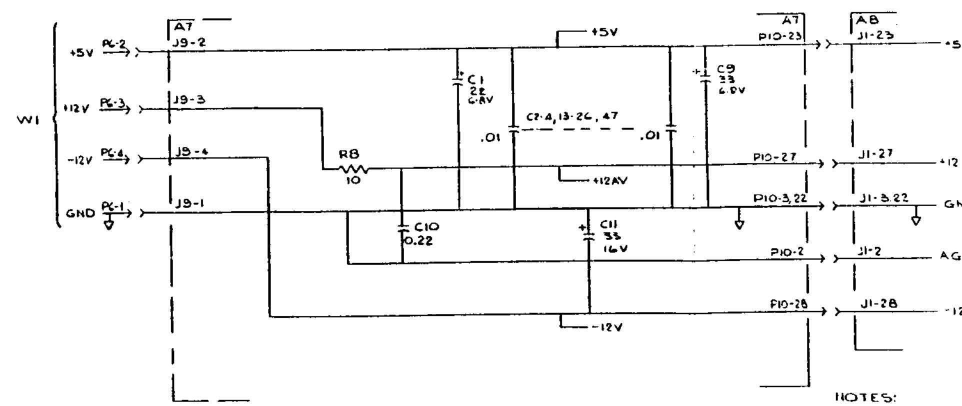


HIGHEST DESIGNATIONS USED

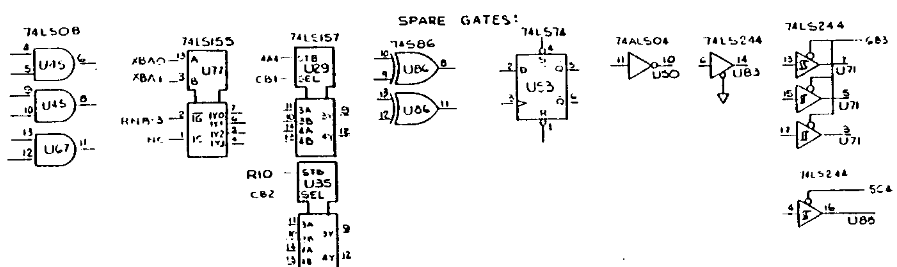
C	D		E	J	K	P	Q	R	RN	U	Y
C48	D7		E5	J9	K1	P11	Q4	R40	RN8	U89	Y1

HIGHEST DESIGNATIONS NOT USED

C31-44 C48											



SPARE GATES:



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, 1/4 W; CAPACITANCE VALUES ARE IN MICROFARADS (μF).
2. CIRCUIT COMPONENTS SHOWING THE SYMBOLS * OR ** ARE COMMON TO THE SAME IC PACKAGE.
3. SCHEMATIC 110005-000-09 IS TO BE USED WITH PWA 100005-000-09 AND PWB DRAWING 200004-000-06.

REVISIONS

REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
99		PRELIMINARY RELEASE				
98		CIRCUIT & DESIG. CHANGES	[illegible]			[illegible]
0A		CIRCUIT & DESIG. CHANGES				
00	316	PRODUCTION RELEASE	[illegible]	[illegible]	[illegible]	[illegible]
01	328	CIRCUIT UPDATE	[illegible]			
02	328	ON SHT6 ZONE D2 DEL. C5-C8	[illegible]			
03	323	USED SPARE GATE U8 SHT2 ZONE D6 & U5 SHT 6 ZONE C1	[illegible]		[illegible]	[illegible]
03	323	IN ZONE A3 SHEET 6 USED SPARE U78 PIN 14 E15	[illegible]		[illegible]	[illegible]
04	357	CONNECTIONS CHANGED/ ADDED		[illegible]	[illegible]	[illegible]
06	401	CIRCUITRY UPDATED U53 WAS 74LS08 U89 ADDED	[illegible]	[illegible]	[illegible]	[illegible]
07	437	REV 07 USE WAS 06, AND REFLECT ASSY DWG REV	[illegible]	[illegible]	[illegible]	[illegible]
08	457	CHANGED DESCRIPTION OF C6, C32 & C46	[illegible]	[illegible]		[illegible]
09	471	CIRCUIT CHANGES AS PER SHEETS 4 TO 6	[illegible]			

NEXT ASS'Y	USED ON
100005-000	HYPERION

REV	06	09	09	0A	0A	09
SHEET	7	6	5	4	3	2 1

SHEET INDEX

DRAWN: G. LEVEILLE, 19 MAY 1981
CHECKED: I.C. SULLIVAN
ENGINEER: I.C. SULLIVAN

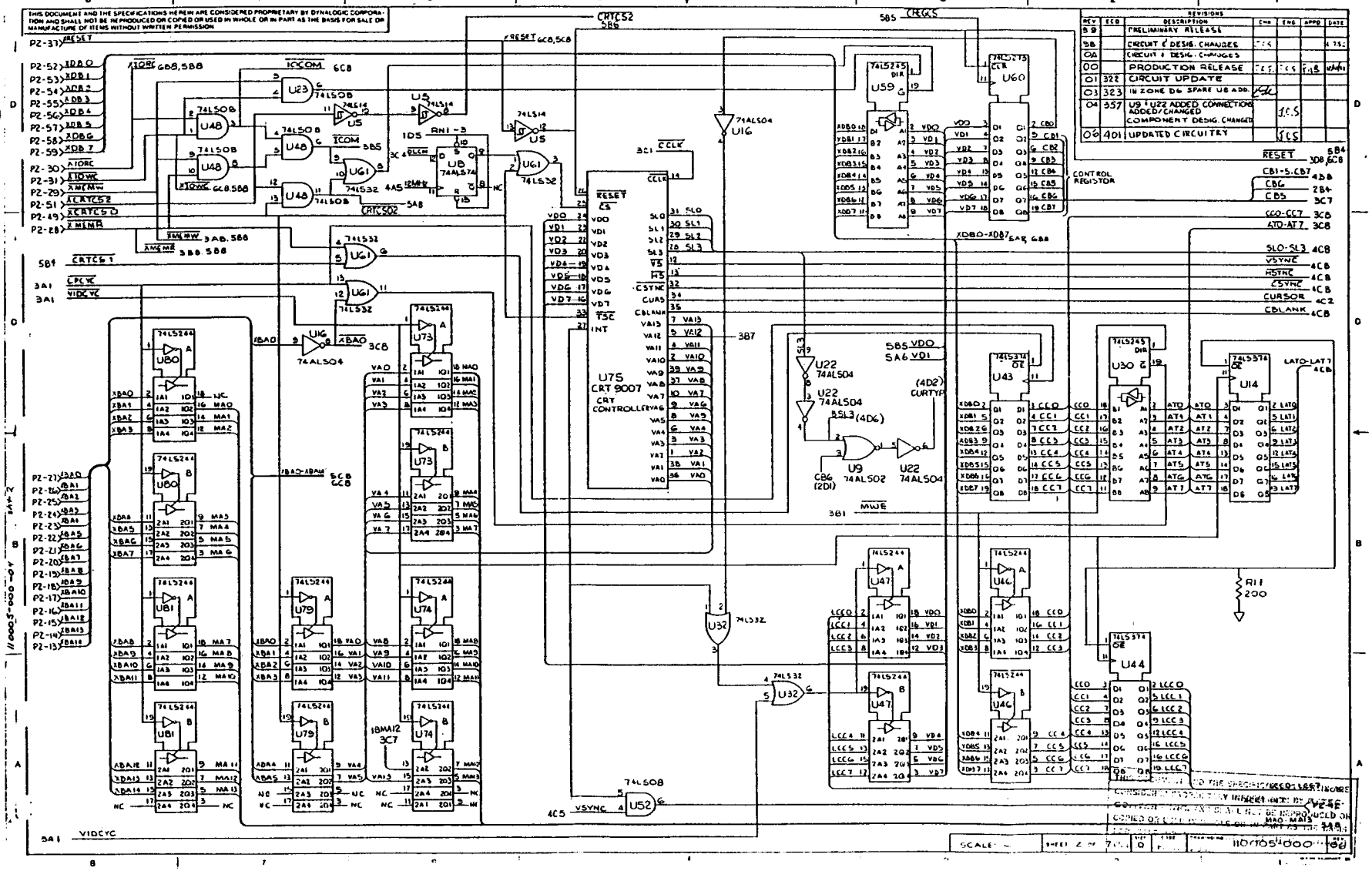
Dynalogic Corporation, Ottawa – Canada

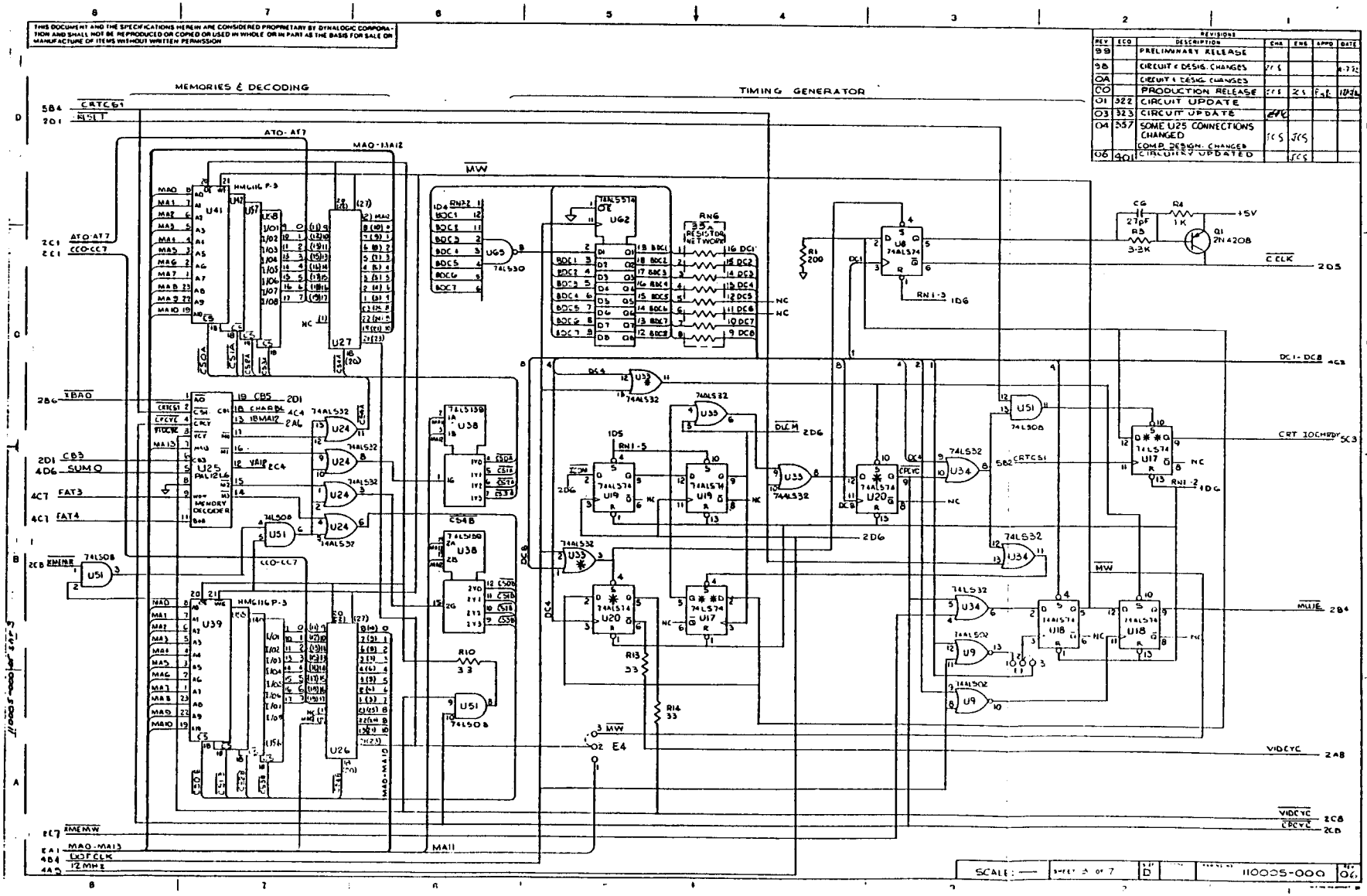
TITLE: DISPLAY AND I/O CARD - A7

SIZE D — DRAWING No. 110005-000 — REV 09

SCALE: — SHEET 1 OF 7

110005-000-09 REV 1


U75
CRT 9007
CRT CONTROLLER
U59
U60
U43
U30
U14
U44
U47
U46
U73
U74
U79
U80
U81
U1
U2
U3
U5
U6
U8
U9
U16
U22
U32
U52
74LS244
74LS245
74LS374
74LS08
74LS32
74LS04
74LS14
74LS74
74LS02
RESET
CCLK
VSYNC
HSYNC
CSYNC
CURSOR
CBLANK
CONTROL REGISTOR
XDB0-XDB7
VDO-VD7
MA0-MA13
LAT0-LAT7
SL0-SL3
CB1-5,CB7
CBG
CB5
CC0-CC7
AT0-AT7
R11
200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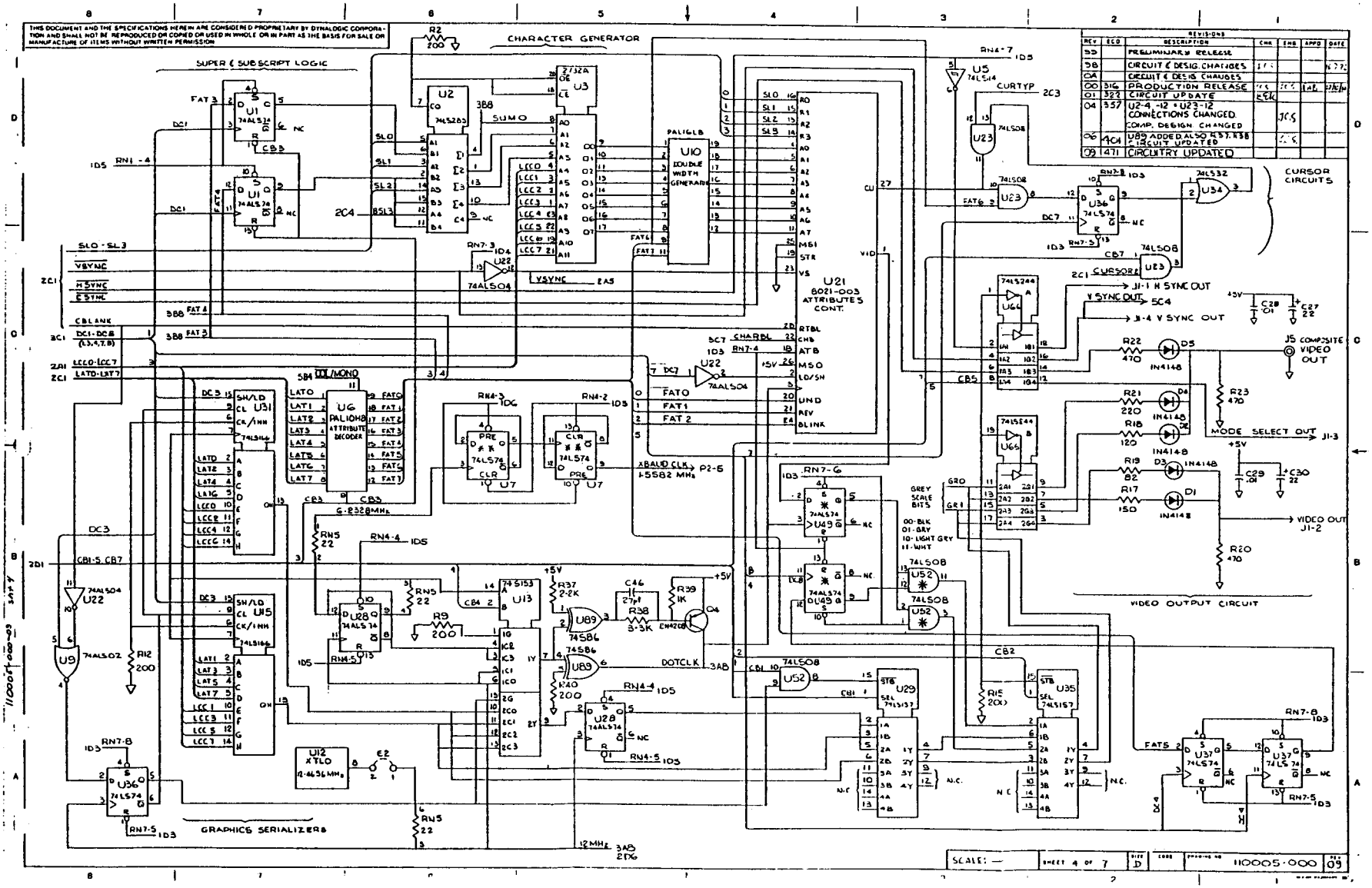
REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
99 | | PRELIMINARY RELEASE
9B | | CIRCUIT & DESIG. CHANGES
0A | | CIRCUIT & DESIG. CHANGES
CO | | PRODUCTION RELEASE
01 | 322 | CIRCUIT UPDATE
03 | 323 | CIRCUIT UPDATE
04 | 357 | SOME U25 CONNECTIONS CHANGED; COMB. DESIGN. CHANGED
06 | 401 | CIRCUITRY UPDATED
MEMORIES & DECODING
TIMING GENERATOR
CRTCS1
MW
ATO-AT7
MA0-MA13
CCO-CC7
CBS
SUMO
FAT3
FAT4
RMINH
RMEMW
MA0-MA13
LOPCLK
12 MHz
MA11
CCLK
DC1-DC8
CRT IOCHRDY
MLLIE
VIDCYC
CBCYC
HMG116 P-3
74ALS32
74ALS74
74ALS08
74ALS02
74ALS138
74ALS244
74ALS374
74ALS573
74ALS30
MEMORY DECODER
SCALE: —
SHEET 1 OF 7
SIZE D
110005-000
REV 06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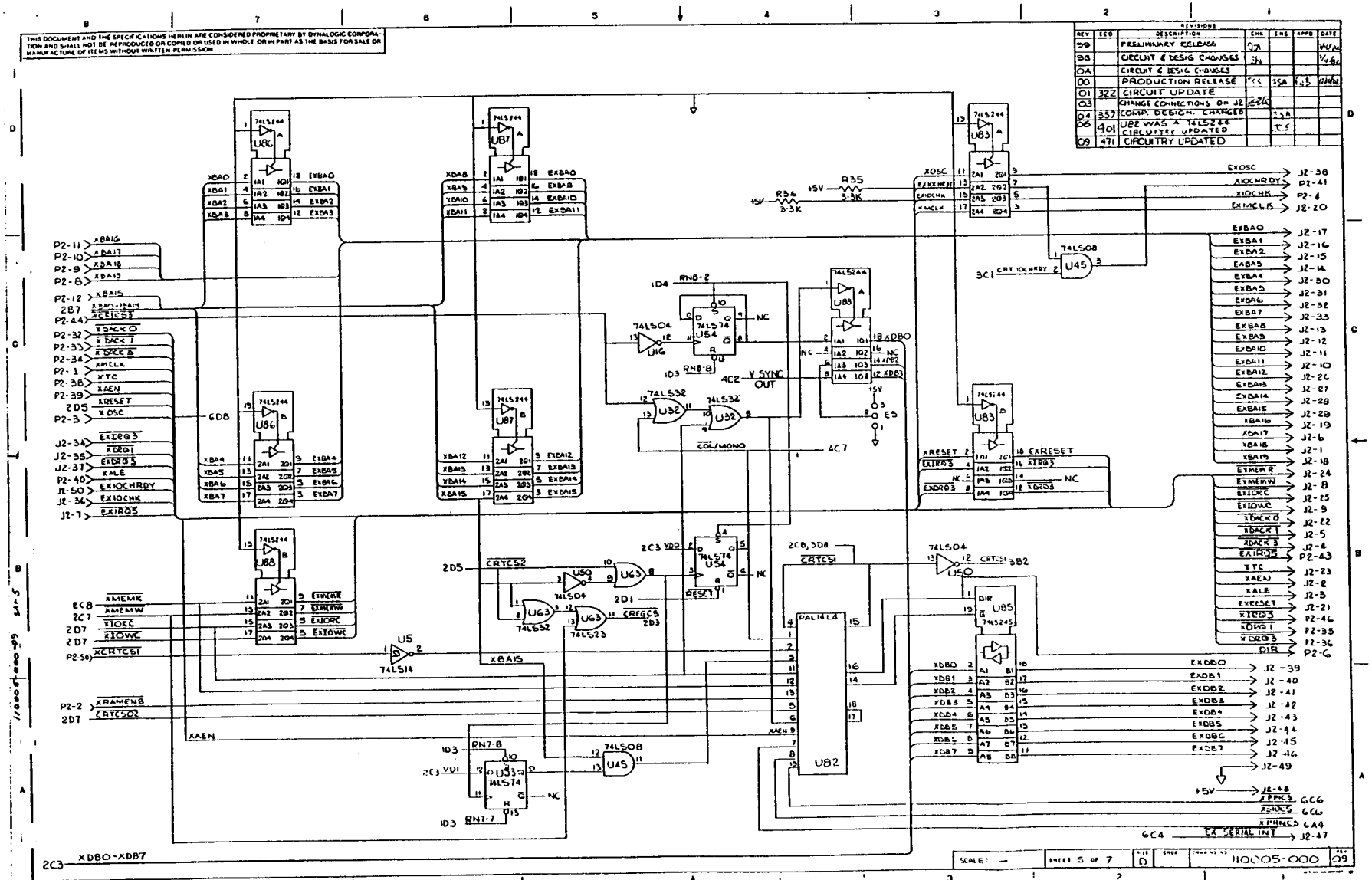
REVISIONS
REV ECO DESCRIPTION CHK ENG APPD DATE
00 PRELIMINARY RELEASE
01 CIRCUIT & DESIG. CHANGES
04 CIRCUIT & DESIG CHANGES
00 316 PRODUCTION RELEASE
01 323 CIRCUIT UPDATE
04 357 U2-4, -12 + U23-12 CONNECTIONS CHANGED. COMP. DESIGN CHANGED
06 401 U89 ADDED ALSO R37, R38 + CIRCUIT UPDATED
09 471 CIRCUITRY UPDATED
CHARACTER GENERATOR
SUPER & SUBSCRIPT LOGIC
GRAPHICS SERIALIZER
CURSOR CIRCUITS
VIDEO OUTPUT CIRCUIT
U21 8021-003 ATTRIBUTES CONT.
U6 PAL16H8 ATTRIBUTE DECODER
U10 DOUBLE WIDTH GENERATOR
U12 XTLO 12.4656 MHz
12 MHz
XBAUD CLK → P2-5 1.5582 MHz
G-2328 MHz
DOTCLK
VSYNC
CURSOR
JI-1 H SYNC OUT
V SYNC OUT → 5C4
J3-4 V SYNC OUT
J5 COMPOSITE VIDEO OUT
MODE SELECT OUT → JI-3
VIDEO OUT JI-2
GREY SCALE BITS
00-BLK 01-DRY 10-LIGHT GREY 11-WHT
SCALE: —
SHEET 4 OF 7
SIZE D
DRAWING NO 110005-000
REV 09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REVISIONS
REV | ECO | DESCRIPTION | CHK | ENG | APPD | DATE
99 | | PRELIMINARY RELEASE | DH | | | 4/4/84
98 | | CIRCUIT & DESIG CHANGES | JN | | | 1/4/84
0A | | CIRCUIT & DESIG CHANGES | | | |
00 | | PRODUCTION RELEASE | TCC | JSA | GJS | 12/14/84
01 | 322 | CIRCUIT UPDATE | | | |
03 | | CHANGE CONNECTIONS ON J2 | EDH | | |
04 | 357 | COMP. DESIGN. CHANGES | | JSA | |
05 | 401 | U82 WAS A 74LS244 CIRCUITRY UPDATED | | TCC | |
09 | 471 | CIRCUITRY UPDATED | | | |
U86
U87
U83
U88
U84
U85
U82
U80
U81
U32
U33
U45
U5
74LS244
74LS574
74LS504
74LS532
74LS08
74LS14
74LS32
74LS245
PAL14L4
RN8-2
RN8-8
RN7-8
RN7-7
R35 3.3K
R36 3.3K
+5V
XBA0
XBA1
XBA2
XBA3
XBA8
XBA9
XBA10
XBA11
EXBA0
EXBA1
EXBA2
EXBA3
EXBA8
EXBA9
EXBA10
EXBA11
XBA4
XBA5
XBA6
XBA7
XBA12
XBA13
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EXBA4
EXBA5
EXBA6
EXBA7
EXBA12
EXBA13
EXBA14
EXBA15
XDB0
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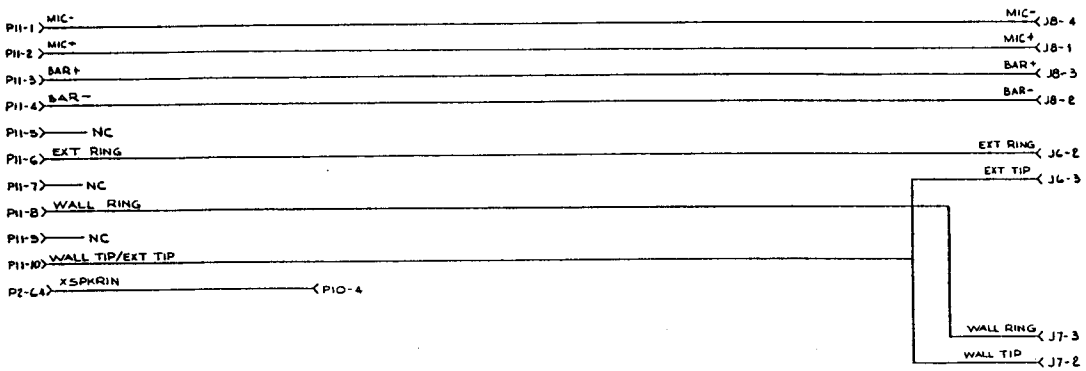
XDB2
XDB3
XDB4
XDB5
XDB6
XDB7
EXDB0
EXDB1
EXDB2
EXDB3
EXDB4
EXDB5
EXDB6
EXDB7
XOSC
EXIOCHRDY
EXIOCHK
XMCLK
EXOSC
XIOCHRDY
XIOCHK
EXMCLK
XRESET
EXRES3
EXDR03
EXRESET
XDR03
XBAIS
XAEN
XCRTCS1
XCRTCS2
XRAMENB
XMEMR
XMEMW
XIORC
XIOWC
EXMEMR
EXMEMW
EXIORC
EXIOWC
XDACK0
XDACK1
XDACK3
EXDRQ3
XDRQ1
XDRQ3
XTC
XAEN
XALE
EXRESET
XIRQ3
XDRQ1
XDRQ3
DIR
XPNNCS
EX SERIAL INT
CRTCS2
CRTCS1
RESET
VSYNC OUT
COL/MONO
XDB0-XDB7
SCALE: —
SHEET 5 OF 7
SIZE D
110005-000
REV 09

REVISIONS						
REV	ECO	DESCRIPTION	CHK	ENG	APPD	DATE
00		PRODUCTION RELEASE	[illegible]	CFM	[illegible]	[illegible]
01	322	CIRCUIT UPDATED	KFM	CFM		
04	357	COMP. DESIGN CHANGED		CFM		
06	401	UPDATED CIRCUITRY				



SCALE: —

SHEET 7 OF 7

SIZE D

110005-000

REV 06