Gesellschaft für
Parallele Systemtechnik mbH

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# M E G A F R A M E  Series

## Hardware Documentation



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MEGAFRAME / IBM Adapter

Technical Documentation

Version 1.5

September 1988

# MEGAFRAME/IBM Adapter

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## 1) Functional description:

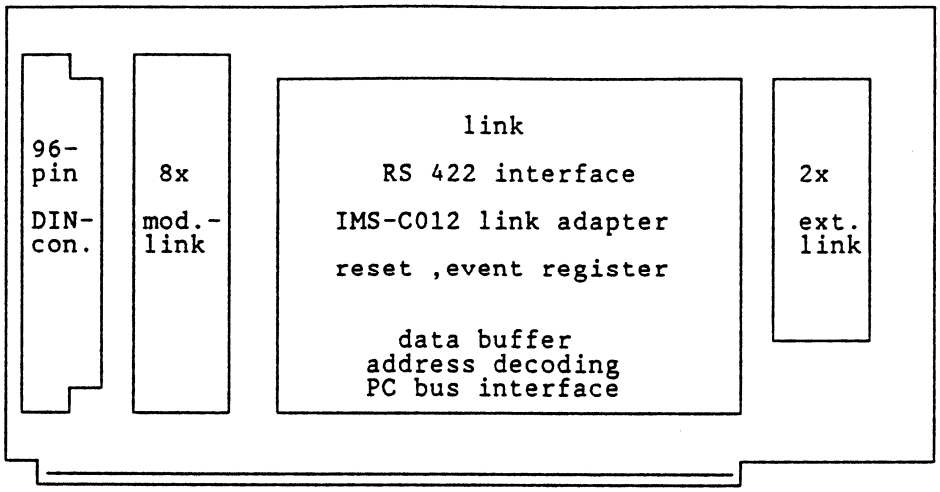



Fig. 1: Functional overview of the MEGAFRAME/IBM adapter

The MEGAFRAME/IBM adapter enables a linkage between the transputer communication channels and the IBM PC I/O bus (XT, AT and true compatibles) by use of the IMS-C012 link adapter. The IMS-C012 converts the bidirectional serial link data into parallel data streams.

The adapter module interfaces to the 8 bit wide standard IBM PC I/O bus and is compatible to the 16 bit I/O version. The integrated link interface renders the serial communication with connected transputer networks, according to the link protocol. This bidirectional serial link is, according to the MEGAFRAME standard, buffered by a RS-422 interface, wich can reliabily communicate at 20 Mbit/s using PARSYTEC link cable (the link speed may be reduced to 10 Mbit/s by use of a jumper).

Parallel to the output link a reset line is added according to MEGAFRAME standard. Before booting a connected transputer by the MEGAFRAME/IBM adapter the network is reseted to obtain a defined state at the beginning.

Link reset signals from the transputer network are detected by a on-board register and may be recognized by the PC either by reading the register information or an interrupt may be released.

The MEGAFRAME/IBM adapter is specialy designed to interface to all modules of the MEGAFRAME series, wich is physically done by a 96-way DIN connector.

As there are up to eight links on the MEGAFRAME transputer modules, these channels are led to special pinconnectors from the DIN connector on the adapter module.

On the backpanle of the adapter board there are two precision plugs (MEGAFRAME standard) to connect the twisted paired link cable (LNK-10).
These two external links (Link 0 & Link 1) can connect peripheral systems to the MEGAFRAME/IBM adapter at a distance up to 10 m by a communication speed of up to 20 Mbit/s. These concerning links are led to special pinconnectors as well.

The external Link 0 is adaptable to the special INMOS standard by use of a jumper ( the special LNK/INMOS cable offers all the functionality requested to combine MEGAFRAME tranputer modules and INMOS boards).

The array of totaly eleven links on the board led to pinconnectors, as mentioned, makes a very differentiated link configuration come possible. Beside this, several units installed in one PC may be connected between each other.

## 2) The links

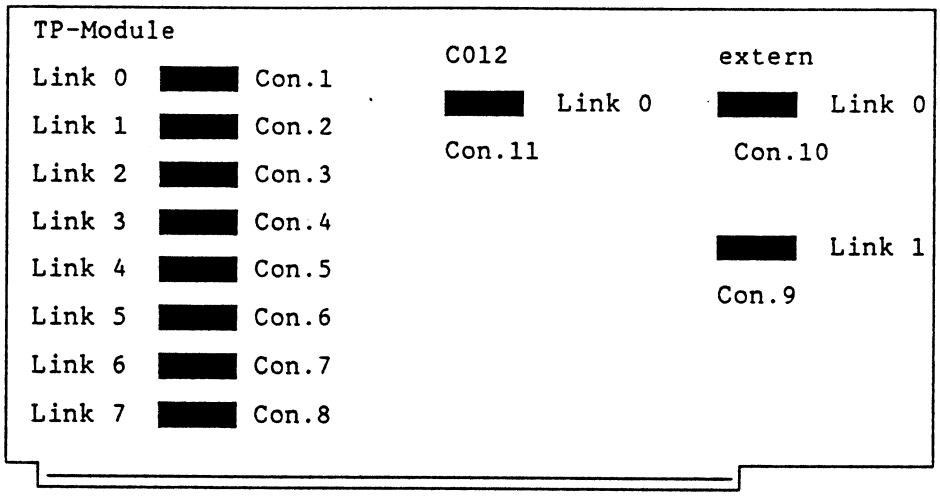



Fig. 2: Positions of the links on the module

Correspondence of the links and the 10-pin. pin connectors:

a) the link adaptor IMS-C012:

Link 0 <=> Con. 11

b) the external links:

Link 0 <=> Con. 10

Link 1 <=> Con. 9

The external link 0 can be adjusted to INMOS standard by configuring jumper J2 as shown in chapter 3.

c) the links of the attached transputer module:

| | | |
|---|---|---|
| Link 0 | <=> | Con. 1 |
| Link 1 | <=> | Con. 2 |
| Link 2 | <=> | Con. 3 |
| Link 3 | <=> | Con. 4 |
| Link 4 | <=> | Con. 5 |
| Link 5 | <=> | Con. 6 |
| Link 6 | <=> | Con. 7 |
| Link 7 | <=> | Con. 8 |

The numbering of the links corresponds directly with those of the 8-link backplane of the MEGAFRAME system unit.

## 3) Hardware addresses

The module address is completely decoded.
The base address is to be chosen by the address switches S1, S2 in the range of $0000 - $0FC0 (S1:LSB , S2:MSB).

The standard base address is $0150 (S2=1, S1=5) (compatible to the delivered software).

| | | | |
|---|---|---|---|
| IMS-C012 | baseadr. + $000 | R | input data register |
| " | baseadr. + $001 | W | output data register |
| " | baseadr. + $002 | R/W | input status register |
| " | baseadr. + $003 | R/W | output status register |
| Event Port | baseadr. + $010 | R | input reset register |
| " | baseadr. + $010 | W | output reset register |
| " | baseadr. + $012 | W | interrupt on reset register |

When using more than one unit in a PC at a time, it is necessary to separate the modules in the valid address range by using two different methods:

a) a seperate baseaddress is chosen for each module,

b) it is possible to obtain a stand-by mode for the link adaptor section on the board by placing B8 of jumper J1. In this case the module is just used as a power line to the attached transputer-module.

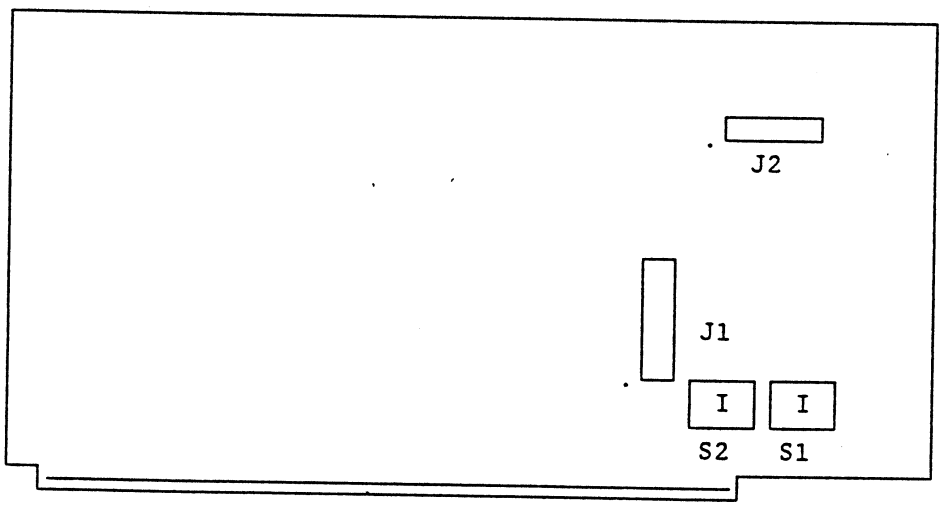
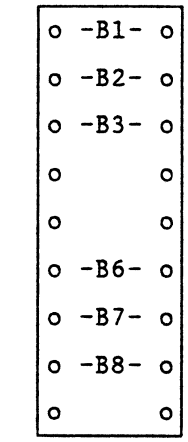



Fig. 3: Positions of jumpers and address switches

## 4) Jumper configurations

Jumper J1 system configuration:




all interrupts disable: ..... B1 placed

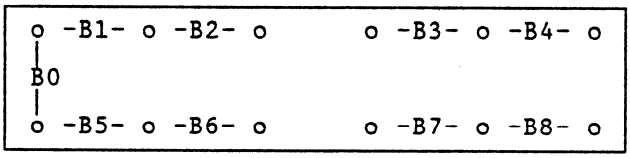
IMS-C012 linkspeed:
20 Mbit/s: ..... B2 placed
10 Mbit/s: ..... B3 placed

link-reset-out enable: ..... B6 placed

link-reset-in enable: ..... B7 placed

MEGAFRAME/IBM adaptor disable: ..... B8 placed

J2 external link 0 standard adaption:




MEGAFRAME standard: ..... B1, B4, B5, B8 placed

INMOS standard: ..... B0, B2, B3, B6, B7 placed

## 5) Description of the register functions

a) The IMS-C012 link adapter register:

The four registers are selected by the addressbits A0 and A1 (see chp.3 'Hardware addresses').
When selected, data is latched by the rising edge of /IOW. On read cycles, the current value of the selected register is placed on data bus D0-D7 by /IOR and the valid address.

The input status register (ISR);
the input present status bit D0 (IP) is set by the link adaptor after a data byte is reseived via the serial link input. The bit is reset low when the data byte is read from input data register on the parallel interface; this causes an acknowldgment to be transmitted on the serial link. Setting once the input interrupt enable status bit D1 (IIE) the input present status bit causes an interrupt (IRQ3).

The input data register (IDR);
A data byte received from the serial link can be read from the input data register on the PC`s I/O data bus. The read-cycle causes an acknowledge to be transmitted on the serial link output.

The output status register (OSR);
the output ready status bit (OR) indicates that the serial link is ready to send a byte of data. It is set high on reset, and after reseiving an acknowledgement from the serial link. It is set low when a data byte is written to the output data register on the parallel interface by the PC.
Setting the output interrupt enable status bit D1 (OIE) asserts an interrupt (IRQ3) when the link adaptor is ready to accept the next byte.

The output data register (ODR);
when the output ready status bit signals that the serial link is ready for transmission, one byte of data can be written to the link adapter`s parallel interface by the PC.

| Register | Adr.offset | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Direct. |
|---|---|---|---|---|---|---|---|---|---|---|
| ISR | $0002 | x | x | x | x | x | x | IIE | IP | R/W |
| IDR | $0000 | Data byte input from link | | | | | | | | READ |
| OSR | $0003 | x | x | x | x | x | x | OIE | OP | R/W |
| ODR | $0001 | Data byte output to link | | | | | | | | WRITE |

b) The event port register:

The input reset register (IR);
If a reset is received on the serial link input, transmitted by a connected transputer, this signal will be prepaired as data bit D0 (RIB) (active low) for use of the PC as long as the link reset will last.

The output reset register (OR);
when data bit D0 (ROB) of the output reset register is set high by the PC, a link reset will be put on the serial link output simultaneously as well as the IMS-C012 is reseted. A repeated write cycle in the same manner will cancel the link reset. Due to this function it is possible to reset the connected transputer network.

The interrupt on reset register (IOR);
when data bit D0 (IER) of this register is set high by the PC, a received link reset will cause an interrupt (IRQ2) on the PC`s interface. This function is selected by jumper J1,B1.

| Register | Adr.Offset | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Direct. |
|---|---|---|---|---|---|---|---|---|---|---|
| IR | $0010 | x | x | x | x | x | x | x | RIB | Read |
| OR | $0010 | x | x | x | x | x | x | x | ROB | Write |
| IOR | $0012 | x | x | x | x | x | x | x | IER | Write |

## 6) RESET function

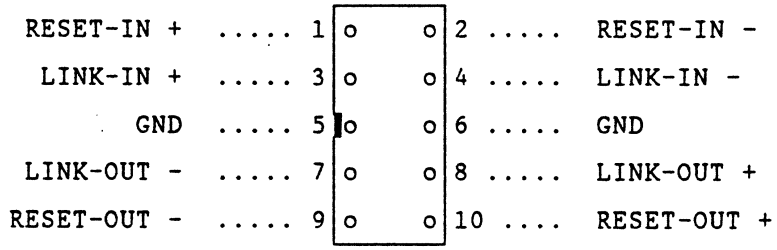
According to the MEGAFRAME standard a software controlled bidirectional reset line is added to each link. Using this, each transputer in a network is able to reset the four next neigbours.

## 7) Connector layout

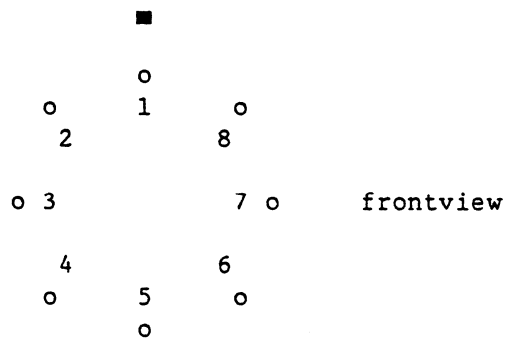
a) DIN Connector pinout ( rev.1.1 )

| | c | b | a |
|---|---|---|---|
| 1 | Reset 0 out + | Reset 1 out + | Reset 0 out - |
| 2 | Link 0 out + | Reset 1 out - | Link 0 out - |
| 3 | GND | Link 1 out + | GND |
| 4 | Link 0 in - | Link 1 out - | Link 0 in + |
| 5 | Reset 0 in - | Link 1 in - | Reset 0 in + |
| 6 | Link 1 in + | Reset 1 in - | Reset 1 in + |
| 7 | Reset 2 out + | Reset 3 out + | Reset 2 out - |
| 8 | Link 2 out + | Reset 3 out - | Link 2 out - |
| 9 | GND | Link 3 out + | GND |
| 10 | Link 2 in - | Link 3 out - | Link 2 in + |
| 11 | Reset 2 in - | Link 3 in - | Reset 2 in + |
| 12 | Link 3 in + | Reset 3 in - | Reset 3 in + |
| 13 | Reset 4 out + | Reset 5 out + | Reset 4 out - |
| 14 | Link 4 out + | Reset 5 out - | Link 4 out - |
| 15 | GND | Link 5 out + | GND |
| 16 | Link 4 in - | Link 5 out - | Link 4 in + |
| 17 | Reset 4 in - | Link 5 in - | Reset 4 in + |
| 18 | Link 5 in + | Reset 5 in - | Reset 5 in + |
| 19 | Reset 6 out + | Reset 7 out + | Reset 6 out - |
| 20 | Link 6 out + | Reset 7 out - | Link 6 out - |
| 21 | GND | Link 7 out + | GND |
| 22 | Link 6 in - | Link 7 out - | Link 6 in + |
| 23 | Reset 6 in - | Link 7 in - | Reset 6 in + |
| 24 | Link 7 in + | Reset 7 in + | |
| 25 | | Reset 7 in - | |
| 26 | | | |
| 27 | + 5 | + 5 | + 5 |
| 28 | + 5 | + 5 | + 5 |
| 29 | + 5 | + 5 | + 5 |
| 30 | GND | GND | GND |
| 31 | GND | GND | GND |
| 32 | GND | GND | GND |

b) 10-pin Connector




c) 8-pin Backplane Connector (ext. Link 0 u. 1)




| MEGAFRAME-standard | | INMOS-compatibility ( ext. Link 0 only ) | |
|---|---|---|---|
| Pin | Function | Pin | Function |
| 1 ... | RESET-OUT + | 1 ... | RESET-OUT |
| 2 ... | RESET-OUT - | 2 ... | int.Fct. |
| 3 ... | LINK-OUT + | 3 ... | LINK-IN |
| 4 ... | LINK-OUT - | 4 ... | nc |
| 5 ... | LINK-IN - | 5 ... | int.Fct. |
| 6 ... | LINK-IN + | 6 ... | LINK-OUT |
| 7 ... | RESET-IN - | 7 ... | nc |
| 8 ... | RESET-IN + | 8 ... | RESET-IN |