M E G A F R A M E Series

Hardware Documentation

VMTM

VME - Multi Transputer Module

Technical Documentation

Version 1.1

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Contents

1.

1. Block Diagram and Description

The VMTM VME - Multi Transputer Module has been conceived as a VME- slave board (implementation according to VME-spec. Rev.C: IEC 821, IEEE P1014/D 1.0. Operation modes A24/A32/D8, employed in 32-bit systems).

The board contains four independent transputer nodes based upon the IMS T800 (T414) transputer with 1 MByte DRAM local memory each. This means an on-board computing power of 40 MIPS respectively 6 MFLOPS.

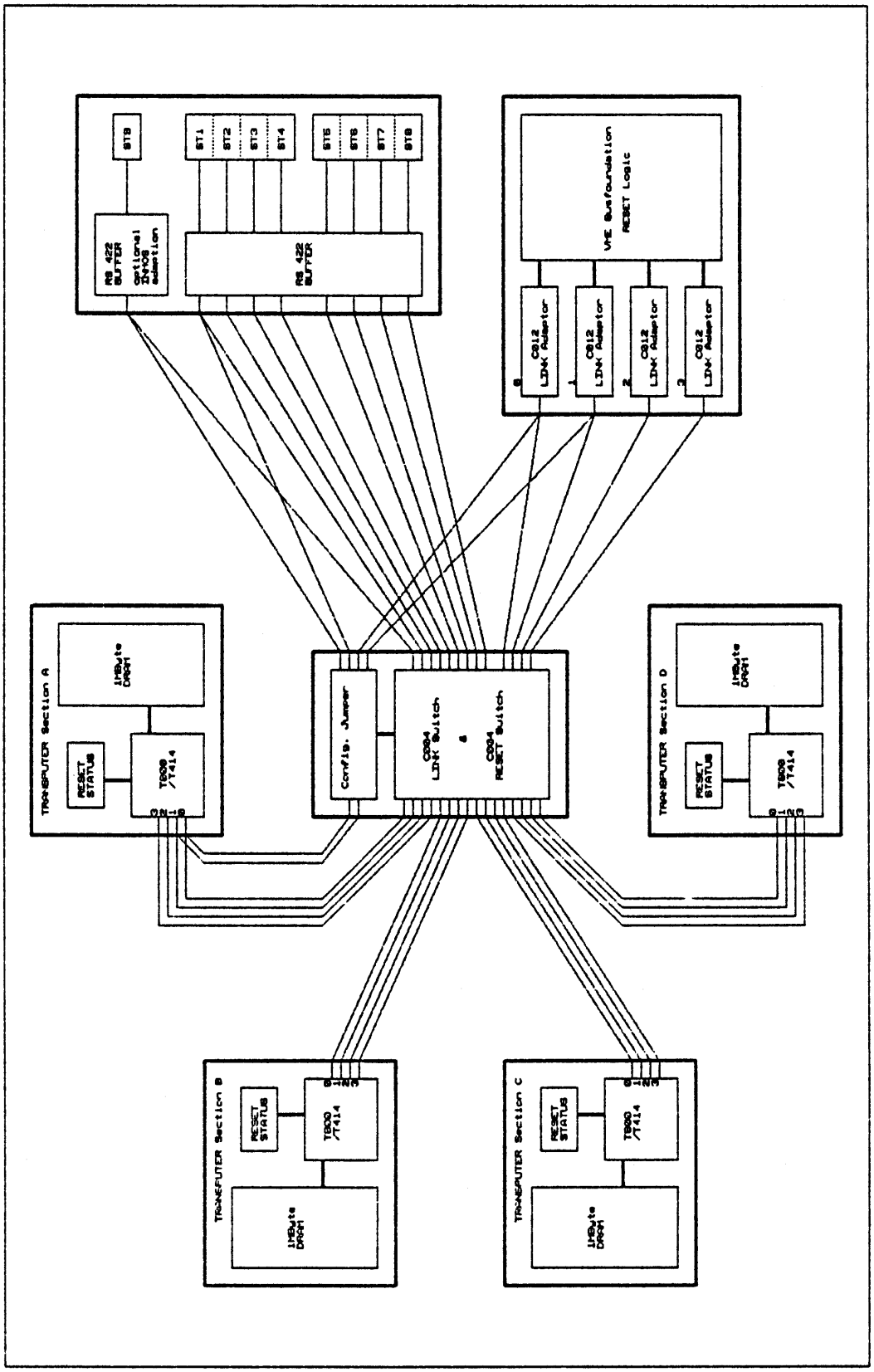
Four link- adapter IMS C012 are available to implement communication channels between the transputer nodes and the VME-bus. Due to this the VMTM Module can be used as a multiuser transputer development system, wich supports up to four users each working on its own independent transputer section . Software to support this under OS-9 and UNIX is available (MEGATOOL Transputer Development System).

Furthermore, there is the possibility to integrate the VMTM module into transputer networks via external link channels. To support this nine RS422 buffered link-channels are led to the front panel. So it is possible to implement an interconnection in case of using several VMTM modules in one VME system, or to control a remote transputer system at distances up to 10 m.

The connectivity of all 29 link channels is accomplished by electronic link switches (IMS C004). This means that all the communication channels on board are software configurable.

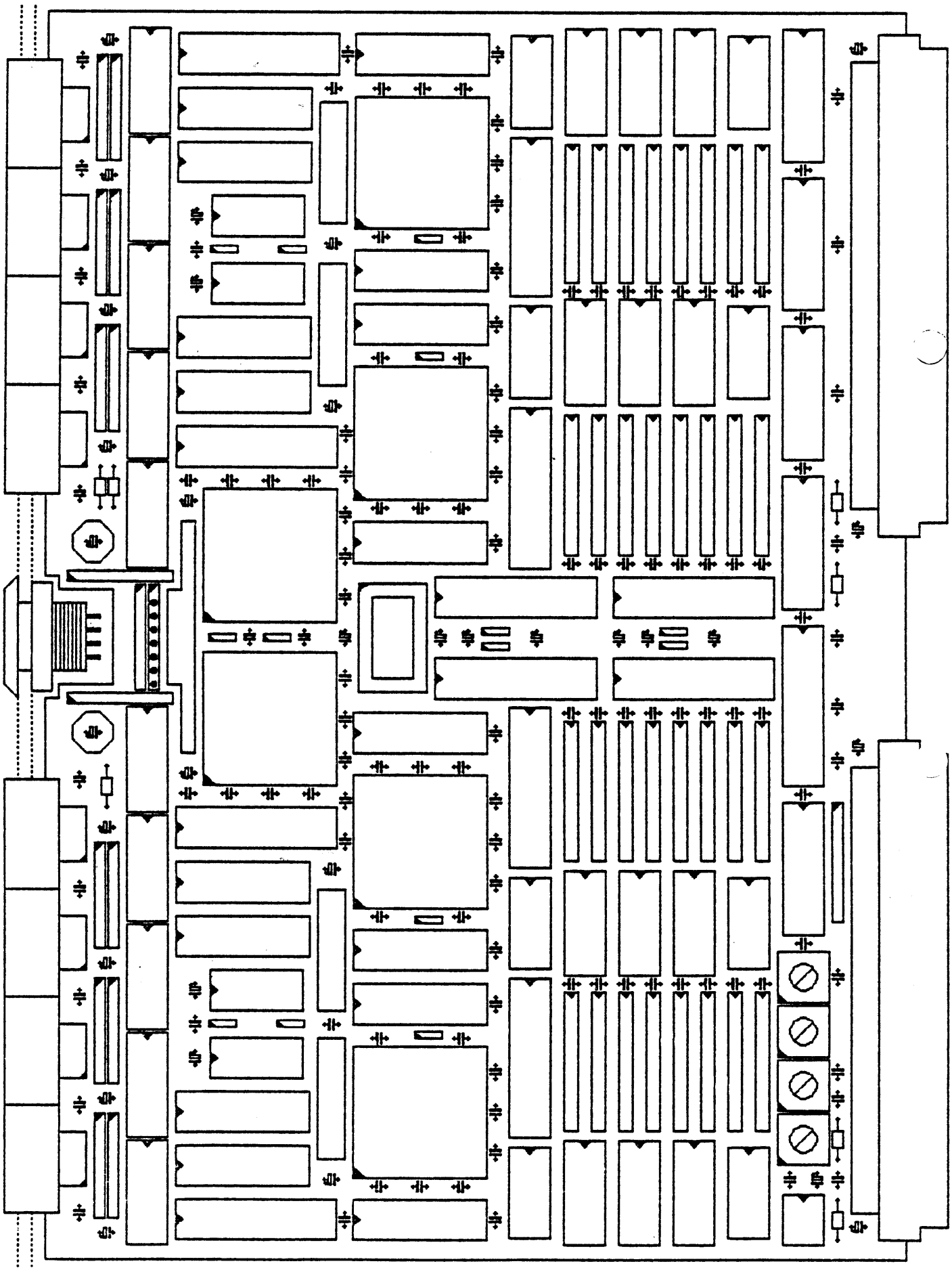
1.

Figure 1 : The VMTM - Board, Block Diagram



1.

Figure 2 : The VMTM - Board, General View



2. The Transputer Sections

2.1. Block Diagram and Description

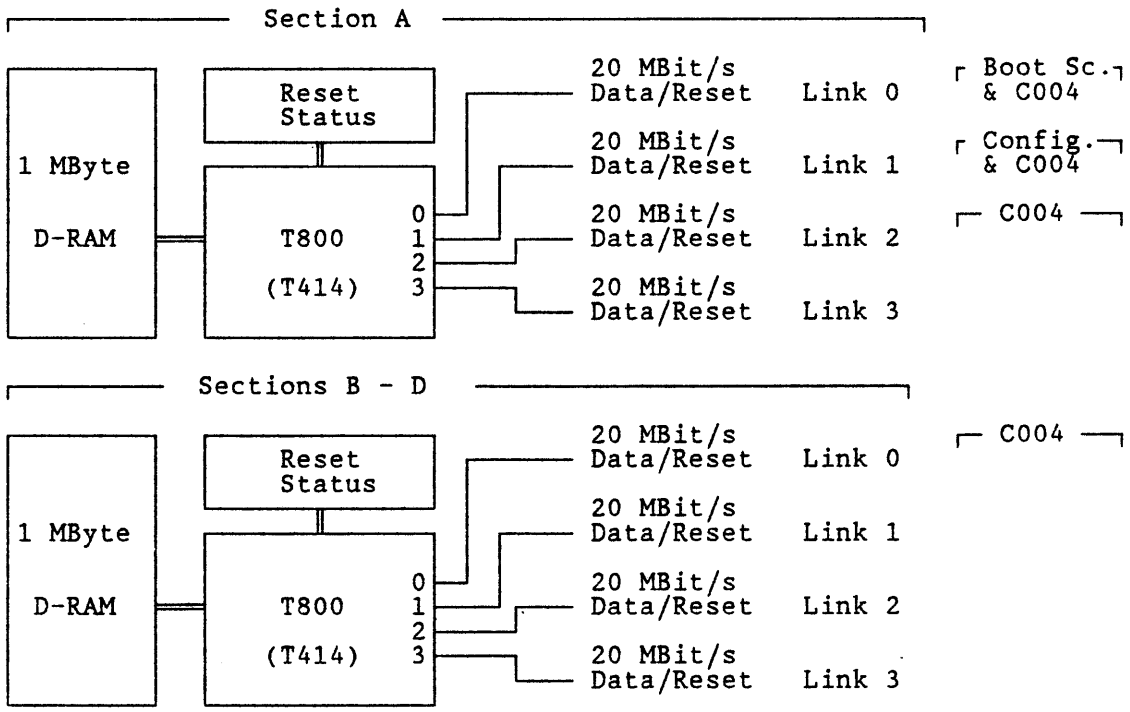


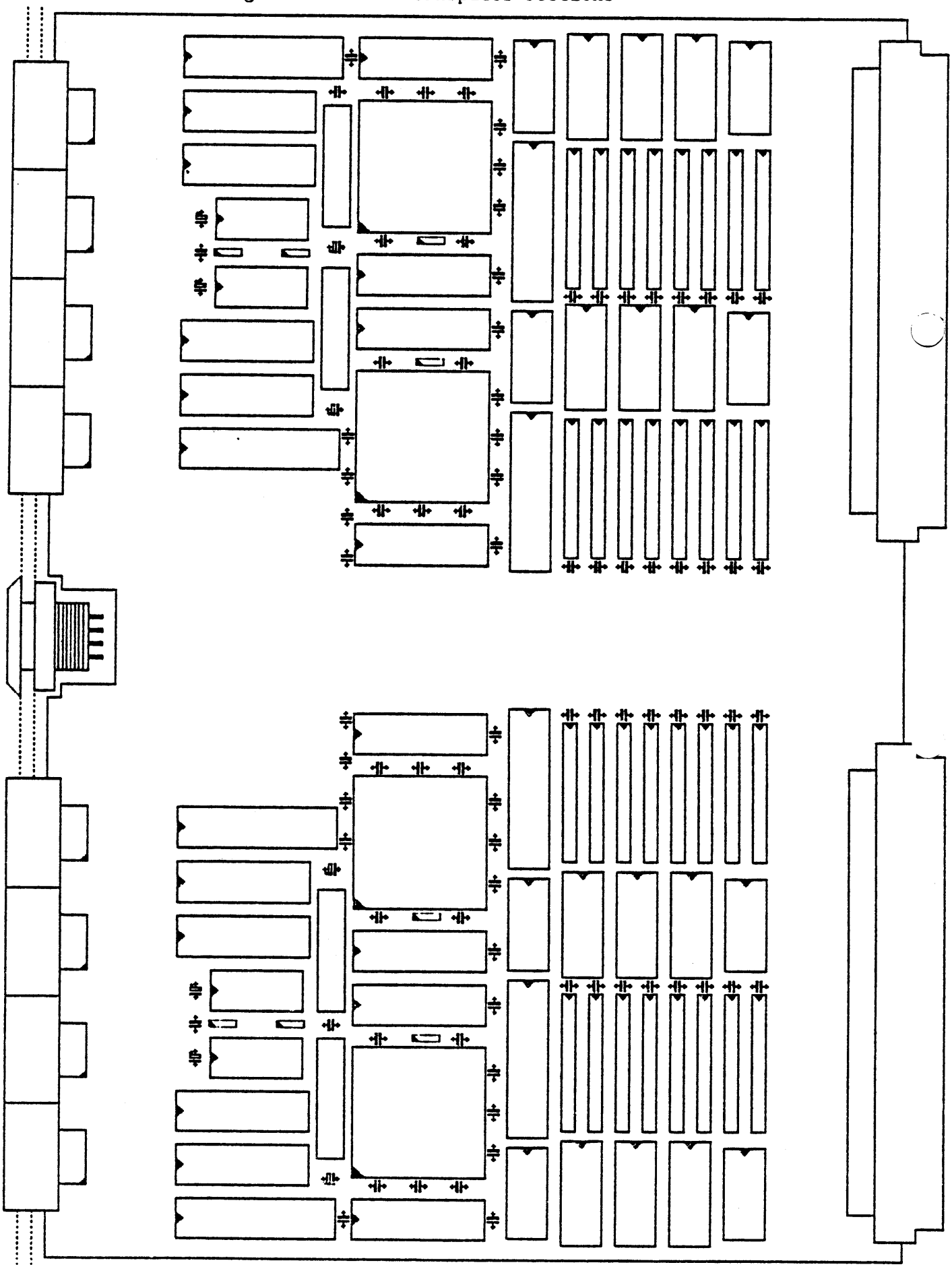
Figure 4: Block Diagram of the VMTM - Transputer Section

The VMTM is a 4-Transputer module with up to 40 MIPS processing capability. Each transputer node consists of a T800 (T414) 32 bit transputer, a 20 MHz system clock and 1 MByte dynamic RAM with a 100 ns access time.

The 4 transputer links can be adjusted to 20, 10 or 5 MBit/s working speed. Parallel to each link there exists the possibility of setting up program controlled bi-directional resets. This ensures that within a network each transputer has the possibility, by communication, of controlling the activity of its four immediate neighbours and in the event of an error to reset them and start anew. A status register holds all the error conditions and can be read-out at any time. One bit is provided for the transputer error and one for the address error. In the event of an error, either the analyse condition, an interrupt or an external error is generated according to the settings of the jumper selectors. The following functional description is applied to only one of the four transputer nodes but it is equally valid for any of them.

2.

Figure 3 : The Transputer Sections



2.2.

2.2. Hardware Addresses

Address space of the T800 (T414)

Hardware Addresses		Addresses in present OCCAM-2-Implementation PLACEment as word address
0000 00C0	Reset	#2000 0030
0000 0080	Status	#2000 0020
0000 0040		#2000 0010
800F FFFF		#0003 FFFF
...	1 MByte working memory	...
8000 0000		#0000 0000

2.3. Software - Addresses of the Links

After declaration of the channels the following address allocation is valid for the 4 links of the T800 (T414):

```
PLACE Link0.Output AT #0 :
PLACE Link1.Output AT #1 :
PLACE Link2.Output AT #2 :
PLACE Link3.Output AT #3 :
PLACE Link0.Input  AT #4 :
PLACE Link1.Input  AT #5 :
PLACE Link2.Input  AT #6 :
PLACE Link3.Input  AT #7 :
```

2.4. Bootstrap

Every processor of the VMTM is basically link-booted, that is, the processor awaits its program via a link following every reset. In such a condition, all four links have equal priority. The first information which arrives over one of these links is interpreted as a boot program and is executed accordingly.

2.5. Error and Analyse

The VMTM offers the possibility under the error conditions to react with a structured shut-down of all processes. Basically, only two types of errors can occur: program- and address errors. Programming errors, such as the division by zero, an integer overflow or an array overspill is signalled by the transputer by the setting of an error flag. An address error, i.e. accessing an address outside the boards memory, sets a bit in the status-PAL.

According to the jumper selection an error condition will initiate either an analyse condition, an interrupt, generate an external error or do nothing. Analyse mode initiates a controlled shutdown of all processes that means all active processes are systematically run down and the system can be analysed externally after resetting and re-loaded. The actual error condition can be read-out and examined.

If the transputer node is driven as host the analyse facility must be disabled!

The interrupt activates a service routine (waiting for input on OCCAM channel EVENT) which may be programmed by the user. The external error input of the T800 (T414) has, when activated, the same effect as an internal transputer error.

The addresses of the status- PALs are listed above. The bits 0 and 1 have the following meaning when set (active low):

Bit 0: Transputer Error
Bit 1: Address Error

2.6. Program controlled Reset

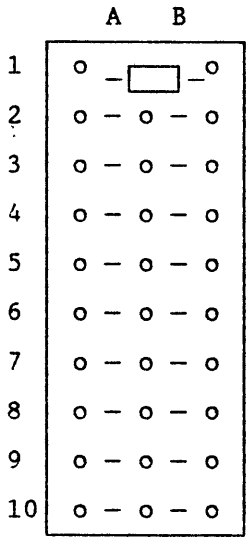
Parallel to each link a reset line is lead which puts the addressed transputer in the boot-condition. That gives the possibility to watch the activity of the next four neighbours via the links and in the event of an error to execute an aimed reset. Afterwards they can be supplied with a new program code via the links and started anew. The following program example shows the necessary command sequence for the reset:

```
PROC reset ( VAL INT channel)
  --  Reset channel 0: channel = 1
  --  Reset channel 1: channel = 2
  --  Reset channel 2: channel = 4
  --  Reset channel 3: channel = 8
  INT addr.reset :
  PLACE addr.reset AT #20000030 :  -- Address of the Reset-PAL
  TIMER clock :
  VAL INT wait IS 2 :              -- 2 times 64 microseconds
  SEQ
    addr.reset := 0                -- This sequence enables the
    addr.reset := 1                -- transmission of a
    addr.reset := 2                -- Reset.
    addr.reset := 3                --
    addr.reset := channel          -- set Reset for channel number
    clock ? time                   --
    clock ? AFTER time PLUS wait   -- 128 Micro seconds delay
    addr.reset := 0                -- erase Reset
```

2.7. Jumper Allocation

In the following jumper diagrams the position and orientation are adequate to the respective board jumpers;
(viewed from the DIN connectors's right-hand side); see also figure 5.

J101/201/301/401 external Error, Memory access, Link speed, Clock frequency T800 (T414):



External Error (Event)

enable Event : 2B jumpered
disable Event: 2A jumpered

Memory access:

30 MHz Transputer, 100 ns RAM:	4B	jumpered
30 MHz Transputer, 120 ns RAM:	3B	jumpered
20 MHz Transputer, 100 ns RAM:	3A	jumpered
20 MHz Transputer, 120 ns RAM:	4B	jumpered

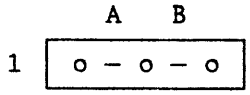
Link speed:

all Links at 20 MBit/s:	5B,6B,7B
all Links at 10 MBit/s:	5A,6A,7A
all Links at 5 MBit/s:	5A,6B,7B
Link 0 at 20 MBit/s, Link 1-3 at 10 MBit/s:	5B,6A,7B
Link 0 at 10 MBit/s, Link 1-3 at 20 MBit/s:	5B,6B,7A
Link 0 at 10 MBit/s, Link 1-3 at 5 MBit/s:	5A,6B,7A
Link 0 at 5 MBit/s, Link 1-3 at 10 MBit/s:	5A,6A,7B

Clock frequency T800-Processor:

For 20 MHz Transputer: 8A, 9A, 10A jumpered.
All other frequencies the same until final definition.

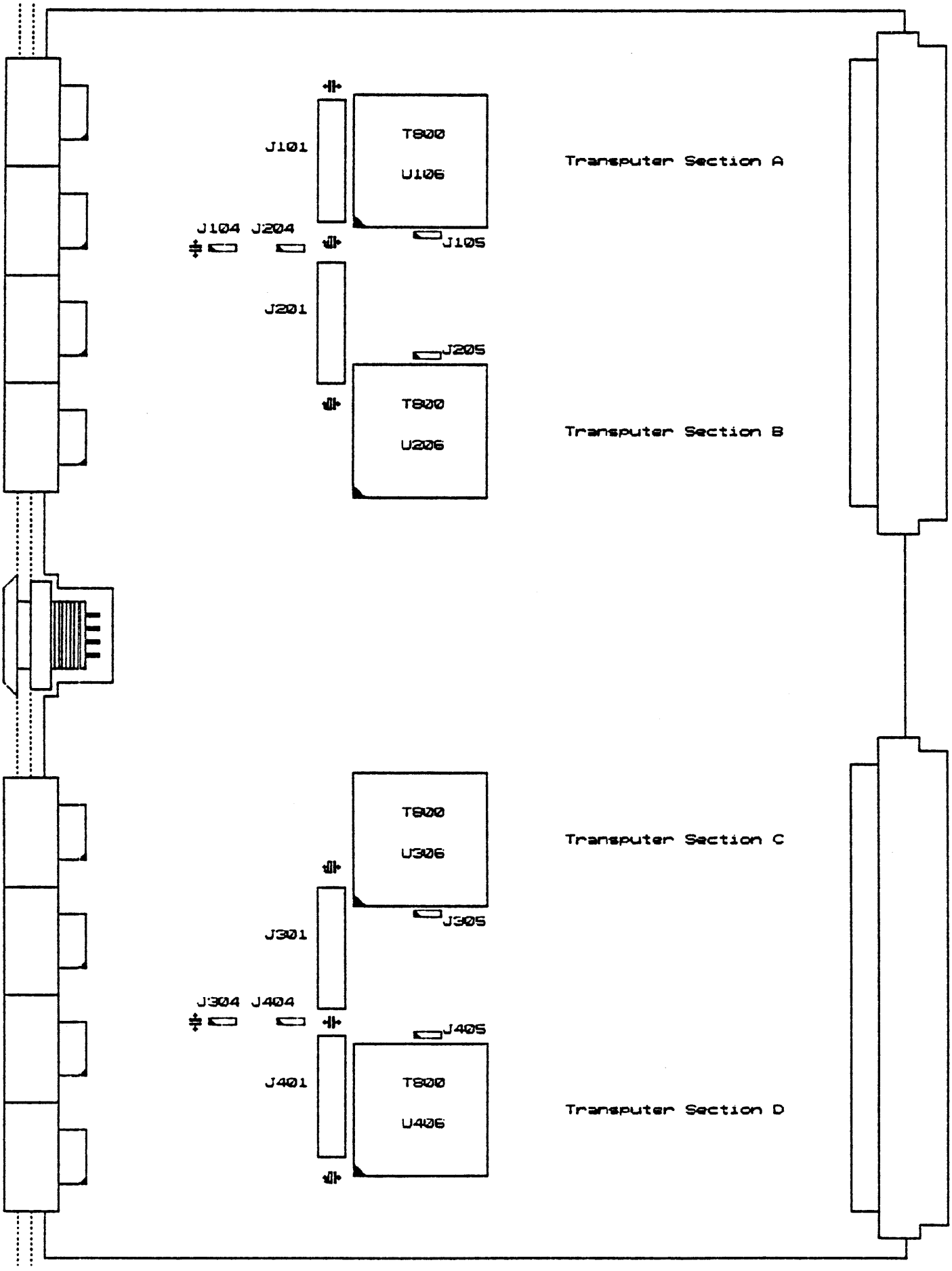
J105/205/305/405 Analyse:



Analyse enable : 1A jumpered
Analyse disable: 1B jumpered.

2.7.

Figure 5 : The jumper of the Transputer Sections



3.

3. The VME - Linkadapter Section

3.1. Block Diagram and Description

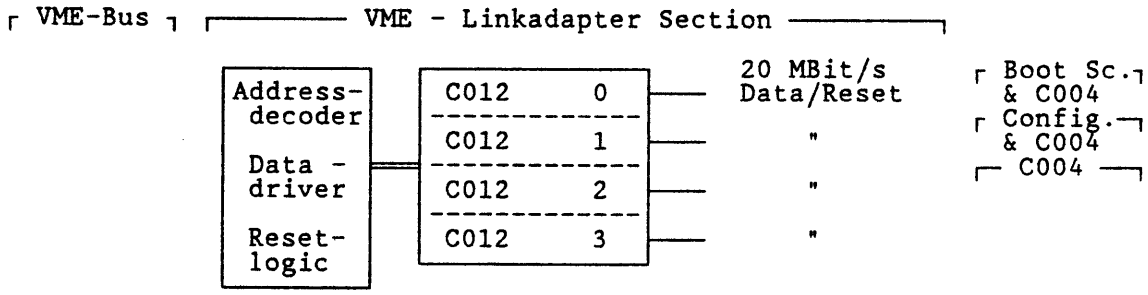


Figure 7: Block Diagram of the VMTM - VME - Linkadapter Section

The VME - link adapter section provides, from the VME-bus side, four IMS C012 link adapters for coupling transputer nodes to a VME system.

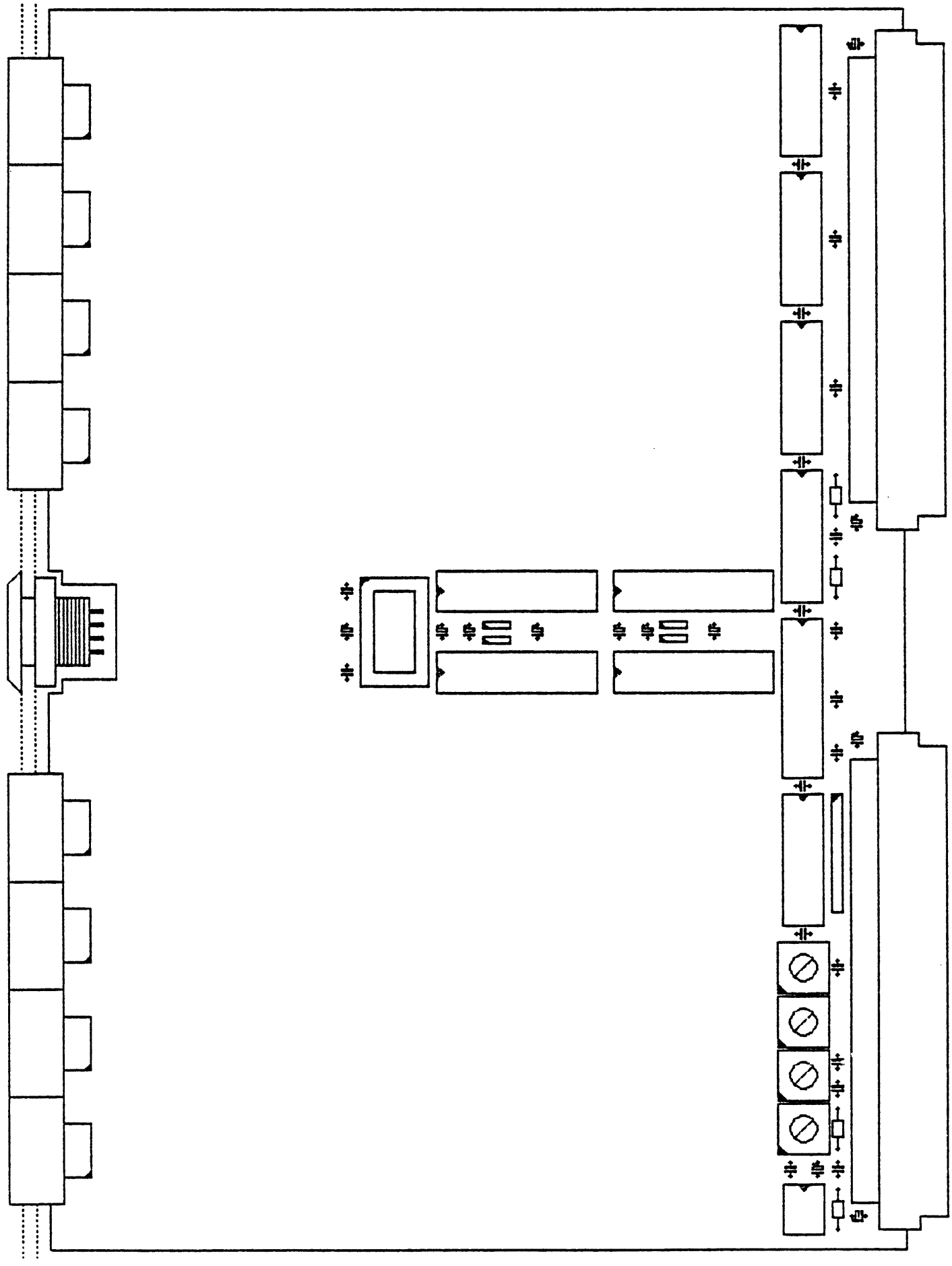
The link-adapter IMS C012 is a coupling element between the transputer-communication channels and an 8- bit wide parallel data bus.

On the one hand it has a bi-directional 8-bit I/O-data bus which is coupled to a VME-bus via an appropriate data buffer. On the other hand the integrated link interface enables a serial communication with connected transputers in accordance with the link protocol. These serial data channels can support data transfer rates of 20 Mbit/s (10 Mbit/s jumper-selectable).

The reset functions, which are integral to the link structure according to the MEGAFRAME standard, are supported by the necessary hardware. When a VME- bus has loaded a connected transputer as host transputer via the link adapter, a reset of the appropriate network (e.g. the remaining 3 transputer of the VMTM) to a defined start condition is initiated by the configurer software package.

3.

Figure 6 : The VME - Linkadapter Section



3.2.

3.2. Addressing of the VMTM

Address	Meaning
AM5 - AM0	Board Select
A31 - A8	Board Select
A7 - A4	Link Select
A3 - A0	Function Select

Board Select:

AM5 - AM4
3 = Standard Addressing
or
0 = Extended "

AM3 - AM0
D = Supervisory Data
or
9 = Non Privileged Data

A31 - A28 Addr compare with Select Switch SW4
A27 - A24 " " " SW3
A23 - A20 " " " SW2
A19 - A16 " " " SW1
A15 - A8 0 = Board Select
(Position SW1 - SW4 see figure 8)

Note: Standard addressing assumes the adjustment 'F'of the ADDR Select Switches SW4 and SW3 .

Link Select:

Selection of the Linkadapter (C012)
A7 - A4
8 = Link 3
4 = Link 2
2 = Link 1
1 = Link 0

Note: During write operations up to four links can be simultaneously addressed by adding the corresponding addresses A7 - A4 .

3.2.

Function Select:	A3 - A0	F = Stop Reset	(RD)/ WR
		D = Start Reset	(RD)/ WR
		(B)= Stop Reset	(RD)/ WR
		(9)= Start Reset	(RD)/ WR
		7 = Linkadapter Output Stat	RD / WR
		5 = Linkadapter Input Stat	RD / WR
		3 = Linkadapter Output Data	(RD)/ WR
		1 = Linkadapter Input Data	RD /(WR)

Note: The funktions F - 9 are address-triggered, that means, only Dummy-Data transfer takes place.
Addresses and Read/Write Modes in brackets should not be used.
All accesses are 8bit (D0-D7)

3.3. Programming of the Data Transfer in Polling- Mode

Note:

Users with a MEGATOOL transputer development system for OS-9 or UNIX need not care for the following section,as all accesses from host processor are already implemented in the supplied driver software. However, for specialised applictions, the user may wish to directly access the link adapters from the VME master processor.

Description of the IMS C012 Register Functions:

The four registers are selected by address bits A1 and A2 (see b) 'Addressing of the VMTM'). Should a data byte be registered in the selected register, the data information is taken over by D0 - D7 with /DS0 as well as WRITE and the valid address. In a read cycle a data-byte is put on data lines D0 - D7 with a valid address and /DS0 as well as /WRITE.

The Input-Status-Register (ISR); the Input-Present Statusbit D0 (IP) is set by the link adapter as soon as it has received a data byte via a serial link channel. Upon read-out of the Input-Data-Register the reset of the Input-Present-Statusbit and the output of an Acknowledge via the link channel follows.

The Input-Data-Register (IDR); the Input-Present- Statusbit signals that a data byte has been received via a serial link- channel: this data byte can be read-in by the VME bus; concurrently with the read-in an Acknowledge is transmitted back via a link channel.

The Output-Status-Register (OSR); the Output-ready Statusbit (OR) indicates whether the serial link-channel is ready to transmit a data-byte. Following a reset and the subsequent reception of an Acknowledge via the link-channel a status bit D0 is set. It is reset as soon as a data byte is written into the output data-register.

The Output-Data-Register (ODR); indicates by means of the status- bit D0 that the serial link-channel is primed for transmission and a data byte from the VME bus can be written into the output data- register.

3.3.

Programming examples :

Register	AddrOffset	D7	D6	D5	D4	D3	D2	D1	D0	Access
ISR	$0005	x	x	x	x	x	x	x	IP	R/W
IDR	$0001	Data-Byte				Input from Link				Read
OSR	$0007	x	x	x	x	x	x	x	OR	R/W
ODR	$0003	Data-Byte				Output to Link				Write

Link 0:

Constants :

```
INPDATA  EQU   $01
OUTDATA  EQU   $03
INPSTAT  EQU   $05
OUTSTAT  EQU   $07
STRTRES  EQU   $0D
STOPRES  EQU   $0F
```

Soft- Reset of the Link- Interface- Adapter :

```
Entry with  A1 : BBK Board Addr.
            D1 : Link No. ( 0 - 3 )
```

```
MOVE.L    $10,D2
ASL.L     D1,D2
MOVE.B    STRTRES(A1,D2),D4    ; Trigger for Start Softreset
BSR       WAIT                 ; 5 Microseconds
MOVE.B    STOPRES(A1,D2),D4    ; Trigger for Stop  Softreset
BSR       WAIT                 ; 5 Microseconds
RTS
```

3.3.

Block Send to Transputer Network :

```
    Entry with  A0 : Memory Startaddr.
                A1 : BBK Board Addr.

                D0 : Transfer Count ( 32 Bit )
                D1 : Link No. ( 0 - 3 )

    MOVE.L    $10,D2
    ASL.L     D1,D2

    LEA       OUTDATA(A1,D2),A2
    LEA       OUTSTAT(A1,D2),A3

    MOVE.L    $10,D2
    ASL.L     D1,D2
    CLR       D3                    ; Bitpointer for Output Ready
    L0:
    BTST      D3,(A3)               ; Output ready ?
    BEQ       L0
    MOVE.B    (A0)+,(A2)            ; Byte to Link Adapter
    SUBQ      #1,D0                 ; Block End ?
    BGT       L0
    L1:
    BTST      D3,(A3)               ; await last Acknowledge
    BEQ       L1
    RTS
```

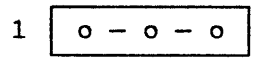
3.3.

Block Receive from Transputer Network :

```
    Entry with  A0 : Memory Startaddr.
                A1 : BBK Board Addr.

                D0 : Transfer Count ( 32 Bit )
                D1 : Link No. ( 0 - 3 )

    MOVE.L    $10,D2
    ASL.L     D1,D2

    LEA       INPDATA(A1,D2),A2
    LEA       INPSTAT(A1,D2),A3

    CLR       D3                    ; Bitpointer for Data Present
    L0:
    BTST      D3,(A3)               ; Data present ?
    BEQ       L0
    MOVE.B    (A2),(A0)+            ; Byte from Link Adapter
    SUBQ      #1,D0                 ; Block End ?
    BGT       L0
    RTS
```

3.4. Jumper Allocation and Address switches

J1,J2,J3 and J4 Link speed of the Linkadapter (C012):



10 MBit/s : 1B jumpered

20 MBit/s : 1A jumpered

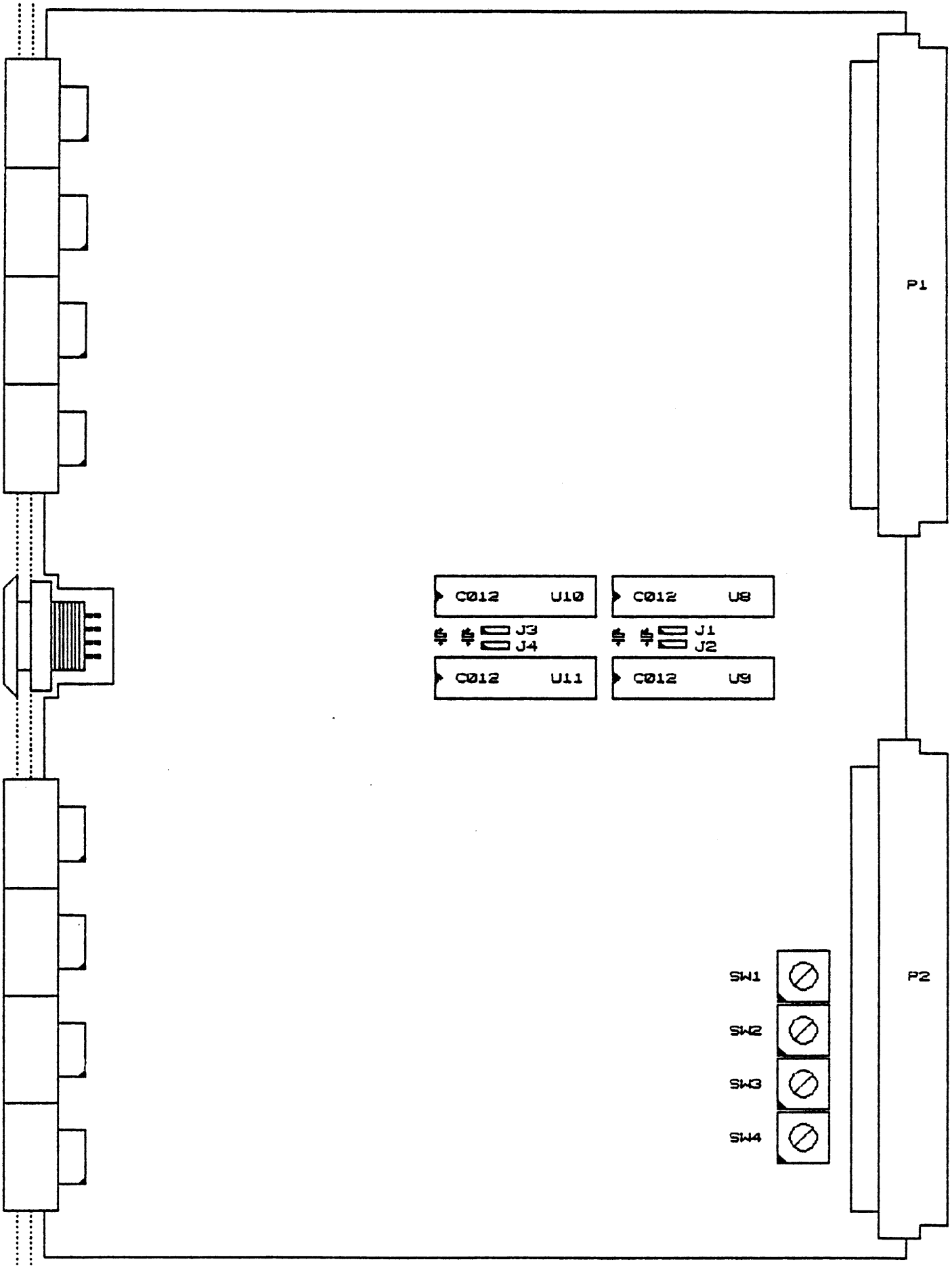
(Position J1 - J4 see fig. 8)

Correspondence Linkadapter-Channel <-> Jumper:

0	-	1
1	-	2
2	-	3
3	-	4

3.4.

Fig. 8: The Jumper and Address switches of the VME-Linkadapter Section



3.5.

3.5. PIN-out of the 96-way DIN Connectors

DIN-Connector P1:

	c	b	a
1			D0
2			D1
3			D2
4			D3
5			D4
6			D5
7			D6
8			D7
9	GND		GND
10			
11	GND		
12	/SYSRESET		/DS1
13	/LWORD		/DS0
14	AM5		/WRITE
15	A23		GND
16	A22	AM0	/DTACK
17	A21	AM1	GND
18	A20	AM2	/AS
19	A19	AM3	GND
20	A18	GND	/IACK
21	A17		
22	A16		
23	A15	GND	AM4
24	A14		A7
25	A13		A6
26	A12		A5
27	A11		A4
28	A10		A3
29	A9		A2
30	A8		A1
31			
32	VCC	VCC	VCC

3.5.

DIN-Connector P2:

	c	b	a
1	.....	VCC	
2	.....	GND	
3			
4	.....	A24	
5	.....	A25	
6	.....	A26	
7	.....	A27	
8	.....	A28	
9	.....	A29	
10	.....	A30	
11	.....	A31	
12	.....	GND	
13	.....	VCC	
14			
15			
16			
17			
18			
19			
20			
21			
22	.....	GND	
23			
24			
25			
26			
27			
28			
29			
30			
31	.....	GND	
32	.....	VCC	

4.

4. The Link switch Section

4.1. Functional Description

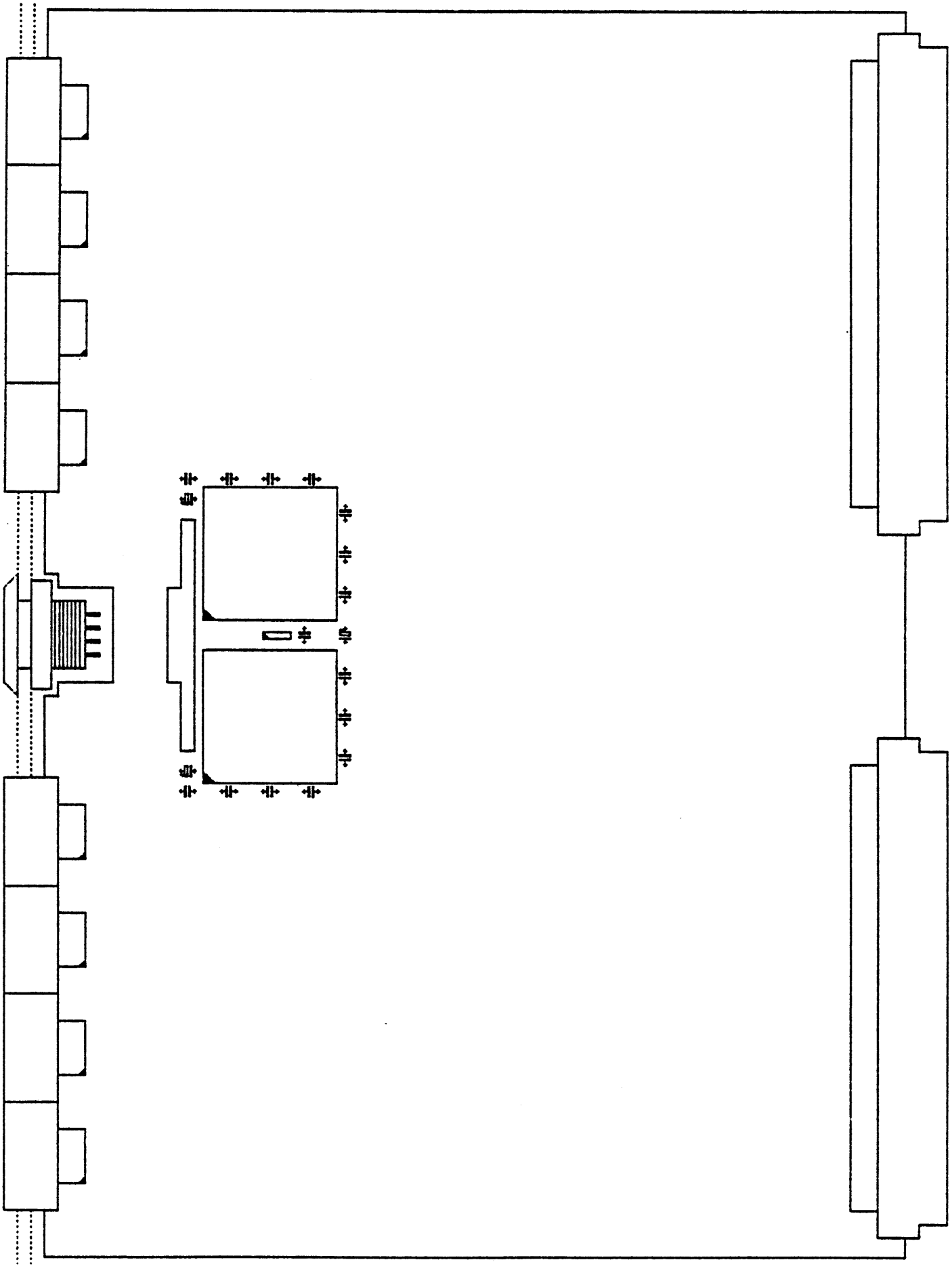
Through the employment of electronic link switches 'IMS C004' the user is able to switch as desired to the various on-board functions. The configuration is the result of a suitable initialisation of the link switches via their configuration link.

As a reset is implemented in parallel to every link function in accordance with the Megaframe specifications, this reset function is automatically carried out by a second switch. In this manner both switches are initialised in parallel.

The link switch 'IMS C004' can handle data rates of 0 to 20 MBit/s (10 MBit/s; see J5). The configuration link works with 10 or 20 MBit/s (selectable by jumper J5).

4.

Figure 9 : Link/Reset Switches



4.2. Configuration

The link switch IMS C004 is internally constructed as a 32 x 32 ways to 1 multiplexer. Each of these multiplexers is controlled by a 6 bit register. An input is selected by 5 of the bits as a data source for a corresponding output; the 6th bit will enable or disable the connection. These registers can be written into, and read from via the C004's configuration link.

The inputs and outputs are numbered from 0 to 31. The configuration code consists of one, two or three bytes. The configuration information which is sent to the C004 configuration link contains then the following tabulated information:

Information (Bytes)	Function
[0][input][output]	Connects 'input' to 'output
[1][link1][link2]	'link1'is connected to 'link2'.This connects the input from 'link1' to the output of 'link2' and vice versa.
[2][output]	Determines which input is connected to the 'output'. The highest value bit of the byte indicates whether the connection is made (1) or open (0).
[3]	This byte must be sent at the end of every configuration sequence. The appropriate connections are made and the data transmission can be commenced over this link.
[4]	Resets the switch. All connections are disabled and the outputs returned to ground.
[5][output]	The 'output' is opened.
[6][link1][link2]	The connection between the output 'link1' and the input 'link2' is opened. Correspondingly, the output 'link2'is opened from the input 'link1'.

4.2.

The following table contains the arrangement of the C004 link- channel numbers and the corresponding link functions on the VMTM-board:

Link-Channel No.	On-Board Link-Function	
[0]	Transputer Section 'A'	Link 0
[1]	"	Link 1
[2]	"	Link 2
[3]	"	Link 3
[4]	Transputer Section 'B'	Link 0
[5]	"	Link 1
[6]	"	Link 2
[7]	"	Link 3
[8]	Transputer Section 'C'	Link 0
[9]	"	Link 1
[10]	"	Link 2
[11]	"	Link 3
[12]	Transputer Section 'D'	Link 0
[13]	"	Link 1
[14]	"	Link 2
[15]	"	Link 3

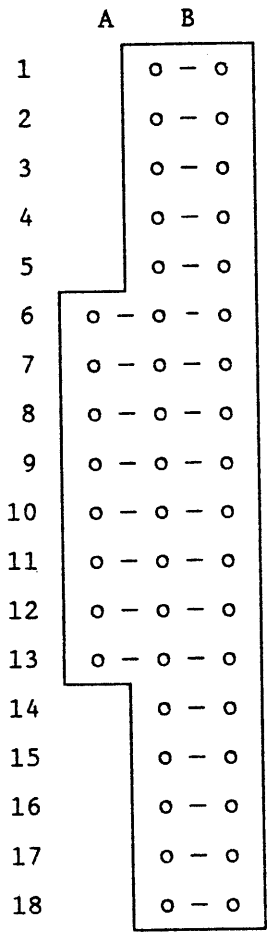
4.2.

Link-Channel-No.	On-Board Link-Function
[16]	external Link St.9
[17]	nc
[18]	nc
[19]	nc
[20]	Link-Adapter Section Link 0
[21]	" Link 1
[22]	" Link 2
[23]	" Link 3
[24]	external Link St.5
[25]	" St.6
[26]	" St.7
[27]	" St.8
[28]	" St.2
[29]	" St.1
[30]	" St.3
[31]	" St.4

4.3. The Configuration-Jumper

Jumper J7 determines wich source will load the section 'A' transputer via its link 0.
Jumper J7 selects the configuration source as well.
The following possibilities are available:

J7 Configuration



a) The booting of the transputer is done by the VME-Bus via the C012 Link-Adapter link 0, and ..

i. the transputer configures the C004 via its link 1:

1B, 3B, 10B, 11B, 12B, 13B, 14B, 15B, 16B,

6A, 9A jumpered;

ii. the configuration of the C004 is enabled via the VME-Bus by means of the C012 link-adapter link 1:

3B, 4B, 7B, 9B, 10B, 11B, 12B, 13B, 14B,

15B, 16B, 17B jumpered;

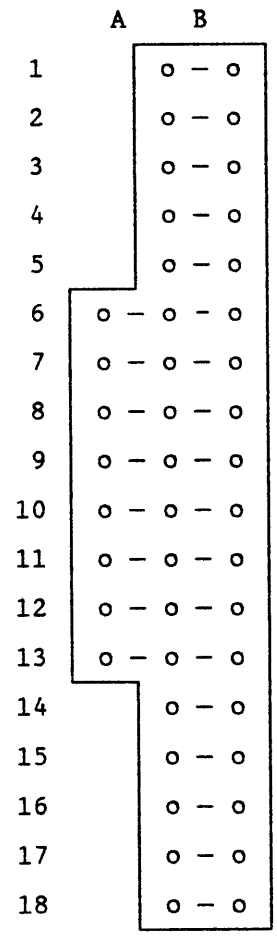
iii. a source external to the VMTM- Board configures the C004 by use of the external link-plug St.1:

1B, 3B, 4B, 6B, 8B, 10B, 11B, 12B, 13B,

16B, 17B jumpered.

—>

4.3.



b) The transputer is loaded via the external link-plug St.9 (8-way round socket), and ..

i. the transputer configures the C004 via its link 1:

6A, 9A, 10A, 11A, 12A, 13A,

1B, 2B, 14B, 15B jumpered;

ii. the configuration of the C004 is enabled via the VME-Bus by means of the C012 link-adapter link 1:

10A, 11A, 12A, 13A,

2B, 4B, 7B, 9B, 14B, 15B, 17B jumpered;

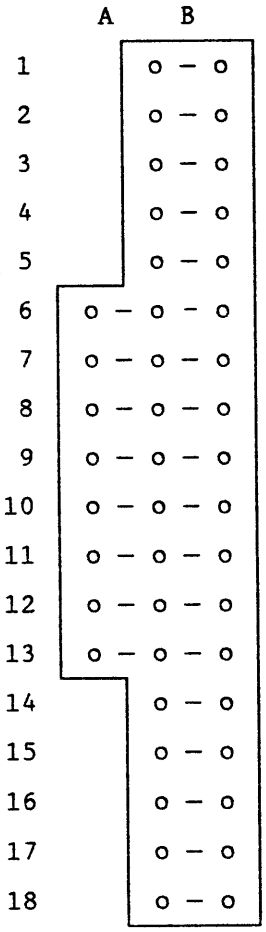
iii. a source external to the VMTM- Board configures the C004 by use of the external link- plug St.1:

10A, 11A, 12A, 13A,

1B, 2B, 4B, 6B, 8B, 17B jumpered.

—>

4.3.



c) The transputer of the section 'A' is exclusively accessed via the link switch, and ..

i. the configuration of the C004 is enabled via the VME-Bus by means of the C012 link-adapter link 1:

2B, 3B, 4B, 5B, 7B, 9B, 14B, 15B,

16B, 17B, 18B jumpered;

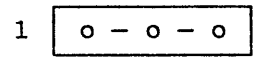
ii. a source external to the VMTM- Board configures the C004 by use of the external link- plug St.1:

1B, 2B, 3B, 4B, 5B, 6B, 8B,

16B, 17B, 18B jumpered.

4.3.

J5 Configuration-link transmission speed:

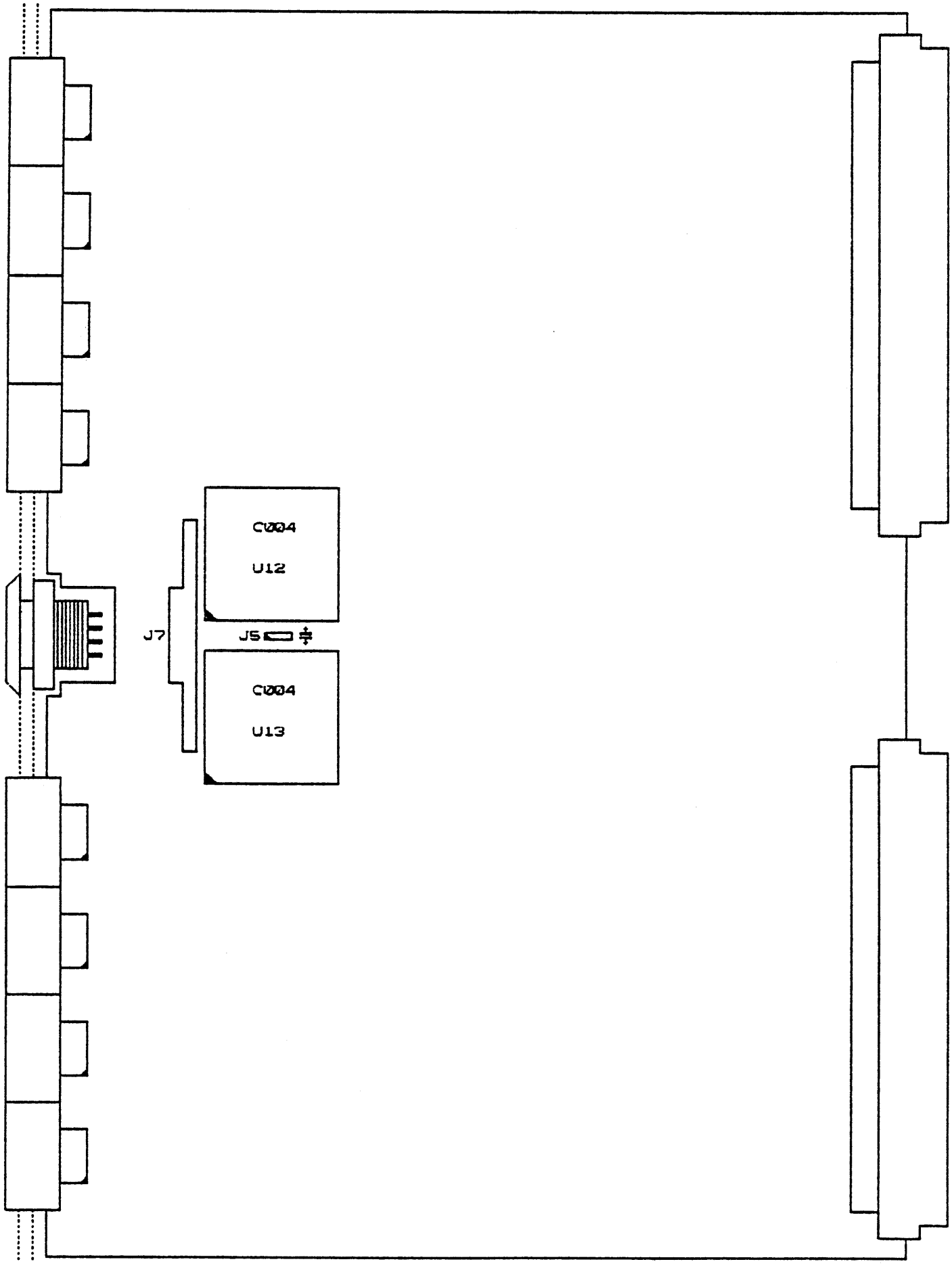


10 MBit/s : 1B jumpered

20 MBit/s : 1A jumpered

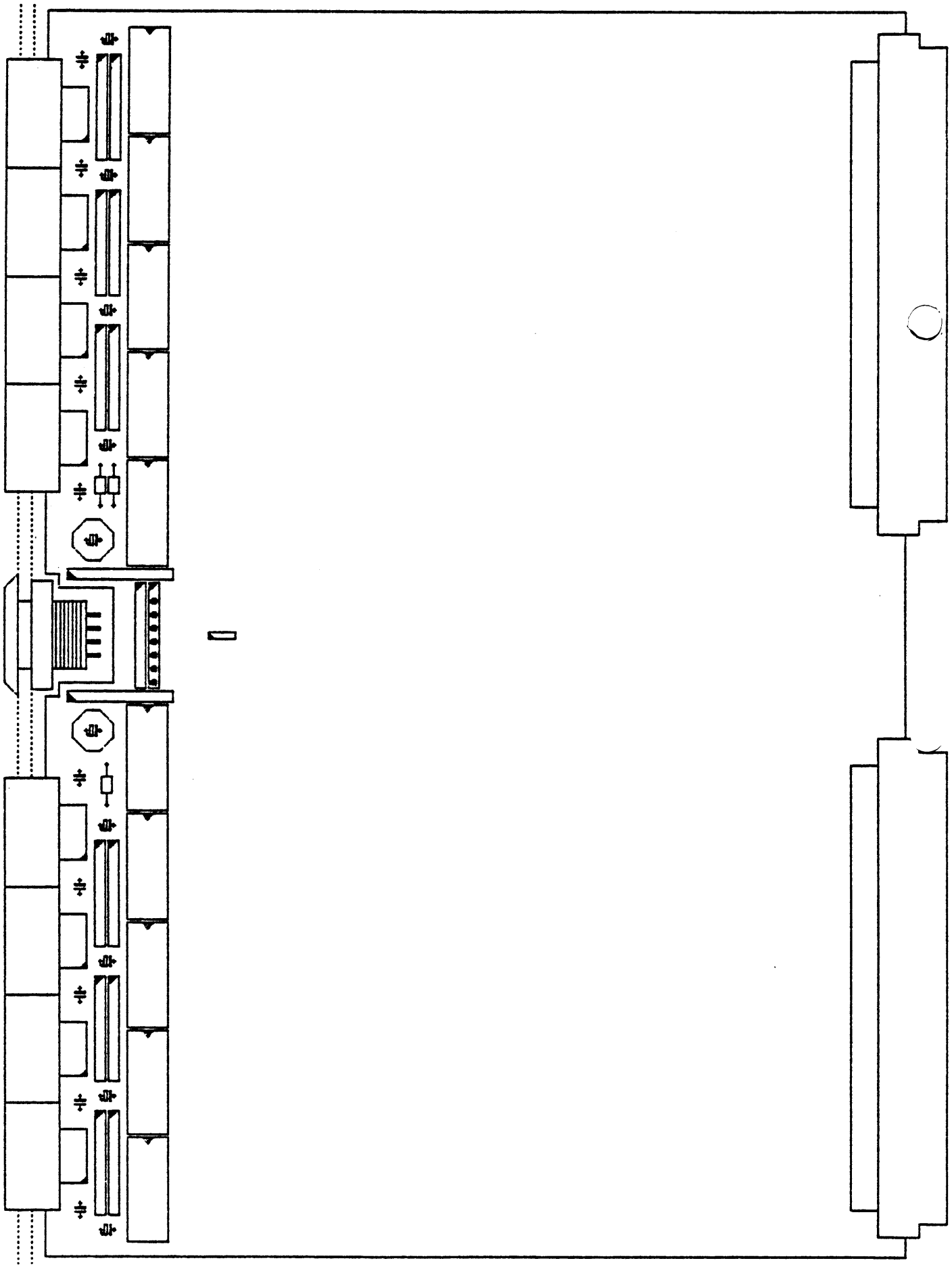
4.3.

Figure 10 : The Jumpers of the Link switch section



5.

Figure 11 : The Link buffers



5.

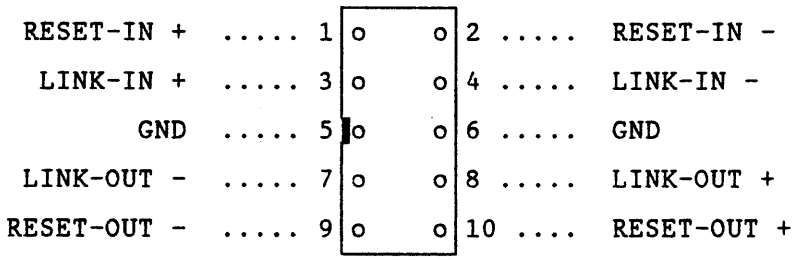
5. The Link buffers

In order to be able to employ the VMTM module in larger networks, nine external link channels have been provided (St.1 ... St.9). In the link buffer section, the internal TTL link channel signals are transformed to the RS422 standard. This measure ensures a considerably higher security of the data transmission over large distances.

5.1. Local Connections with other Modules

Link cabling between several boards within the equipment is effected by user operated flat-cable connections located on the front panel.

10-way connector pin-out (St. 1 -8)



5.2. Connections in distributed Systems

Screened twisted-pair cables are used for the links in the distributed transputer systems. In the VMTM module these connections are made via the link-plug St.9. Distances of up to 10 m may be covered using a transmission rate of 20 Mbit/s. Greater distances may be covered by setting the transmission rate to 10 or 5 Mbit/s.

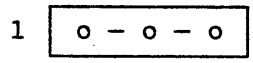
Furthermore it is possible to adopt the INMOS-Standard via this link channel.

This is accomplished by changing the resister- network position from 'RP3' over to 'RP4':

Position 'RP3': MEGAFRAME - Standard
Position 'RP4': INMOS - Compatibily.

Furthermore, jumper J6 can be configured accordingly:

J6 Standard choice:



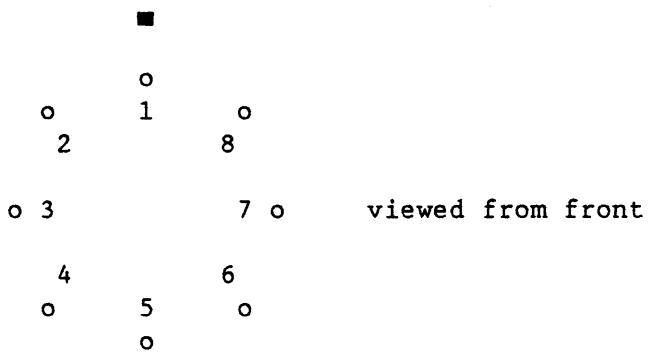
MEGAFRAME - Standard: 1A jumpered
INMOS -Compatibility: 1B jumpered

Using the INMOS- adaption the maximal transmission distance is reduced to 1.50 m!

5.2.

St. 9

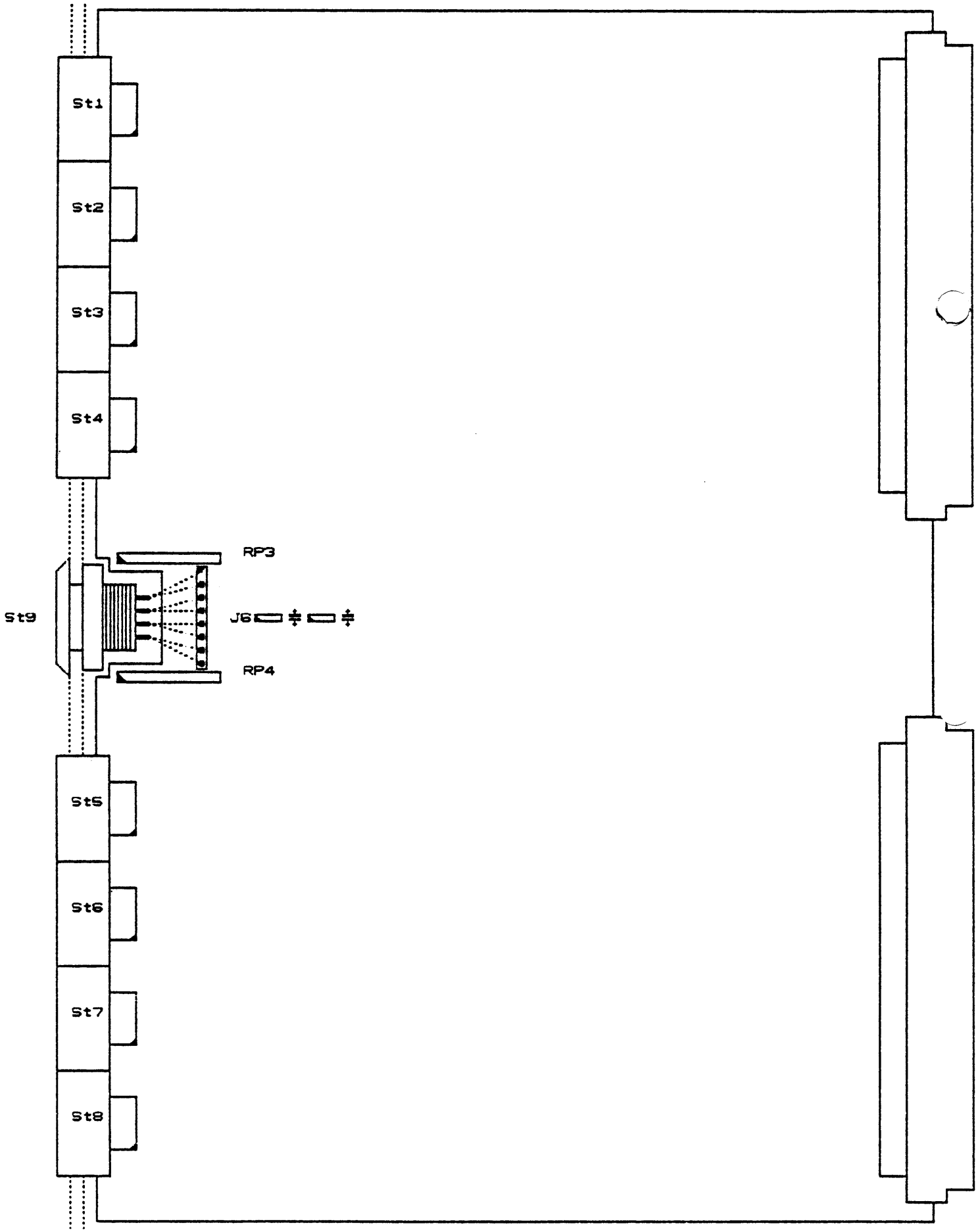
8-way round socket pin-out (Lemosa EGG 2B308CNL)



MEGAFRAME-Standard		INMOS-Compatibility	
Pin	Function	Pin	Function
1	RESET-OUT +	1	nc
2	RESET-OUT -	2	RESET-OUT
3	LINK-OUT +	3	LINK-OUT
4	LINK-OUT -	4	GND
5	LINK-IN -	5	nc
6	LINK-IN +	6	LINK-IN
7	RESET-IN -	7	RESET-IN
8	RESET-IN +	8	nc

5.2.

Figure 12 : The Jumpers of the Link buffer Section



6. Technical Data

VME- Spec. Rev.C: IEC 821, IEEE P1014/D 1.0
Modes of operation: A24/A32/D8

Link-buffers: 9 * RS-422,
link I/Os match cable impedance of 100 Ohm,
open link inputs have logic zero level (no signal)

Board: standard double euro card 233.5 * 160 mm , 7-layer multilayer

DC-Voltage-Supply: 5.0 V ± 5%

max. Current: 4.5 A